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54 **Method and apparatus for executing object code instructions compiled from a high-level language source.**

57 A high-level language processor is utilized in a system with a conventional host computer for executing object code instructions compiled from a high-level language source. Object code instructions specifying low-level operations (e.g., input/output, interrupt, and scheduling) are executed in the host computer in accordance with a stored emulator program. Upon identification by the emulator program of an object code instruction specifying a high-level operation, the language processor is activated. The central processing unit (CPU) in the language processor reads object code context section information from the host computer memory into a local memory. Using an instruction pointer in the context section, the language processor CPU reads the next high-level language object code instruction from the procedure section in the host computer memory and performs a required complex operation. Execution of the object program by the language processor continues until an input/output command is encountered, whereupon the information in the context section is written back into the host computer memory and an interrupt is issued to re-activate the emulator program. The emulator program then runs executing the input output command and continues until the next high-level language object code instruction is encountered. Object code context section information is switched back and forth in the foregoing manner between the host computer memory and the language processor local memory until the entire object program has been executed.

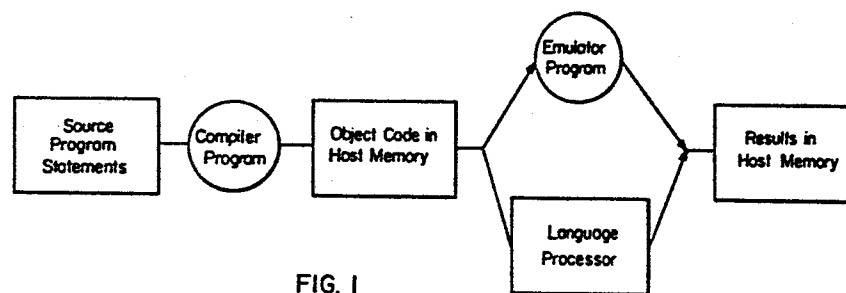


FIG. 1

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METHOD AND APPARATUS FOR  
EXECUTING OBJECT CODE INSTRUCTIONS

15 COMPILED FROM A HIGH-LEVEL LANGUAGE SOURCE

The present invention relates to processing of high-level language commands in a computer system; and more particularly, it relates to a hardware high-level language processor for use in a system with a conventional host computer.

Heretofore, when running a high-level language (e.g., COBOL, PASCAL, FORTRAN, BASIC) computer program, it has been necessary to use a compiler program to convert the program commands to object code or machine language. The object code is then executed by an emulator program in the computer system. Run times of such execution are lengthy because each high-level language object code command can require several hundred system memory cycles to execute. Improvements in computer system performance have been achieved by increases in memory size and memory access speed. Also, there have been improvements in the central processing unit (CPU). Along with these improvements, high-level language processing performance has correspondingly been improved, but the approach has remained the same.

In accordance with the present invention, a language processor is utilized in a system with a conventional host computer to execute object code instructions compiled from a high-level language source. In accordance with the  
5 present invention, high-level language operations are performed in the language processor, and the low-level operations including input/output, interrupt, and scheduling operations are performed in the host computer.

10 Apparatus in accordance with the present invention comprises a host computer having a memory containing the compiled object code instructions. The host computer executes in accordance with a stored emulator program only object code instructions specifying low-level operations.  
15 A language processor is coupled to the host computer and activated thereby upon identification by the emulator program of an object code instruction specifying a high-level operation. The language processor accesses the host computer memory and executes the high-level instruction.

20 Before executing a program, the object code consisting of a procedure section, a data section, and a context section is placed in the host computer memory in the same manner as if the program were to be executed by  
25 the software emulator program. The emulator program executes only those object code commands that specify a low-level operation. Upon encountering an object code command in the program that requires a complex operation, the emulator program provides the address of the context  
30 section of the program to the language processor. The emulator program then ceases operation, although the host computer may continue to attend to other ongoing input/output operations. The language processor is activated by the setting of a pointer to the context  
35 section and reads the information from the context section of the object code. Using an instruction pointer in the

context section, the language processor reads the next object code command from the host computer memory and performs the required complex operations. Execution by the language processor of the object code program continues until a low-level operation object code command is encountered, whereupon the language processor writes the context section information back into the host computer memory and issues an interrupt to the host computer to re-activate the emulator program.

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The operation of the system continues under the direction of the emulator program until the next complex object code command is encountered. Object code context section information is switched back and forth between the language processor in the host computer memory until the entire program has been executed.

The language processor may be coupled to the host computer over a system bus. The language processor includes a central processing unit (CPU), a control memory storing microcode commands for execution by the CPU and a local data memory. As indicated in the discussion of the method of the present invention for processing object code commands, the CPU of the language processor is activated upon identification by the emulator program in the host computer of an object code instruction specifying a high-level operation. Upon activation, the CPU accesses the host computer memory to read information from the context section of the object code and store it in the local data memory of the language processor. Thereafter, the CPU accesses the host computer memory using an instruction pointer in the stored context section information to read the next command from the procedure section of the object code and execute the specified high-level operation.

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A written description setting forth the best mode presently known for carrying out the present invention, and of the manner of implementing and using it, is provided by the following detailed description of preferred  
5 embodiments which are illustrated in the attached drawings wherein:

Fig. 1 is a diagram of the operation of a system in accordance with the present invention for processing  
10 high-level language commands;

Fig. 2 is a diagram of the system concept illustrating the arrangement of system elements;

15 Fig. 3 is a diagram of object code context section switch operation;

Fig. 4 is a diagram of language processor functional elements: and  
20

Fig. 5 is a schematic of circuitry for implementing the test and status logic block indicated in Fig. 4.

#### Detailed Description of a Preferred Embodiment

25

##### A. Structure of High-Level Language Object Code

Languages are compiled into object programs that all have the same basic structure, regardless of language.  
30 There are three classes of data generated by a compiler to define an executable object program: a procedure section, a data section, and a pseudo-machine context section. The procedure section contains codes specifying which high-level language operations are to be performed and in what  
35 order. The data section contains data to be acted upon and a place to put results. The pseudo-machine context

section contains information that completes the meaning of the codes in the procedure section and storage for temporary results.

5        In the Context Section, the Instruction Pointer is a value which points to the command in the Procedure Section which is to be executed next. The Accumulator(s) (and/or a Stack) are storage locations reserved for intermediate results left between commands. The Data Section pointers  
10 are values which indicate where in the Data Section various data items are located. The Status Flags are values which temporarily hold control information between commands. They along with the Instruction Pointer determine which commands are to be executed next.

15

      In the conventional implementation of High-Level Languages, an emulator program is run which performs, in software, the operations that need to be done to execute the program specified in the Procedure Section, above.  
20 Using the Instruction Pointer (from the Context Section) the emulator references a command in the Procedure Section. The command code is then decoded (by emulator software) to determine what action to perform on the Data and Context Sections. The emulator program then operates  
25 on the Data and Context Sections to perform the specified operation. When that is done, the sequence is repeated for the next command in the Procedure Section until the entire High-Level Language object program is completed. Examples are:

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	Language	Compiled	
	<u>Source</u>	<u>Object Code</u>	<u>Executed By Emulator</u>
	COBOL	POPS Commands	"POPS Interpreter"
5	PASCAL	P-Codes	"P-Code Machine Emulator"

B. System Concept

Referring now to Figs. 1-3, the system concept  
10 and operation thereof in accordance with the present  
invention for processing high level language commands is  
diagramed. In Fig. 1, the operation indicated shows that  
source program statements are compiled using a compiler  
program into object code stored in the memory of a host  
15 computer. Low-level operations including input/output,  
interrupt, and scheduling operations are executed using a  
software emulator program, and the results are stored in  
the host computer memory. The complex or high-level  
operations in the program are specified by the object code  
20 in the host computer memory, and are executed by the  
hardware language processor.

Fig. 2 shows that the host central processing unit  
(CPU), the host computer memory, the language processor  
25 and the input/output interfaces coupling to peripheral  
devices are all coupled to a common system by memory bus.  
The bus may be, for example, in accordance with the UNIBUS  
used in computer systems made by the Digital Equipment  
Corporation. Alternately, the system memory bus may be a  
30 TILINE bus system as utilized in the computer systems of  
Texas Instruments Inc.

In Fig. 3, there is diagramed the host computer  
memory contents and the language processor central pro-  
35 cessing unit (CPU) and local data memory. Fig. 3 is  
illustrative of the switching operation between the host



computer memory and the language processor local data memory involving object code context section information. When the emulator program in the host computer encounters an object code command in the data section which requires  
5 complex high-level language operations (i.e., the operations do not involve input/out, interrupt or scheduling operations), the emulator program places the address of the context section of the program in an interface register to the language processor. The emulator program then  
10 ceases operation, while allowing the host computer to attend to other ongoing input/output operations. The language processor CPU which is activated by the setting of a pointer to context reads the information from the context section of the host computer memory and places it  
15 into a local data memory in the language processor. Using the instruction pointer in the context section, the language processor CPU reads the next object code command from the procedure section of the object code and performs the required complex operations. The language processor  
20 continues to execute object code program commands until a low-level command is encountered. Upon identification of a low-level operation, the language processor CPU writes the context section information back into the host computer memory and issues an interrupt to the host computer  
25 to re-activate the emulator program. The emulator program then resumes operation and continues until another complex high-level language command is encountered in the object code program. Context section information is then switched back to the language processor. Switching of the  
30 context section back and forth between the host computer memory and the language processor local data memory continues until the entire program has been executed.

Operation in accordance with the present invention  
35 may include more than one language processor to provide even higher levels of performance and redundancy. This

configuration is also illustrated in Figs. 2 and 3 wherein a second language processor is shown coupled to a first language processor. Operation in such a configuration may be required where the Host computer is run in a multi-  
5 programming mode. For operation with multiple language processors, the emulator program must be designed to assign an available language processor when a highlevel language instruction is bid to run. As used herein, the term "multi-programming" refers to the running of multiple  
10 programs using a single host computer.

### C. Language Processor Structure

Referring now to Fig. 4, there is shown a functional  
15 diagram of the structure of the language processor. In general, the language processor comprises a CPU having control memory storing microcode commands that direct functional operations in the processing procedure. The microcode is initially loaded into the language processor  
20 by the host computer. Suitably, the microcode may be contained on a diskette and loaded into the language processor control memory from the diskette. The language processor may also be viewed as comprising two cooperative parts. These are a data path and a microcontroller. The  
25 data path includes those portions which perform operations on data, and the microcontroller includes those portions which provide the control commands to the data path portion.

30 In the language processor 10 shown in Fig. 4, the microcontroller portion 12 is shown to include a microsequencer 14 providing an address to control memory 16. The microinstruction pointer selects the next microinstruction to be executed. The microsequencer also  
35 contains logic to select the next value to be placed into the microinstruction pointer which value may either be an

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incremented current value or a new value loaded from B-bus 18 or from pipeline register 20.

Control memory 16 stores the microcode which determines the overall operation of the language processor. Each word is one microinstruction of the microcode. Microcode is loaded into control memory 16 through load buffers 22 comprising bi-directional data transfer logic. Preferably, control memory 16 is 8,192 words by 64-bits wide. Accordingly, load buffers 22 provide for the reading and writing of 64-bit wide words from the 16-bit host computer memory bus.

Pipeline register 20 is a 64-bit register used to hold the micro-command read from control memory 16. This register makes it possible for the language processor to overlap microinstruction fetch and execution. Outputs of pipeline register 20 are distributed as controls to other logic blocks within the language processor. Also, pipeline register 20 provides an address to local data memory 24.

Local data memory 24 comprises 1,024 registers, each of which is 16-bits wide. Data can be written into memory 24 or read out of memory 24 over the A-bus 26. Local data memory 24 functions to hold object code context section information which, of course, is switched between language processor 10 and the host computer.

Data buffers 28 and address buffers 30 couple to the host computer memory bus. These bi-directional drivers move data and memory address information respectively, between the host computer memory bus and the interface registers 32. The interface registers comprise four 16-bit registers containing information to be exchanged with the host computer memory bus. These four registers

include a read/write data register, two memory address registers, and a status register.

5       The interface registers 32 interconnect with load buffers 22 and data shifter 34. The data shifter allows data read from interface registers 32 to be shifted right or left and masked in order to select decimal digits from the 16-bit word.

10       Bits implemented in the interface status register are accessible to both the Host computer and the language processor. They, along with an interrupt to the host, provide the control communication between the processor and programs in the host. The bits indicate conditions  
15       inside the processor to the host and allow the host to start and stop the processor. For example, an IDLE bit indicates to the host that the processor is not running. The processor FAULT bit provides the combination Host processor with redundant back-up in case the processor  
20       fails. A self-test microprogram in the processor is run before the processor is used. If it sets the FAULT bit, then the interpreter program in the host is run to execute all of the object program commands. Although execution is very slow, the system can still be used.

25

      The A-bus 26 and the B-bus 1B present data to a decimal/binary arithmetic unit 36. Operations performed by the arithmetic unit are determined by commands from the microsequencer. The result of the operation is made  
30       available on the Y-bus 38. Preferably, the arithmetic unit is 16-bits or 4 decimal digits wide. The operations which arithmetic unit 36 is capable of performing include the following: binary or decimal addition or subtraction; all combinational logic operations; and left or right  
35       shifts.

Register file 40 contains registers providing storage of 16 words of data. The width of the register is 16-bits or 4 decimal digits. Any one of two registers can be selected to the Abus or the B-bus. A register selected to  
5 the B-bus may be loaded with data available on the Y-bus.

Finally, language processor 10 includes test and status logic 42. Control of microinstruction branching is by means of the test and status logic. This logic func-  
10 tions under control of the current microinstruction in pipeline register 20 to select some condition in the data path to be used in a determination of whether a micro-instruction branch would be performed.

15 Referring to Fig. 5, a schematic diagram for test and status logic 42 is presented. This circuitry basically samples data signals using a set of flip-flops contained in device 50 (SN74LS174 device) and flip-flop 52. The direct inputs CO, OV, N and Z are from the arithmetic  
20 logic unit 36. Bit 15 of the Y-B bus is applied to flip-flop 52 and entered therein by an address logic clock controlled by bit 34 from the pipeline register 20. The Key output of flip-flop 52 is applied along with the compliment of bit 34 from a pipeline register 22 AND GATE  
25 54. Bit 54 of the pipeline register and bit 15 of the Y-B bus are applied as inputs to AND GATE 56. OR GATE 58 receives the outputs of GATES 54 AND 56 and generates an output for entry in flip-flop device 50. The remaining input to flip-flop device 50 is from OR GATE 60 which  
30 receives the signals CYC and RMW which are derived from bits 0, 1, and 2 of the pipeline register 20. Flip-flop device 50 is clocked by the pipeline register clock.

The Key outputs of flip-flop device 50 are applied to  
35 various gates as shown to generate the indicated signals. These additional gates perform a re-coding function to

provide a more diverse set of microcode jump commands.  
For example, the combination of the EQ signal (Y-B bus =  
0) and the CO (no carry) signal in OR GATE 62 provides a  
re-coded signal indicating the Y-B bus is less than or  
5 equal to 0.

The re-coded signals are applied to selector circuits  
64 and 66 (SN74LS251 devices). Pipeline register bits 5,  
6 and 7 determine which of the 16 inputs will be tested.  
10 The output signal CC is applied to microsequencer 14 to  
indicate whether or not a microcode jump is to be per-  
formed.

15 D. Components For Implementing Language  
Processor Structure

Microsequencer 14 is made from an AM2910 integrated  
circuit described in the 1982 Integrated Circuit Catalog  
from Advanced Micro Devices Corporation.

20

Control memory 16 is made from MBB168-70 integrated  
circuits described in the 1982 catalog from Fujitsu  
Corporation, 2985 Kifer Road, Santa Clara, Calif. 95051.

25

Pipeline register 20 is made from SN74LS374 inte-  
grated circuits described in the 1982 Integrated Circuits  
Catalog from Texas Instruments Inc. of Dallas, Texas.

Local data memory 24 is made from AM2149 integrated  
30 circuit memories described in the 1983 Integrated Circuit  
Catalog from Advanced Micro Devices.

The arithmetic unit 36 can be realized using four  
AM29203 four-bit expandable bipolar microprocessor slice

integrated circuit devices available from Advanced Micro Devices. Register file 40 is part of the AM29203 device.

Data shifter 34 is realized using SM74LS253 multi-  
5 plexors available from Texas Instruments, Inc.

Microcode load buffers 22 are implemented using SN74LS245 integrated circuit devices available from Texas Instruments, Inc. Buffers 22 are coupled to data shifter  
10 34 and interface register 32 over the R-bus.

The status register portion of interface register 32 can be made of SN74LS399 integrated circuit devices. Output data drivers for driving the host computer memory  
15 bus can be SN74LS244 devices. The address registers can be SN74LS670 devices. The data register is made of AM2957 devices. Data buffers for driving the R-Bus can be SN74LS244 devices. Address buffers are suitably SN74LS670 devices. All of these devices are available from Texas  
20 Instruments except the AM2957 which is available from Advanced Micro Devices.

E. Microcode For COBOL Language Processor

25 The following microcode listing is for operation of the language processor 10 diagrammed in Figs. 1-4 to execute object code instructions compiled from COBOL source program statements. The following code particularly adapts the language processor to interface as a  
30 common peripheral device to DX10, DNOS, or COS 990 operating systems used in the computer series available from Texas Instruments, Inc. In such an installation, the language processor replaces the COBOL Interpreter to execute COBOL POPS commands directly in hardware. The  
35 microcode is in machine language form.

0000 6000009EBC700008  
0001 6000009EBC700010  
0002 6000009EBC70001E  
0003 7F12008DB5D00002  
0004 7F0A028DA59000CC  
0005 E000048AC5D007FE  
0006 7EC0488845D0020C  
0007 60001888C5D0018C  
0008 644D988845D001CE  
0009 6000009EBC300260  
000A 6455988845D00150  
000B 645D988845D00168  
000C 6465988845D0015E  
000D 6000408D0D90001E  
000E 6000009EBC300280  
000F 646D988845D0017E  
0010 6475988845D0012C  
0011 647D988845D0010C  
0012 6000009E8D90005C  
0013 6000009EBC300260  
0014 6485988845D0029E  
0015 648D988845D0020E  
0016 6495988845D0021E  
0017 6000009EBC7D00BE  
0018 7F0A0286C5D003CC  
0019 7F12008DB5900154  
001A 60000888C5D0020C  
001B 7EC0808DOC7D00DE  
001C 60000288ADD00000  
001D E00000888DD00002  
001E 649D988845D00220  
001F 64A5988845D002CC  
0020 6000009EBC300260  
0021 64AD988845D002D0  
0022 64B5808D0DD00000  
0023 7E00068DB47D011E  
0024 6004608D0DD00001  
0025 6000009EBC7D012E  
0026 7F0A0286E5D003BC  
0027 7F12008DB5900046  
0028 E0000888C5D00200  
0029 60E20092CDD00080  
002A 7EC0808DOC7C022B  
002B 60E20084CFD000F0  
002C 6000009EBC74022B  
002D 7E1C068DB47D0168  
002E 60000260A5D00000  
002F 7E90009EBC7E018B  
0030 6000006087D00000

0031 E000008D0DD00002  
0032 7E7A069E85D00000  
0033 6000026085D00000  
0034 6000009EBC7E01B0  
0035 6000006087D00000  
0036 6000009EBC7D01B0  
0037 7E56069E85D00000  
0038 7E2E069E85D00000  
0039 6000008D0DD00002  
003A E00462882D300169  
003B 6000026085D00000  
003C 6000009EBC7E01F0  
003D 6000006087D00000  
003E 7E1C068DB47D01F0  
003F 6000008D0DD00002  
0040 E0000288ADD00000  
0041 7E7A069E85D00000  
0042 616C608D0DD00000  
0043 7E00068DB47D021B  
0044 6164608D0C700A30  
0045 6000009E8D90009B  
0046 7E00068DB47D0230  
0047 60000260A5D00000  
0048 7E90009EBC7E0250  
0049 6000006087D00000  
004A E00460880D300233  
004B 6000009EBC700A30  
004C 7E00068DB47D0260  
004D 6004628027D00001  
004E FE80008D05300266  
004F 6000009E8D500000  
0050 7E06068DB47D0280  
0051 7E58068DB47702CB  
0052 6004628027D00001  
0053 7E80008D05D00006  
0054 FE46068DB5D00000  
0055 7E18068DB47702D0  
0056 6004608D0DD00001  
0057 7E80009E8D300280  
0058 6000009E8D500000  
0059 6000469E04700290  
005A 6000469E047002B0  
005B 6000009EBC7D02DB  
005C 7F12008DB5D00002  
005D 7F0A028DA59000BB  
005E 6002068DB5D00000  
005F 9F04649105D00000  
0060 60000488C5D0000B  
0061 7EC0408D0C3006DB



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0063 6000009E8C300700  
0064 6002068D847D0321  
0065 7F04628027D00000  
0066 9E80008D05D00006  
0067 6000009E8D900048  
0068 6000009E8C3006D8  
0069 60000888C5D00200  
006A 6000009E8C7D0350  
006B 7F0A0286C5D003B0  
006C 7F12008D8590004C  
006D 7EC0808D0C3006D8  
006E 6000009E8C7D0370  
006F 7F0A0286C5D003C0  
0070 7F12008D85900044  
0071 60000888C5D001F8  
0072 60E20092CDD00080  
0073 7EC0808D0C7C06A0  
0074 60E20084CFD000F0  
0075 6000009E8C7406A0  
0076 6002068D85D00001  
0077 7F04626005D00000  
0078 7E1C0A8D847E03D0  
0079 6000006087D00000  
007A 7E360A9E847D03D0  
007B 6000208D2DD00000  
007C 9F04A08B0DD00002  
007D 6000026085D00000  
007E 7F04608D0C7E0600  
007F 6000006086700600  
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0085 6000009E8C700848  
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0087 6000009E8C700848  
0088 6000009E8C7048B8  
0089 6000009E8C7048D0  
008A 6000009E8C7048E8  
008B 6000009E8C705148  
008C 6000009E8C702FD8  
008D 6000009E8C702FB8  
008E 6000009E8C702F98  
008F 6000009E8C7050A8  
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00CD 6162068D847E0678  
00CE 6000006087D00000  
00CF 7F04608D0DD00000  
00D0 6000009E8C7D0680  
00D1 6000008D0DD00002  
00D2 8000208D2DD00000  
00D3 6000009E8C700750  
00D4 6000009E8D900098  
00D5 6002068D847D06A9  
00D6 60000260A5D00000  
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The foregoing description of the invention has been directed to a particular preferred embodiment for purposes of explanation and illustration. It will be apparent, however, to those skilled in this art that the method in  
5 apparatus may be utilized for other program languages and COBOL. Also, it will be apparent that many modifications and changes in both apparatus and method may be made without departing from the scope of the invention. It is the applicant's intention of the following claims to cover  
10 all equivalent modifications and variations as fall within the scope of the invention.

CLAIMS:

1. Apparatus for executing object code instructions  
compiled from a high-level language source characterized  
5 in that:

a host computer having a memory containing the  
compiled object code instructions;

10 said host computer executing in accordance with  
a stored emulator program only object code  
instructions specifying low-level  
operations; and

15 a language processor activated by the host  
computer upon identification by the  
emulator program of an object code  
instruction specifying a high-level  
operation, for accessing the host computer  
20 memory and executing the high-level  
instruction.

2. The apparatus of claim 1 wherein said host computer  
25 is operable in a multiprogramming mode, and wherein a  
second language processor is coupled to said language  
processor.

30 3. Apparatus for executing object code instructions  
compiled from a high-level language source and including a  
procedure section, a data section, and a pseudo-machine  
context section, characterized in that:

35 a host computer having a memory containing the  
compiled object code instructions,

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said host computer executing in accordance with  
a stored emulator program only object code  
instructions specifying low-level  
operations;

5

a language processor coupled to the host  
computer over a system bus,

10 said language processor including a central  
processing unit (CPU), a control memory  
storing microcode commands for execution by  
the CPU, and a local data memory;

15 the CPU being activated upon identification by  
the emulator program in the host computer  
of an object code instruction specifying a  
high-level operation, and upon activation  
the CPU accessing the host computer memory  
to read information from the context  
20 section of the object code and store it in  
the local data memory, and thereafter the  
CPU accessing the host computer memory  
using an instruction pointer in the stored  
context section information to read the  
25 next instruction from the procedure section  
of the object code and execute the  
specified high-level operation.

30 4. The apparatus of claim 3 wherein the CPU continues to  
execute instructions in the procedure section of the  
object code until an input/output instruction is identi-  
fied.

35

5. The apparatus of claim 4 wherein the CPU upon identifying an input/output instruction writes the context section information back into the host computer memory and issues an interrupt to the host computer to re-activate  
5 the emulator program.

6. A language processor for coupling over a system bus to a host computer having a memory containing object code  
10 instructions compiled from a high-level language source and including a procedure section, a data section, and a pseudo-machine context section, said host computer executing in accordance with a stored emulator program  
only object code instructions specifying low-level operations,  
15 tions, characterized in that:

a central processing unit (CPU);

a control memory storing microcode commands for  
20 execution by the CPU;

a local data memory; and

an interface register;  
25

said CPU being activated by the host computer to access the host computer memory and read information from the context section of the object code and store it in the local data  
30 memory;

said CPU using an instruction pointer in the stored context section information to read the next instruction from the procedure  
35 section of the object code in the host

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computer memory and execute the specified high-level operation.

5 7. Method of executing object code instructions compiled from a high-level language source, characterized in that the steps of:

10 providing compiled object code instructions in a host computer memory;

15 executing in accordance with an emulator program stored in a host computer only object code instructions specifying low-level operations;

activating a processor upon identification by the emulator program of an object

20 code instruction specifying a high-level operation, to access the host computer memory and read the next object code instruction; and

25 executing in the processor the high-level instruction defined by the object code instruction.

30 8. Method of executing object code instructions compiled from a high-level language source, characterized in that the steps of:

35 providing compiled object code instructions in a host computer memory, said code including a

procedure section, a data section, and a  
pseudo-machine context section;

5       executing in accordance with an emulator program  
      stored in a host computer only object code  
      instruction specifying low-level  
      operations;

10       activating a central processing unit (CPU)  
      coupled to the host computer upon  
      identification by the emulator program of an  
      object code instruction specifying a high-  
      level operation;

15       accessing the host computer memory with the CPU  
      to read information from the context  
      section of the object code and store it in  
      a local data memory;

20       accessing the host computer memory with the CPU  
      and using an instruction pointer in the  
      stored context section information to read  
      the next instruction from the procedure  
      section; and

25       executing in the CPU the high-level operation  
      specified by the instruction.

30   9.   The method of claim 8 further characterized in that  
     the steps of:

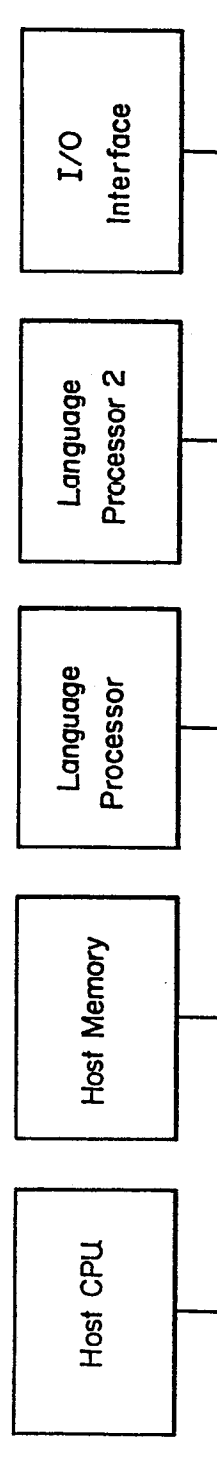
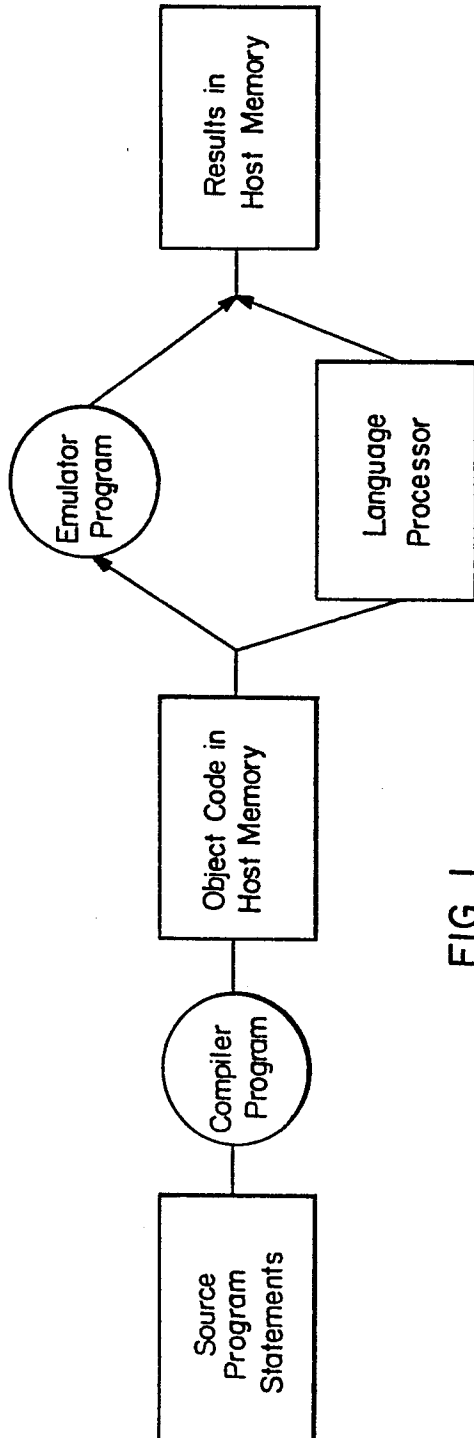
     repeatedly accessing the host computer memory to  
     read instructions for execution until an  
35   input/output instruction is identified;



writing the context section information back  
into the host computer memory; and

issuing an interrupt to the host computer to  
re-activate the emulator program.

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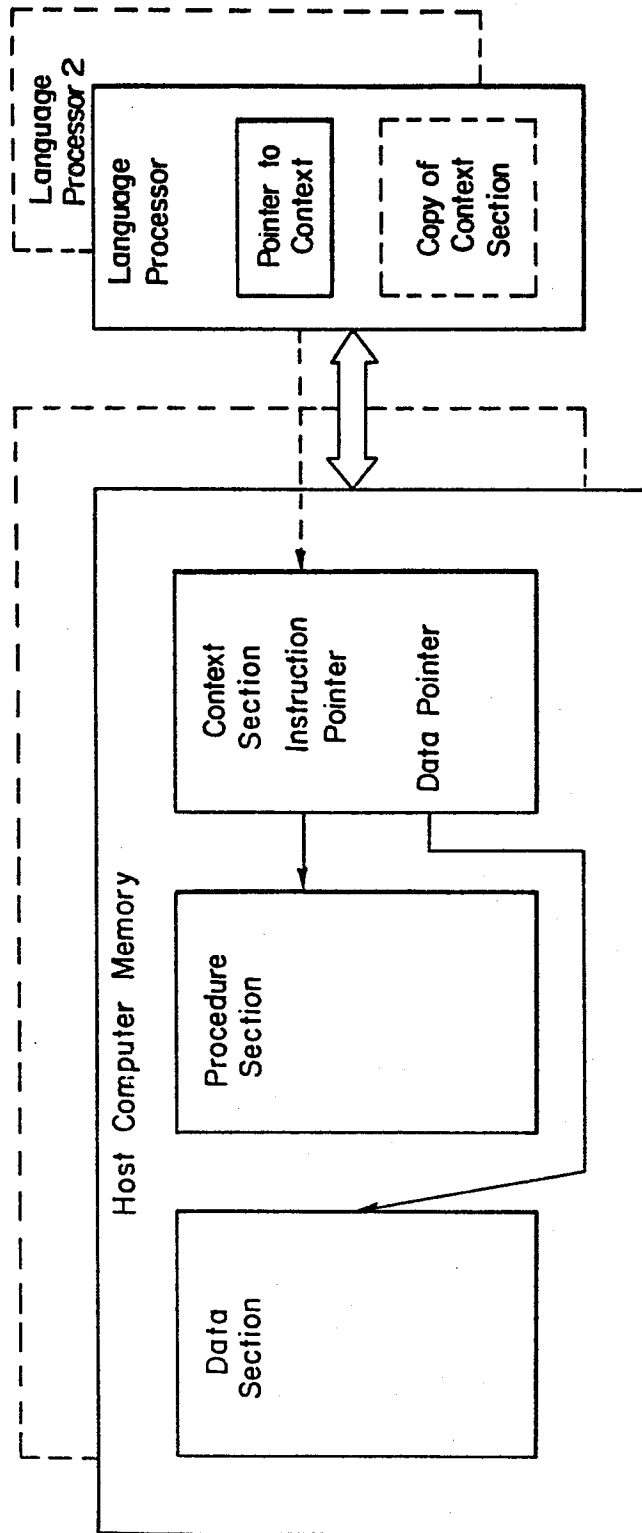


FIG. 3

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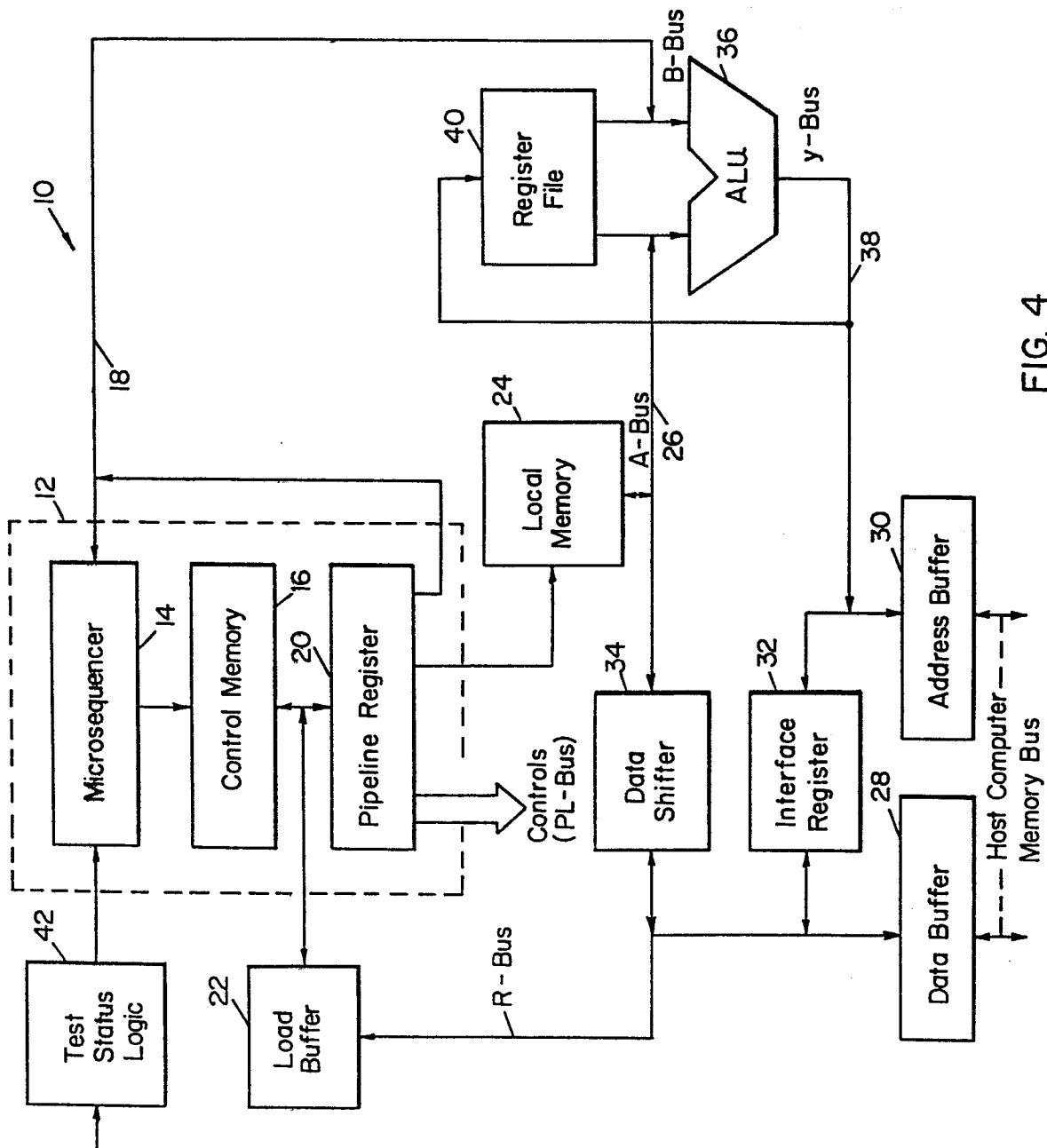


FIG. 4



FIG. 5