X-LINK File Accelerator™

USER INTERFACE OVERVIEW

The X-LINK File Accelerator (boards and software) can support a variety of concurrent processing functions. Most of the system software and support functions were written to allow adaptability for different tasks. Although most of the software written for the system so far involves the use of the X-LINK System as a file acceleration system, components of this software can be used for other types of processing.

The general approach Ten X has taken to allow custom applications to run on the system is to provide a user shell process through which the application interfaces to the X-LINK File Accelerator software. This shell can load the user's code into the DRAM memory, handle DOS EXE file relocation, if necessary, and start up the code. Custom software interrupt calls can be designed to the user's specifications to provide access to the X-LINK system.

Communication between the host AT and the user application is done with a defined interface. This interface involves an interrupt handler on the AT side which handles packet communication. Packets include a Ten X header and user data. Software is available to transfer packets from AT memory to 80186 memory and back. The user application on the board usually receives or sends the address of this packet with its interface to the Ten X software.

Typical functions provided by the Ten X interface shell are memory management, process communication and task scheduling. A number of processes currently exist for communication with the host AT screen and keyboard. Routines also exist for limited DOS support. A complete high speed file system is supported on the X-LINK File Accelerator version of this product and user applications can make use of this support if desired.

User applications can access 80186 resources such as timers, DMA, interrupts and I/O ports. The use of these hardware resources usually requires a portion of the application to run only on one of the 80186 processors.

A number of debugging tools have been developed for use with the board. A debugger similar to the DOS debugger can be run on the board. This debugger handles problems with breakpointing with two processors running and communication with the host AT. A concurrent packet generator has been written for the AT side. This program can generate multiple requests to the board and keep statistics on performance and errors. Other support on the board includes error handling routines, packet dumps and some statistical analysis tools.

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HARDWARE OVERVIEW

The X-LINK File Accelerator is designed for execution of high speed concurrent tasks in AT based systems. The board uses two 80186 processors, each of which can run concurrently with the host AT processor. These processors work best in a task oriented environment with the tasks divided into subsets which can be run simultaneously. Two processors also allow multiple requests to be processed at the same time. The input/output load on the board is divided between the two processors. One processor interfaces to the host AT and each processor has an expansion port connector.

There are several different banks of memory on the board. Each processor has 512K bytes of no-wait state memory for execution of code and private data. Both processors and the AT share a 1Mbyte three-way memory. The AT addresses this memory in 32K or 64K blocks. The 80186's address 512K of this memory directly and another 512K in 64K blocks. This extra 512K of memory is primarily for use as a cache. Semaphores and software/hardware locking mechanisms are used to force sequential access to data structures in common memory.

HARDWARE SPECIFICS

Full slot AT board

Two 80186 microprocessors

- Speed - 12.5MHz (board can accomodate faster parts)
- 2 DMA channels
- 3 timers
- Interrupt handler
- INTEL instruction set (compatible with most code for AT)

1Mbyte 3-Way Dynamic RAM

- Signetics Dual Port Dynamic RAM Controller
- 1 wait-state single access
- Lower cost 512K byte option available

2 banks of 512K byte Dynamic RAM

- 1 bank for each processor
- No-wait states
- Provides high speed execution of common code

Memory Mapped AT interface

- AT has access to all 3-WAY memory

Full expansion port

- Interface to the 80186 bus

Piggy-back expansion port

- Subset of full expansion connector