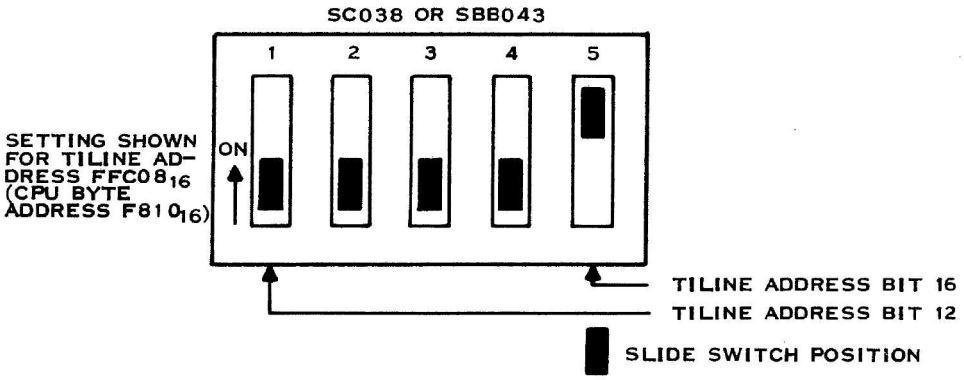

HEXADECIMAL ADDRESS		TILINE ADDRESS SWITCHES				
TILINE	CPU BYTE	1	2	3	4	5
FFC00	F800	OFF	OFF	OFF	OFF	OFF
FFC08	F810	OFF	OFF	OFF	OFF	ON
FFC10	F820	OFF	OFF	OFF	ON	OFF
FFC18	F830	OFF	OFF	OFF	ON	ON
FFC20	F840	OFF	OFF	ON	OFF	OFF
INCREMENTS OF 08$_{16}$	INCREMENTS OF 10$_{16}$	STRAIGHT BINARY SEQUENCE				
FFCF0	F9E0	ON	ON	ON	ON	OFF
FFCF8	F9F0	ON	ON	ON	ON	ON

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Figure 2-15. TILINE Base Address Switch Settings

The slave idle F/F and associated logic allow the disk controller to respond with a simulated W7 word if the controller is busy. This simulated W7 word has a zero at bit 0 to identify busy status, and bits 1-15 are meaningless. No register file operations are performed, and the on-going controller operation is not disrupted.