HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4

16384-word × 1-bit Dynamic Random Access Memory

The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe ($\overline{\text{CE}}$). Data out of the HM4716A will remain valid from the access time from the Column Address Strobe unitl $\overline{\text{CE}}$ goes into precharge (logic 1). However, in early write cyles ($\overline{\text{W}}$ active low before $\overline{\text{CE}}$ goes low), the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

1. Common I/O Operation

If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.

2. Data Output Control

Data well remain valid at the output during a read cycle from TCELQV until $\overline{\text{CE}}$ returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods of Chip Selection

Both $\overline{\text{CE}}$ and/or $\overline{\text{RE}}$ can be decoded for chip selection.

4. Refresh

Refreshing can be accomplished every 2ms by either of the two following methods:
(1) normal read or write cycles on 128 addresses, A0 to A6.
(2) $\overline{\text{RE}}$ only cycles on 128 addresses, A0 to A6.

A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

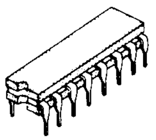
$\overline{\text{RE}}$ only regreshes results in a substantial reduction in operating power.

5. Page Mode Operation

The HM4716A is designed for page mode operation.

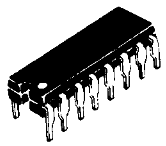
Old	New	Definitions
A0-A6	A0-A6	Address Inputs
$\overline{\text{CAS}}$	$\overline{\text{CE}}$	Column Address Strobe
D_{IN}	D	Data In
D_{OUT}	Q	Data Out
$\overline{\text{RAS}}$	$\overline{\text{RE}}$	Row Address Strobe
$\overline{\text{WRITE}}$	$\overline{\text{W}}$	Read/Write Input
V_{BB}	VBB	Power (−5V)
V_{CC}	VCC	Power (+5V)
V_{DD}	VDD	Power (+12V)
V_{SS}	VSS	Ground

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4



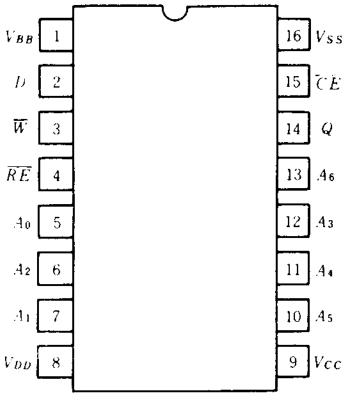
(DG-16A)

HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4



(DP-16)

■ PIN ARRANGEMENT



(Top View)

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4

■ FEATURES

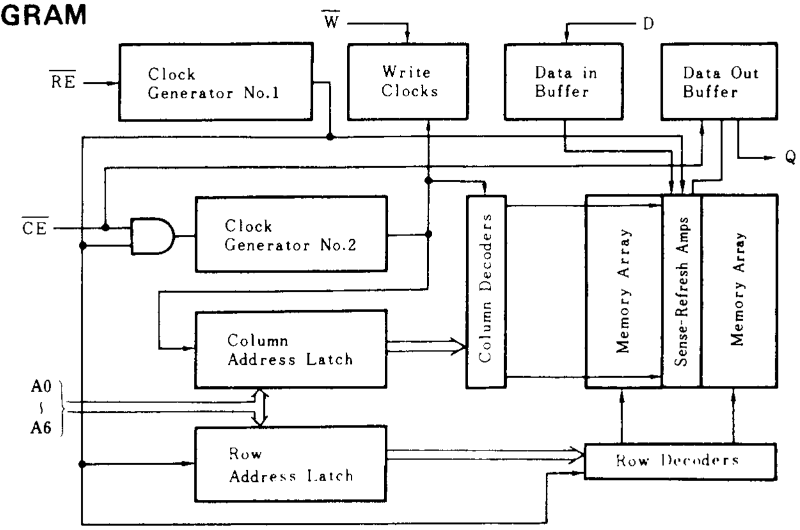
- All Inputs Including Clocks TTL Compatible
- Input Latches for Address and Data in
- Three-State TTL Compatible Output
- Common I/O Capability
- Only 128 Refresh Cycles Required Every 2ms
- Standard Power Supplies +12V, +5V, −5V (all with 10% tolelance)
- Maximum Access Time

HM4716A-1	120ns
HM4716A-2	150ns
HM4716A-3	200ns
HM4716A-4	250ns

- Read or Write Cycle Time

HM4716A-1	320ns
HM4716A-2	320ns
HM4716A-3	375ns
HM4716A-4	410ns

■ FUNCTIONAL DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to VBB	−0.5V to+20V
Voltage on VDD, VCC Supplies relative to VSS	−0.5V to +15V
Voltage on Q pin relative to VSS	−0.5V to +10V
Operating Temperature, TA (Ambient)	0°C to +70°C
Storage Temperature (Ambient)*	−65°C to +150°C
Short-circuit output current	50mA
Power dissipation	1W

* In case of HM4716AP Series are −55°C to +125°C.

■ RECOMMENDED DC OPERATING CONDITIONS (TA=0 to +70℃)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	VDD	10.8	12.0	13.2	V	1
	VCC	4.5	5.0	5.5	V	
	VSS	0	0	0	V	
	VBB	−4.5	−5.0	−5.5	V	
Input High (logic 1) Voltage $\overline{RE}$, $\overline{CE}$, $\overline{W}$	VIHC	2.7	—	6.5	V	1
Input High (logic 1) Voltage All inputs except $\overline{RE}$, $\overline{CE}$, $\overline{W}$	VIH	2.4	—	6.5	V	1
Input Low (logic 0) Voltage all inputs	VIL	−1.0	—	0.8	V	1

■ **DC ELECTRICAL CHARACTERISTICS** (TA=0 to +70°C, VDD=12V±10%, VCC=5V±10%, VBB=−5V±10%, VSS=0V)

Parameter	Symbol	min.	max.	Units	Notes
OPERATING CURRENT	IDD1	—	35	mA	2
Average Power Supply Operating Current	ICC1	—	—	mA	3
($\overline{RE}$, $\overline{CE}$ Cycling; TRELREL=375ns)	IBB1	—	300	μA	2
STANDBY CURRENT	IDD2	—	1.5	mA	
Power Supply Standby Current ($\overline{RE}$ = $\overline{CE}$ = VIHC)	ICC2	−10	10	μA	5
	IBB2	—	100	μA	
REFRESH CURRENT	IDD3	—	27	mA	2
Average Power Supply Current, Refresh Mode	ICC3	−10	10	μA	5
($\overline{RE}$ Cycling, $\overline{CE}$=VIHC; TRELREL=375ns)	IBB3	—	300	μA	2
PAGE MODE CURRENT	IDD4	—	27	mA	
Average Power Supply Current, Page-mode Operation	ICC4	—	—	mA	3
($\overline{RE}$=VIL, $\overline{CE}$ Cycling; TCELCEL=225ns)	IBB4	—	300	μA	
INPUT LEAKAGE Input Leakage Current, any Input (VBB=−5V, VIN=0 to +7V, all other pins not under test=0V)	IIL	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Q is Disabled, VOUT=0 to +5.5V)	IOL	−10	10	μA	5
OUTPUT LEVELS Output High (Logic 1) Voltage (IOUT=−5mA)	VOH	2.4	VCC	V	4
Output Low (Logic 0) Voltage (IOUT=4.2mA)	VOL	0	0.4	V	

NOTES

1. All voltages referenced to VSS, VBB must be applied before and removed after other supply voltage.
2. Current depend on cycle rate: maximum current is measured at the fastest cycle rate.
3. ICC depends upon output loading. The VCC supply is connected to the output buffer only.
4. Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be reduced to VSS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.
5. ICC2, ICC3 and IOL consists of leakage current only.
6. AC measurements assume TT = 5ns.
7. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VIL.
8. Assumes that TRELCEL = TRELCEL (max). If TRELCEL is greater than the maximum recommended value shown in this table, TRELQV exceeds the value shown.
9. Assumes that TRELCEL = TRELCEL (max).
10. Measured with a load circuit equivalent to 2TTL loads and 100pF (in case of HM4716A-2:1 TTL and 50pF). And VSS + 0.8V, VSS + 2.0V are the reference level for measuring timing of Q.
11. TCEHQZ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation with the TRELCEL (max) limit insures that TRELQC (max) can be met TRELCEL (max) is specified as a reference point only; if TRELCEL is greater than the specified TRELCEL (max) limit, then access time is controlled exclusively by TCELQV.
13. These parameters are referenced to $\overline{CE}$ leading edge in early write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
14. TWLCEL, TCELWL and TRELWL are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if TWLCEL = TWLCEL (min), the cycle is an early write and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if TCELWL = TCELWL (min) and TRELWL will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Capacitance measured with Boonton Meter or effective capacitance measuring method.
16. $\overline{CE}$ = VIHC to disable Q.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(TA=0 to +70°C, VDD=12V±10%, VCC=5V±10%, VSS=0V, VBB=−5V±10%)

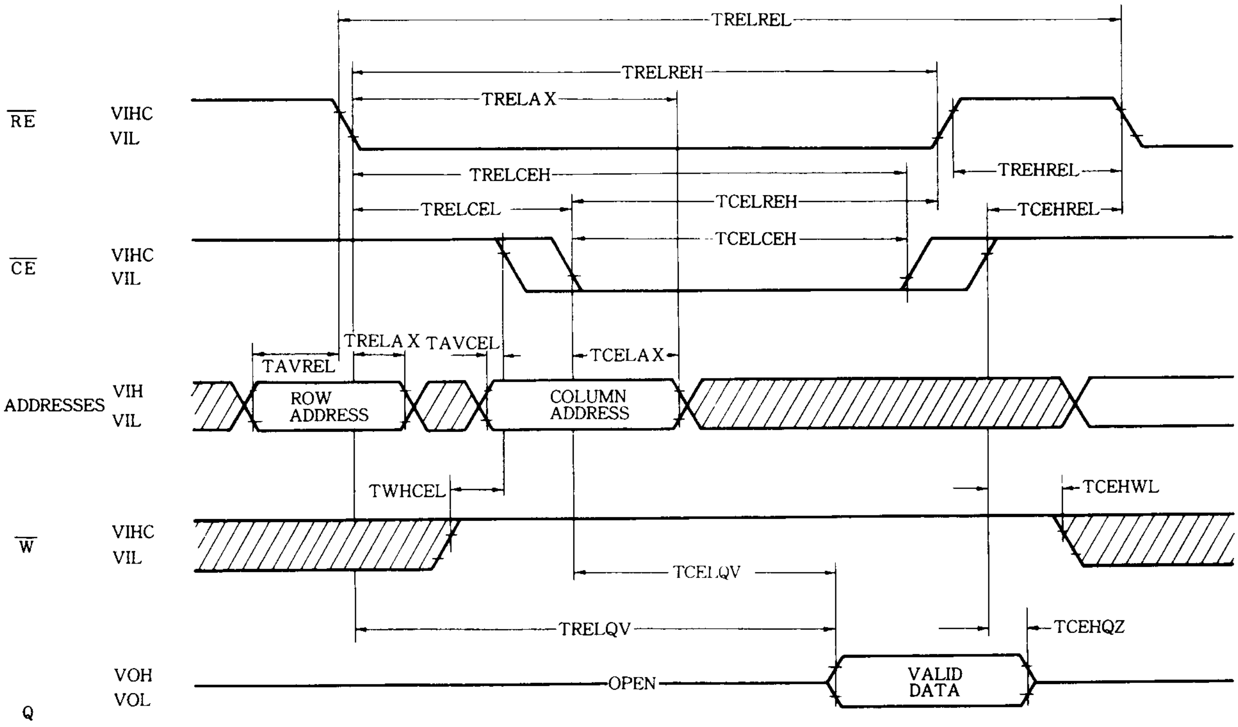
Parameter	Symbol		HM4716A-1		HM4716A-2		HM4716A-3		HM4716A-4		Units	Notes
	Old	New	min.	max.	min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	TRELREL	320	–	320	–	375	–	410	–	ns	
Read-Write Cycle Time	t_{RWC}	TRELREL	320	–	320	–	375	–	515	–	ns	
Page Mode Cycle Time	t_{PC}	TCELCEL	160	–	170	–	225	–	275	–	ns	
Access Time From $\overline{\text{RE}}$	t_{RAC}	TRELQV	–	120	–	150	–	200	–	250	ns	8, 10
Access Time From $\overline{\text{CE}}$	t_{CAC}	TCELQV	–	80	–	100	–	135	–	165	ns	9, 10
Output Buffer Turn-off Delay	t_{OFF}	TCEHQZ	0	35	0	50	0	60	0	70	ns	11
Transition Time (Rise and Fall)	t_{T}	TT	3	35	3	35	3	50	3	50	ns	7
$\overline{\text{RE}}$ Precharge Time	t_{RP}	TREHREL	100	–	100	–	120	–	150	–	ns	
$\overline{\text{RE}}$ Pulse Width	t_{RAS}	TRELREH	120	10000	150	10000	200	10000	250	10000	ns	
$\overline{\text{RE}}$ Hold Time	t_{RSH}	TCELREH	80	–	100	–	135	–	165	–	ns	
$\overline{\text{CE}}$ Pulse Width	t_{CAS}	TCELCEH	80	10000	100	10000	135	10000	165	10000	ns	
$\overline{\text{CE}}$ Hold Time	t_{CSH}	TRELCEH	120	–	150	–	200	–	250	–	ns	
$\overline{\text{RE}}$ to $\overline{\text{CE}}$ Delay Time	t_{RCD}	TRELCEL	15	40	25	50	30	65	40	85	ns	12
CE to RE Precharge Time	t_{CRP}	TCEHREL	0	–	−20	–	−20	–	−20	–	ns	
Row Address Set-up Time	t_{ASR}	TAVREL	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	TRELAX	15	–	20	–	25	–	35	–	ns	
Column Address Set-up Time	t_{ASC}	TAVCEL	−5	–	−5	–	−5	–	−5	–	ns	
Column Address Hold Time	t_{CAH}	TCELAX	40	–	45	–	55	–	75	–	ns	
Column Address Hold Time Reference to $\overline{\text{RE}}$	t_{AR}	TRELAX	80	–	95	–	120	–	160	–	ns	
Read Command Set-up Time	t_{RCS}	TWHCEL	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	TCEHWL	0	–	20	–	20	–	20	–	ns	
Write Command Hold Time	t_{WCH}	TCELWH	40	–	45	–	55	–	75	–	ns	
Write Command Hold Time Referenced $\overline{\text{RE}}$	t_{WCR}	TRELWH	80	–	95	–	120	–	160	–	ns	
Write Command Pulse Width	t_{WP}	TWLWH	40	–	45	–	55	–	75	–	ns	
Write Command to $\overline{\text{RE}}$ Lead Time	t_{RWL}	TWLREH	50	–	60	–	80	–	100	–	ns	
Write Command to $\overline{\text{CE}}$ Lead Time	t_{CWL}	TWLCEH	50	–	60	–	80	–	100	–	ns	
Data-in Set-up Time	t_{DS}	TDVCEL	0	–	0	–	0	–	0	–	ns	13
Data-in Hold Time	t_{DH}	TCELDX	40	–	45	–	55	–	75	–	ns	13
Data-in Hold Time Referenced $\overline{\text{RE}}$	t_{DHR}	TRELDX	80	–	95	–	120	–	160	–	ns	
$\overline{\text{CE}}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	TCEHCEL	60	–	60	–	80	–	100	–	ns	
Refresh Period	t_{REF}	TRVRV	–	2	–	2	–	2	–	2	ms	
$\overline{\text{W}}$ Command Set-up Time	t_{WCS}	TWLCEL	0	–	−20	–	−20	–	−20	–	ns	14
$\overline{\text{CE}}$ to $\overline{\text{RE}}$ Delay	t_{CWD}	TCELWL	60	–	70	–	95	–	125	–	ns	14
$\overline{\text{RE}}$ to $\overline{\text{W}}$ Delay	t_{RWD}	TRELWL	100	–	120	–	160	–	200	–	ns	14
$\overline{\text{RE}}$ Precharge to $\overline{\text{CE}}$ Hold Time	t_{RPC}	TREHCEL	0	–	0	–	0	–	0	–	ns	

■ AC ELECTRICAL CHARACTERISTICS

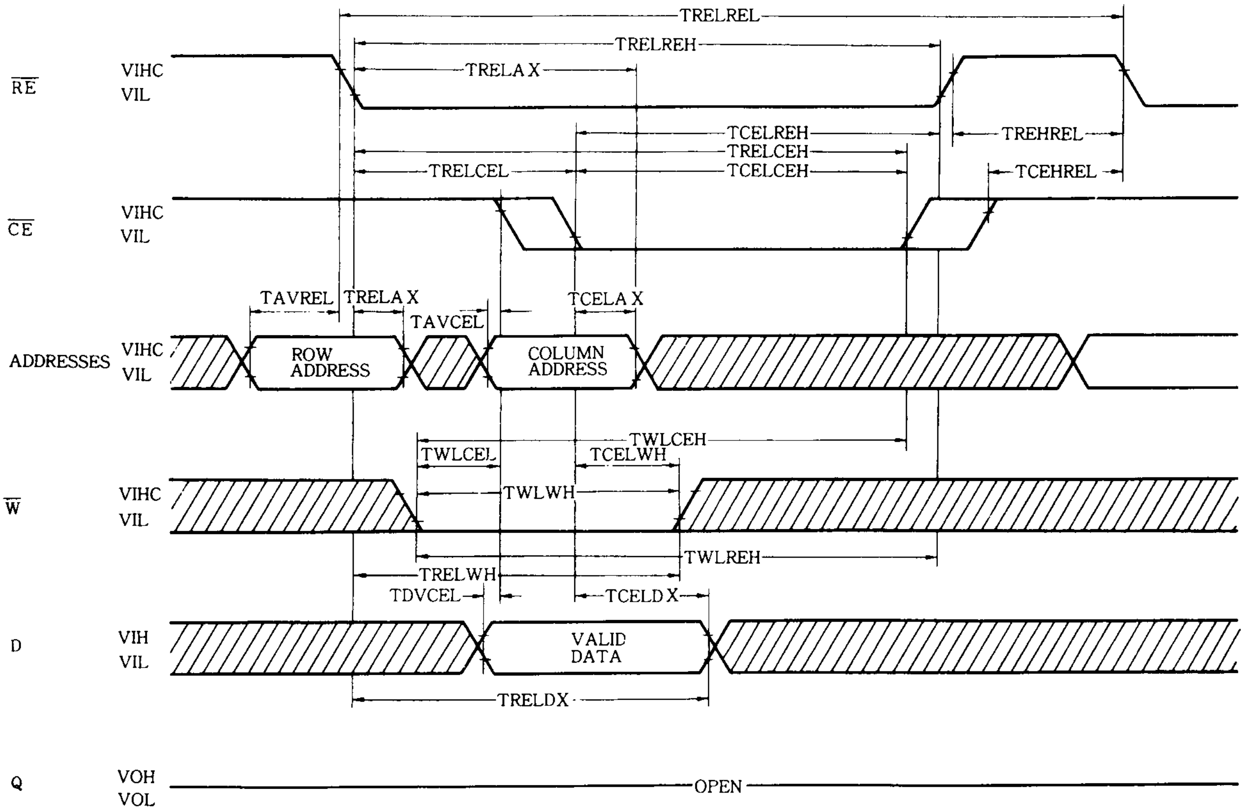
Parameter	Symbol	typ.	max.	Units	Notes
Input Capacitance (A0-A6, D)	CI1	–	5	pF	15
Input Capacitance $\overline{\text{RE}}$, $\overline{\text{CE}}$, $\overline{\text{W}}$	CI2	–	10	pF	15
Output Capacitance (Q)	CQ	–	7	pF	15, 16

■ TIMING WAVEFORMS

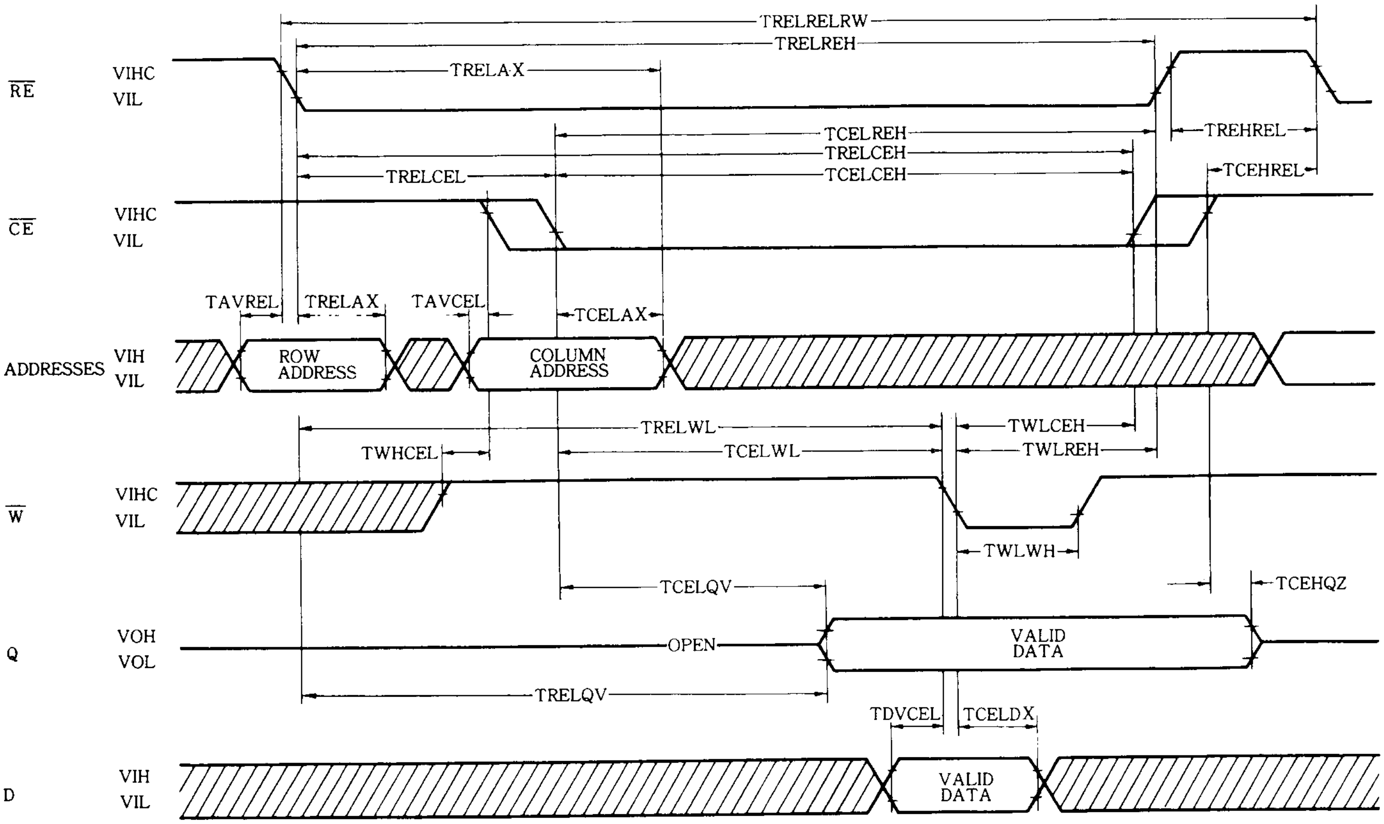
• READ CYCLE



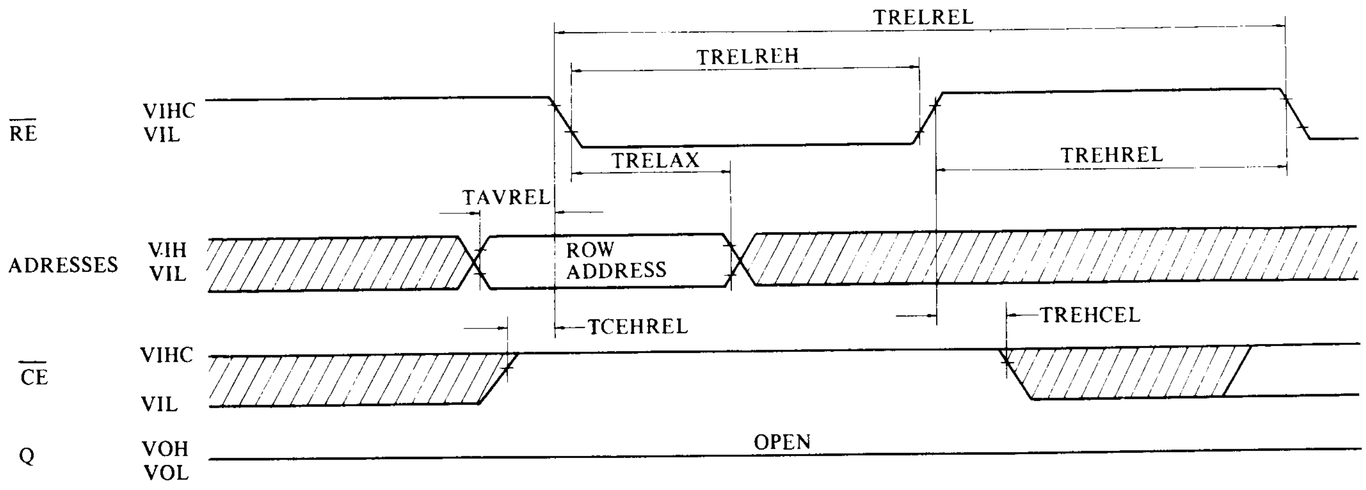
• WRITE CYCLE (EARLY WRITE)



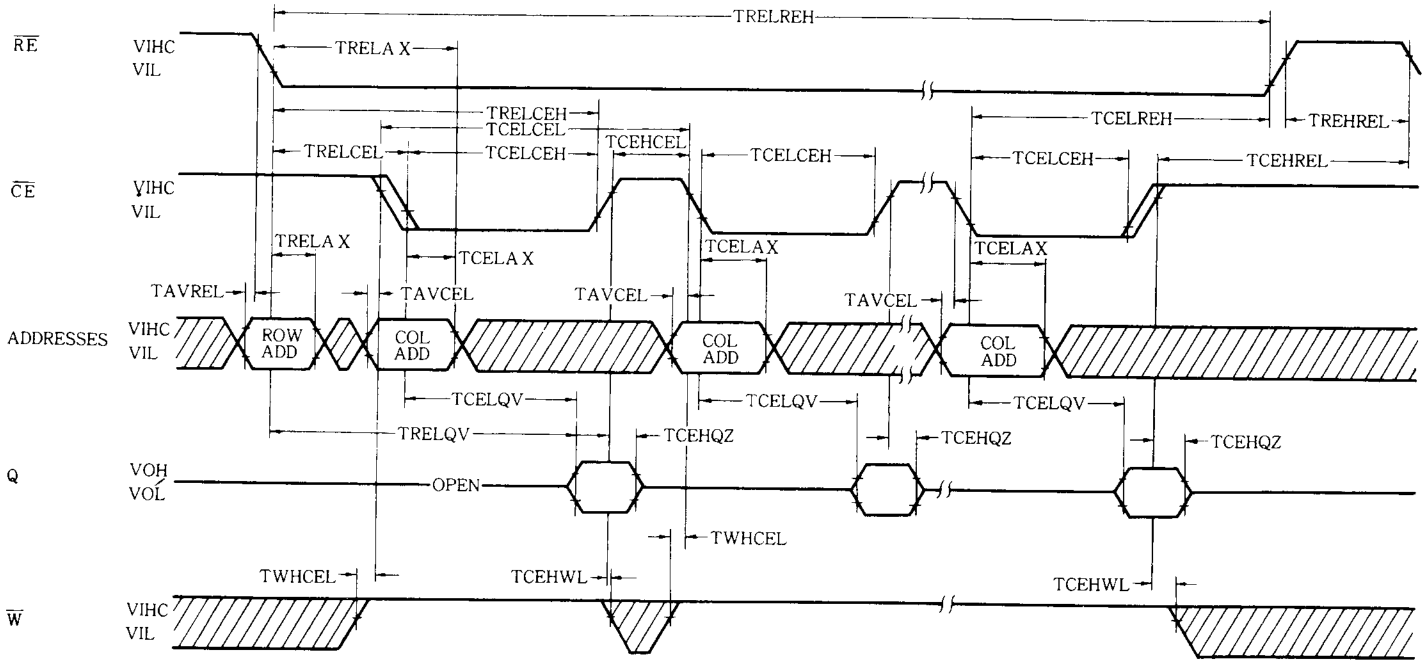
- **READ-WRITE/READ-MODIFY-WRITE CYCLE**



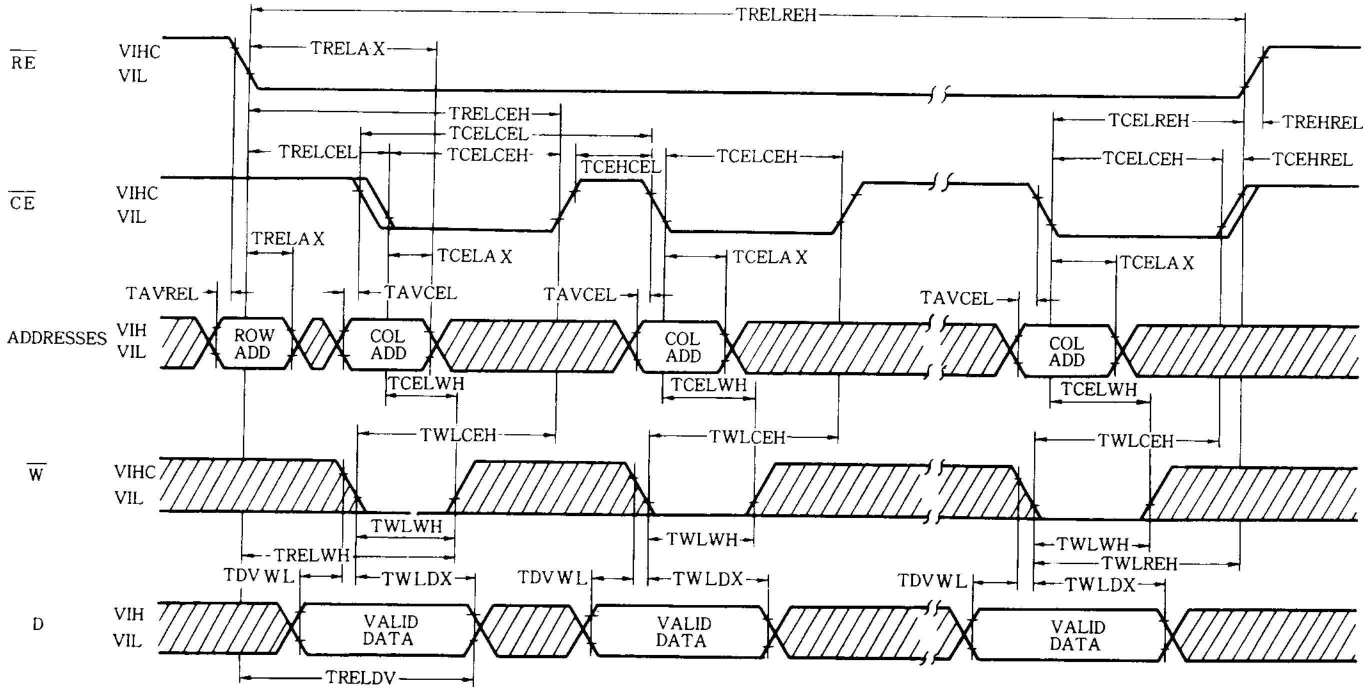
- **"RE ONLY" REFRESH CYCLE**



- **PAGE MODE READ CYCLE**

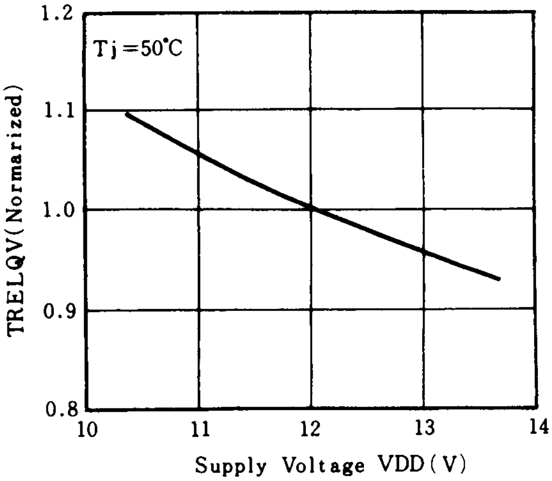


- **PAGE MODE WRITE CYCLE**

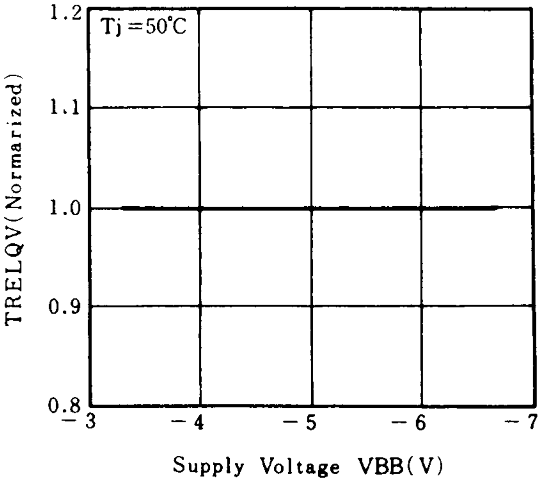


- **TYPICAL CHARACTERISTICS**

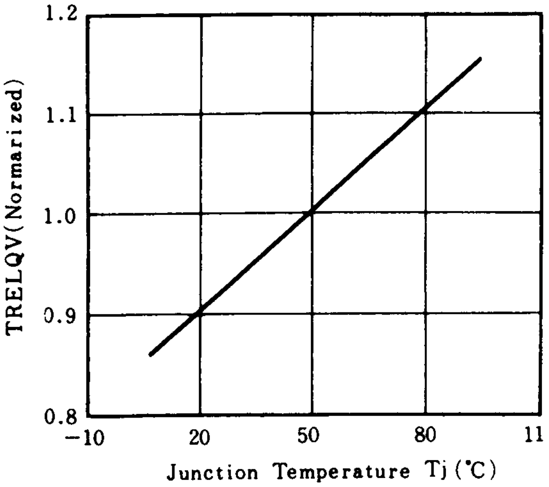
ACCESS TIME (NORMARIZED) vs. VDD



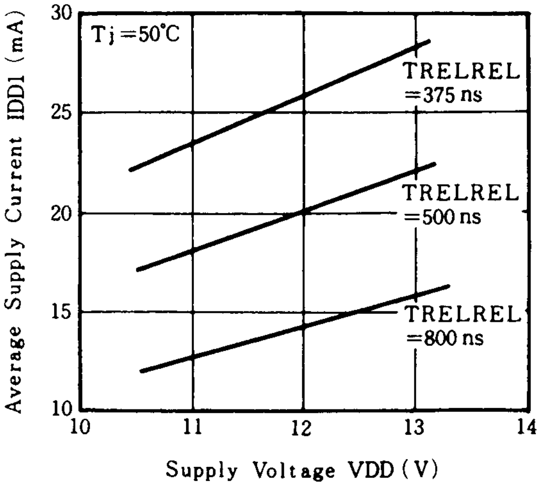
ACCESS TIME (NORMARIZED) vs. VBB



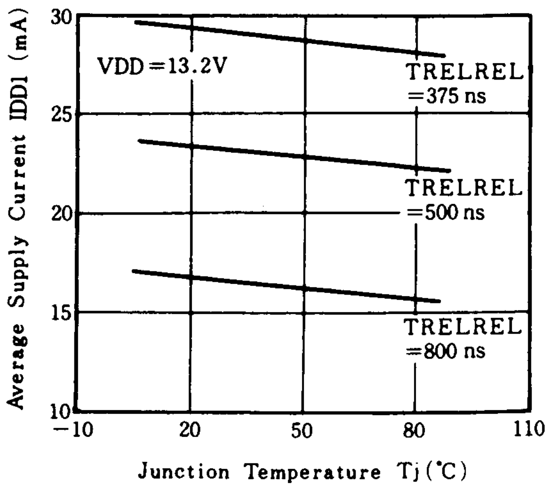
ACCESS TIME (NORMARIZED) vs. Tj



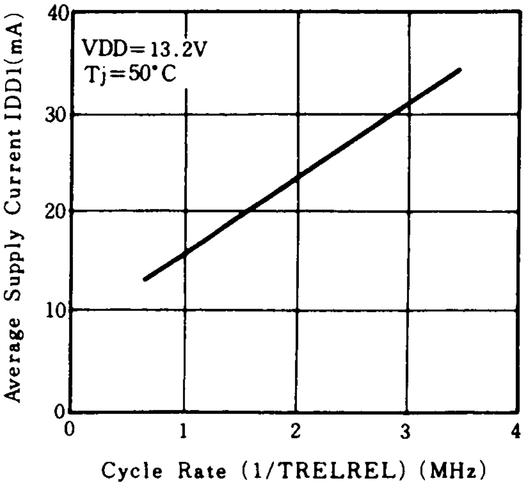
IDDI vs. VDD



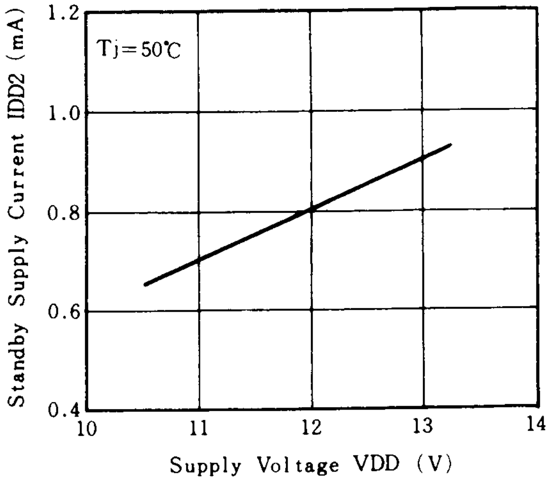
IDDI vs. Tj



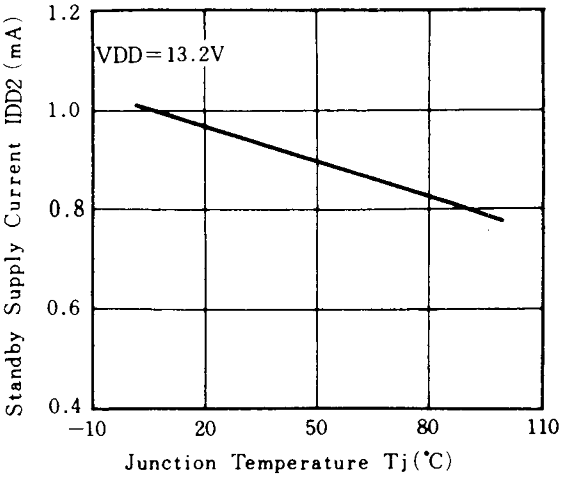
IDDI vs. CYCLE RATE



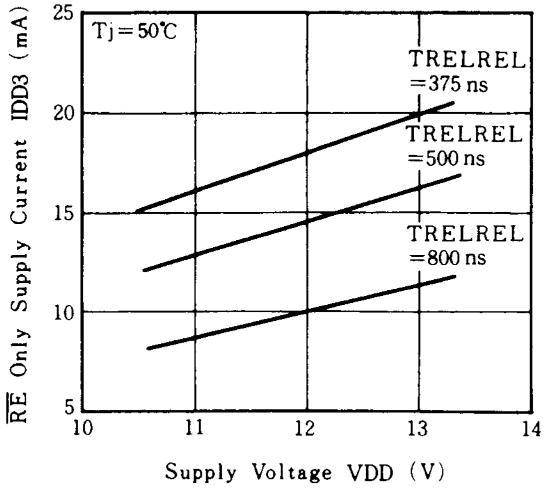
IDD2 (STANDBY) vs. VDD



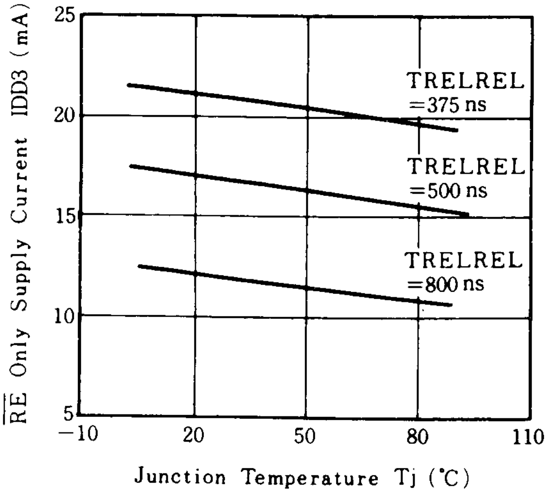
IDD2 (STANDBY) vs. Tj



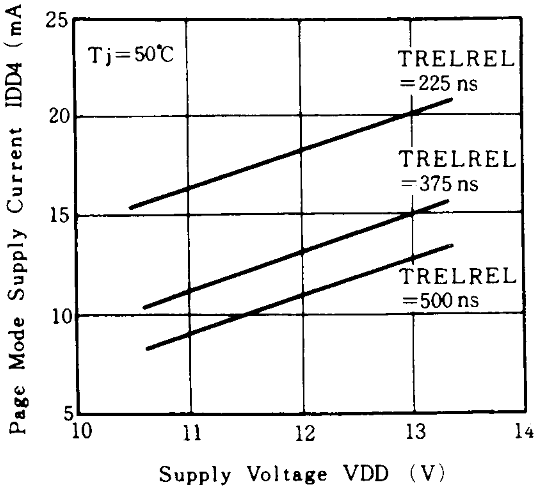
IDD3 ($\overline{\text{RE}}$ ONLY CYCLE) vs. VDD



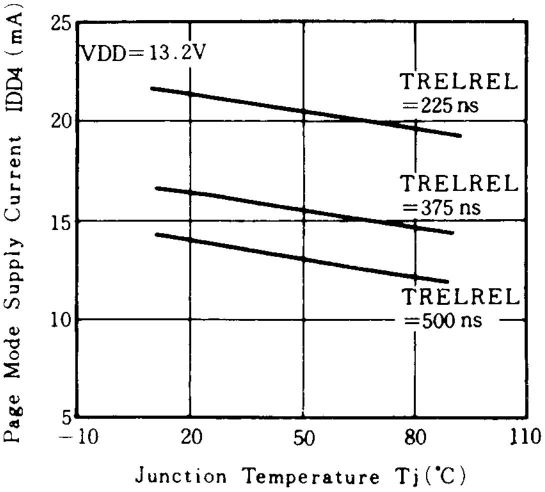
IDD3 ($\overline{\text{RE}}$ ONLY CYCLE) vs. Tj



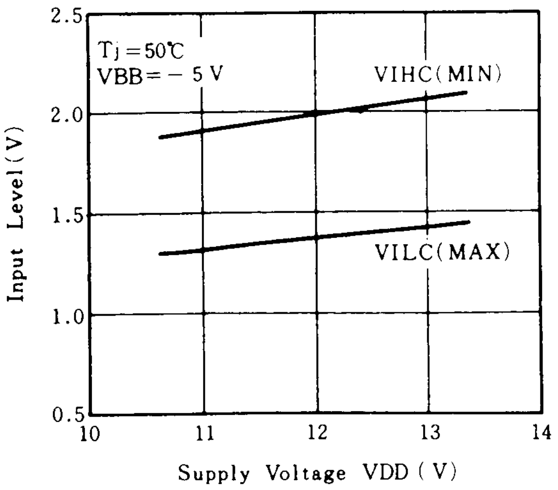
IDD4 (PAGE-MODE CYCLE) vs. VDD



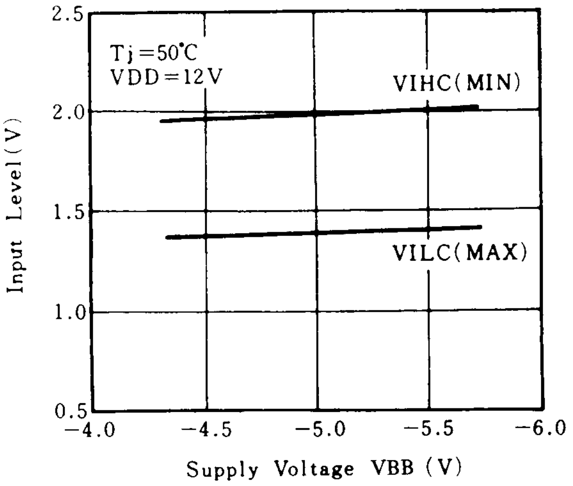
IDD4 (PAGE-MODE CYCLE) vs. Tj



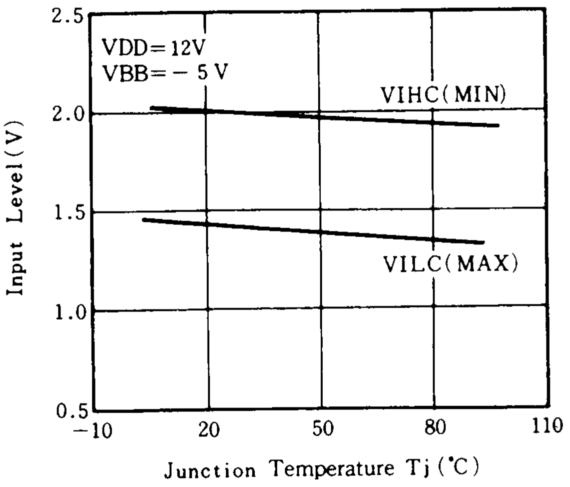
CLOCK INPUT LEVELS vs. VDD



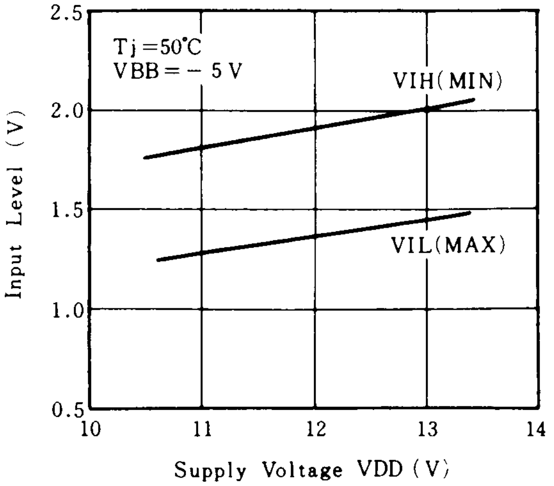
CLOCK INPUT LEVELS vs. VBB



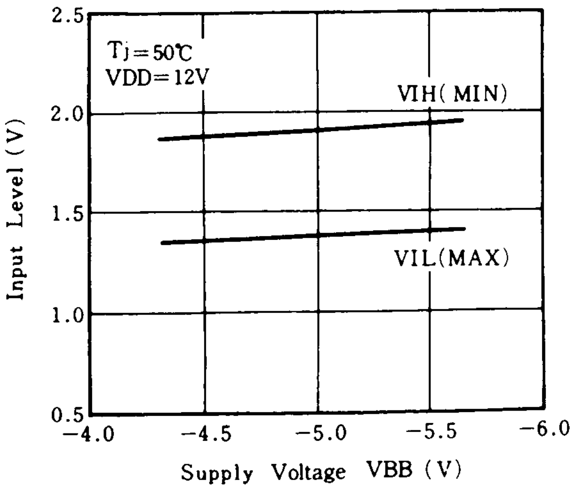
CLOCK INPUT LEVELS vs. Tj



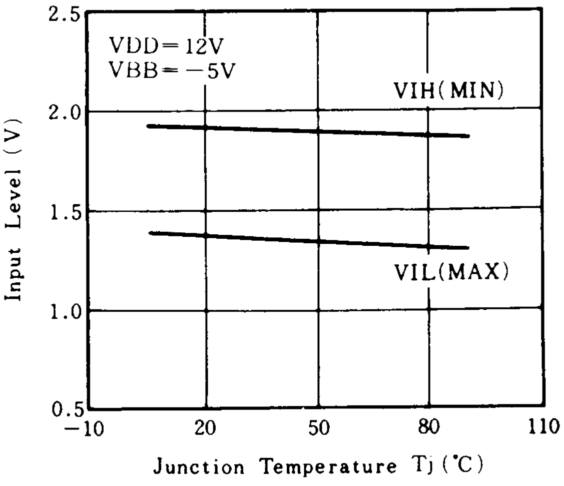
ADDRESS AND DATA INPUT LEVELS vs. VDD



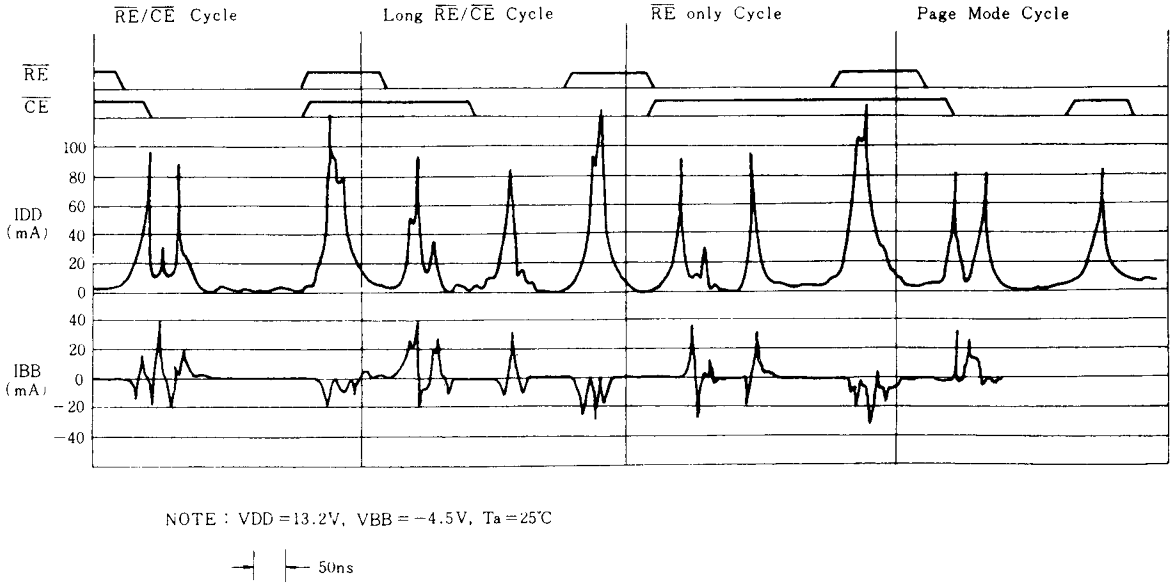
ADDRESS AND DATA INPUT LEVELS vs. VBB



ADDRESS AND DATA INPUT LEVELS vs. Tj



■ CURRENT WAVEFORMS



NOTE : VDD = 13.2V, VBB = −4.5V, Ta = 25°C

APPLICATION INFORMATION

● READ CYCLE;

A read cycle begins with addresses stable and a negative going transistion of $\overline{RE}$. The time delay between the stable address and the start of $\overline{RE}$-on is controlled by parameter TAVREL. Following the time when $\overline{RE}$ reaches its low level, the row address must be held stable long enough to be captured.

This controlling parameter is TRELAX. Following this interval, the address can be changed from row address to column address.

When the column address is stable, $\overline{CE}$ can be turned on.

The leading edge of $\overline{CE}$ is controlled by parameter TRELCEL. The basic limit on the $\overline{CE}$ leading edge is that $\overline{CE}$ cannot start untill the column address is stable, and this is controlled by parameter TAVCEL.

The column address must be held stable long enough to be captured.

The controlling parameter is TCELAX. Note that TRELCEL-(max) is not an operating limit of the HM4716A though its specification is listed on the data sheets. If $\overline{CE}$ becomes on later than TRELCEL(max), the access time from $\overline{RE}$ will be increased by the time which TRELCEL exceeds TRELCEL-(max).

Following the time when $\overline{CE}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is TCELQV-access time from $\overline{CE}$. The access time from $\overline{RE}$-TRELQV-is the time from $\overline{RE}$-on to valid Q. The minimum value of TRELQV is derived as the sum of TRELCEL(max) and TCELQV. The selected output data is held valid internally untill $\overline{CE}$ becomes high, and then Q pin becomes high impedance. This parameter is TCEHQZ.

● WRITE CYCLE;

A write cycle is performed by bringing $\overline{W}$ low before or during $\overline{CE}$-on.

Two different write cycles can be defined as;

Write cycle – Write data are available at the beginning of the $\overline{CE}$-on so that the write operationstarts at the beginning. In this mode, D and $\overline{W}$ signal times are not in any critical path for determining cycle time

Following the time when $\overline{W}$ reaches its low level. $\overline{W}$ must be held stable long enough to be captured. This $\overline{W}$-on pulse duration is called TWLWH.

The time required to capture write data in a latch is called TWLDX.

This cycle is called an "early write"

Read Write cycle – This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated. $\overline{W}$ and D are delayed until after Q. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, D and $\overline{W}$ become critical path signals for determining cycle time.

● CLOCK-OFF TIMING;

$\overline{RE}$ and $\overline{CE}$ must stay on for Q stabilized to valid data. In the case of $\overline{CE}$, this is controlled by parameaer TCELCEH(min). In the case of $\overline{RE}$, this controlled by parameter TCELREH(min). Following the end of $\overline{RE}$, $\overline{CE}$ must stay off long enough to precharge internal circuits. The only parameter of concern is TREHREL.

Normally $\overline{CE}$ is not required to be off for a minimum time of TCEHREL.

However, in a page mode memory operation, there is a TCEHCEL(min) specification to control the $\overline{CE}$-off time.

● DATA OUTPUT;

Q is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{CE}$ is high, Q is in a high impedance state. When $\overline{CE}$ is low, valid data appears after TCELQV at a read cycle, and Q is not valid at an early-write cycle.

● REFRESH;

Refresh of the HM4716A is accomplished by performing A memory cycle at each of the 128 row addresses within each two millisecond time interval.

Any cycle in which $\overline{RE}$ signal occurs refreshes the entire selected row.

$\overline{RE}$-only refresh results in substantial reduction in operating power.

This reduction in power is reflected in the IDD3 specification.

● PAGE MODE;

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining $\overline{RE}$ at a logic low throughout all successive $\overline{CE}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are reflected in the TCELQV, TCEHCEL, IDD4 specifications.