OMNI 800
electronic data terminals

Maintenance Manual

Model 810 Printer

994386-0001, Rev. J
May 1984

Volume I

TEXAS INSTRUMENTS

INSERT LATEST CHANGED PAGES, DESTROY SUPERSEDED PAGES

LIST OF EFFECTIVE PAGES

Model 810 Printer Maintenance Manual, Vol. I
Part No. 994386-0001
Original Issue: 15 July 1977
Revision J: May 1984

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CHANGE NOTICES

Revision Letter	Date	ECN		Description
		Number	Level	
A	3/15/78	432918	D	Update per ECN
B	6/1/78	432332	D	Update per ECN
C	10/9/78	439638	D	Update per ECN
D	11/15/79	444060	E	Update per ECN
E	10/10/80	469070	D	Update per ECN
F	9/22/81	443519	D	Update per ECN
G	10/28/81	492910	E	Update per ECN
H	4/16/82	443532	D	Update per ECN
J	5/1/84	498658	E	Update per ECN; incorporate into two volumes

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Preface

The *Model 810 Printer Maintenance Manual* consists of two volumes.

Volume I, this volume, provides detailed information for installing, operating, maintaining, and replacing assemblies and subassemblies of the Texas Instruments OMNI 800* Model 810 printer in Sections 1 through 8 and the Appendixes.

Volume II provides drawings, lists of materials, schematics, and logic diagrams in Sections 9 and 10.

SECTION 1. GENERAL DESCRIPTION — Provides a description of the Model 810 printer and lists the features and specifications.

SECTION 2. INSTALLATION — Specifies space and power requirements and provides step by step instructions for setting up the printer after it is unpacked.

SECTION 3. OPERATING INSTRUCTIONS (Manual Control) — Describes all control and indicator actions and lists specific operating procedures.

SECTION 4. OPERATING INSTRUCTIONS (Software Control) — Provides the programming material required to operate the printer through the communication line, with and without the line buffer option.

SECTION 5. INTERFACE INFORMATION (Printers Without Line Buffer Option) — Presents interface data such as signal criteria, cabling, and grounding connections for printers without the line buffer option.

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SECTION 6. INTERFACE INFORMATION (Printers With Line Buffer Option) — Provides interface data for printers equipped with the line buffer option.

SECTION 7. THEORY OF OPERATION — Contains the theory of operation including a system block diagram, a discussion of dot matrix printing, and an overview of the major printer subsystems.

SECTION 8. MAINTENANCE — Discusses recommended procedures for routine and preventive maintenance.

SECTION 9. ASSEMBLY DRAWINGS AND PARTS LISTS (Volume II) — Contains all engineering drawings and parts lists for the Model 810 printer.

SECTION 10. SCHEMATIC DIAGRAMS (Volume II) — Provides the logic diagrams and schematics for the printer.

APPENDIXES — Contain information useful for reference. Subjects covered are:

- A — Dot Matrix Character Generation
- B — ASCII Control and Character Codes
- C — Model 810 Printer Versions, Options, and Accessories
- D — TMS 8080A Microprocessor
- E — TMS 5501 I/O Controller
- F — Installation of Option Kits

- G — TMS 6011 Data Sheets
- H — Cable Pin Assignments
- I — U.S. ASCII/Katakana Dual Character Set
- J — Strappable Options for Processor and Line Buffer Boards
- K — Theory of Operation for Drive Board (TI Part No. 994322) and Power Supply (TI Part No. 994394)
- L — First-Generation Front Panels and Carriage Motor Assembly

The various options for the Model 810 printer are identified throughout this manual by configuration codes. For example, BSC indicates the basic printer. Options installed on the Model 810 printer can be determined by examining the printer configuration label on the underside of the access door for comparison to codes listed in Appendix C.

OTHER PUBLICATIONS

The following additional publications support the Model 810 printer.

- *Model 810 Printer Operator's Manual* (TI Part No. 994353-9701)
- *Model 810 Maintenance Manual — Volume II* (TI Part No. 994386-0002)

To order copies, send a company purchase request to:

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Section 1

General Description

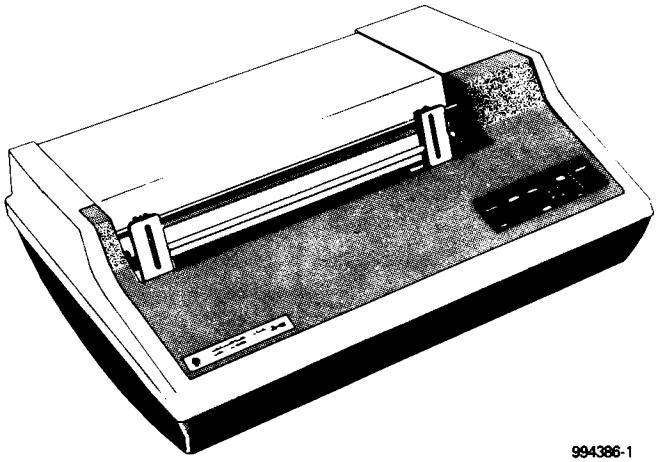
1.1 STANDARD FEATURES

The Texas Instruments *Omni 800* Model 810 printer is a receive-only, forms-programmable, impact printer. It features a microprocessor system which controls all character recognition, printing, and paper movement. Basic operating, data processing, and self-test routines for the microprocessor system are stored in read-only memory (ROM). Random-access memory (RAM) stores vertical format control routines which may be locally programmed by the operator or remotely programmed through the communications line.

A single seven-dot-column printhead produces the nine-by-seven dot matrix for character generation (see Appendix A). The 64-character, limited-ASCII, 95-character set (see Appendix A) and other character sets are available as options. Printing is bidirectional at the rate of 150 characters per second. A full 132-character line is printed in less than one second.

The standard print format is ten characters per inch (cpi) horizontally and six or eight lines per inch (lpi) vertically. Options are available to produce compressed printing (16.5 cpi) and/or expanded printing (five cpi). The printer produces one original and up to five copies using sprocket-fed paper in widths from 76.2 to 381 mm (3 to 15 in.).

In addition to the standard, serial EIA interface, a parallel (option code PLT) interface or a TTY/RS-422 interface is also available as an option. The Line Buffer option is available in three interface configurations: EIA (option code LBE), parallel (option code LBP), or TTY current loop (option code LBT).



994386-1

Figure 1-1. Model 810 Printer

1.2 CONFIGURATIONS

The Model 810 is available in five versions:

TI Part Number	Code	Version
994292-0001	BSC	Basic
994292-0002	FLC	Forms Length Control
994292-0003	VFC	Vertical Format Control
994293-0001	FCO	Forms Length Control, Compressed Print
994293-0002	VCO	Vertical Format Control, Compressed Print
2360013-0001	PKG	Package

Any options installed in your printer are listed on a label affixed to the underside of the access door. The options are identified by a three-letter configuration code.

1.3 SPECIFICATIONS

Standard features and specifications are listed in Table 1-1.

Table 1-1. Standard Model 810 Printer Characteristics and Specifications

Characteristic	Specification
PRINTING	
Technique	Seven-wire matrix, impact
Character matrix	9 × 7 (9 wide, 7 high) dot matrix
Character set	64-character limited ASCII
Characters per inch	10
Characters per line	132 maximum
Lines per inch	6 or 8 (operator—or software—selectable)
THROUGHPUT	
Print speed	150 characters per second
Lines per minute	64 at 132 characters per line, and up to 450 at 10 cpl
Line feed	33 milliseconds
Paper slew	170 mm per second (6.67 in/sec)
PAPER HANDLING	
Paper width	Adjustable from 76 to 381 mm (3 to 15 in.)
Paper loading	Rear or bottom feed
Number of copies	One original and five copies
CONTROL SYSTEM	
Electronics	8080 microprocessor system
Printing method	Bidirectional
Buffer (FIFO)	256 characters
Horizontal tabs	Software Programmable
Vertical format control	Software and operator programmable
Self-test	Prints ASCII characters in a rotating pattern (barberpole)
Bell	Pulsing audible tone

Characteristic	Specification
COMMUNICATIONS	
Interface	Serial (EIA RS-232-C)
Baud rates	110, 150, 300, 1200, 2400, 4800, 9600
Parity	ODD, EVEN or ignore
INPUT POWER	
ac voltage	100, 120, 220, or 240 Vac (+10% to −15%)
Frequency	48 to 62 Hz
Watts	200
Power fuse	100 or 120 Vac range, 5 A, 250 V fuse 220 or 240 Vac range, 2.5 A, 250 V fuse
ENVIRONMENTAL	
Mounting	Table top
Operating temperature	+5°C (+37°F) to +40°C (+104°F)*
Storage temperature	−30°C (−22°F) to +70°C (+158°F)
Operating humidity	10% to 90% (no condensation)
Storage humidity	5% to 95% (no condensation)
PHYSICAL	
Weight	25 kg (55 pounds)
Height	203 mm (8 inches)
Width	654 mm (25.75 inches)
Depth	508 mm (20 inches)

*Up to 2134 m (7000 feet) MSL. Derate linearly to 25°C (+77°F) at 3048 m (10,000 feet) MSL.

1.4 MODIFIABLE FEATURES

The following standard operating option is easily modified in the field on the standard Model 810 printer. See Appendix F for jumper configuration.

- Signal and safety ground isolation by a capacitor (ISC option).

The following standard operating options are easily modified in the field on the standard Model 810 printer without the Line Buffer option. See Appendix F for jumper configurations.

- Enable or disable recognition of DEL character (NDE option)
- BUSY or NOT BUSY on DTR line (DNB option)
- Inverted reverse channel (IRC option) signal
- Enable or disable recognition of DC1-DC3 characters (DCO option).

The following standard operating options are easily modified in the field on the standard Model 810 printer with the Line Buffer option. See Appendix F for jumper configurations.

- BUSY or NOT BUSY on the DTR line (DNB option)
- Inverted reverse channel signal (IRC option)
- Enable or disable gated EIA data (GED option)
- Enable or disable half-duplex operation (HDP option)
- Enable or disable carriage return detect (DSC option)
- Enable or disable gated data strobe (GDS option)
- Enable or disable recognition of DC1-DC3 characters (DCO option).

1.5 OPTIONAL FEATURES

The following character sets* and optional features (identified by configuration code in parentheses) are available for the Model 810 printer:

- Full U.S. ASCII 95-character set (FUL)
- Full U.S. ASCII/Katakana dual-character set (KAT, KTS)
- European (DNF, DNL, SWF, SWL, UKF, or UKL) and other character sets
- Parallel interface (PLT)
- TTY, 20-mA, neutral current loop (TTY)
- Line Buffer option PC board, EIA interface (LBE)
- Line Buffer option PC board, parallel interface (LBP)
- Line Buffer option PC Board, with TTY, 20-mA, neutral current loop (LBT)
- Selectable form lengths (FCO or FLC)
- Vertical Format Control, nonvolatile eight-channel memory (VCO or VFC)
- Compressed Print, 16.5 cpi (FCO or VCO)
- Expanded Print option (EXP) prints five cpi and 8.25 cpi.The EXP option is available only with the standard 64-character ASCII character set. The 8.25 cpi option is available on FCO and VCO printers only.
- Nine-copy printhead—nine copies can be printed.

1.6 ACCESSORIES

The following accessories are available for use

*Only one character set option may be specified in the Model 810 printer.

with the Model 810 printer:

- Tear bar
- Paper baskets for terminal or floor stand
- Floor-mounting stand
- Interface cables (see cabling information in Section 5 or 6 and Appendix H).

Section 2

Installation

2.1 INTRODUCTION

This section provides information for selecting the installation site, unpacking and setting up the printer, and ensuring that the printer is operating properly. Communications line connections to the Model 810 printer are described in Sections 5 and 6 of this manual.

2.2 SPACE REQUIREMENTS

The printer should be located to allow easy access to the operator controls and printed output. If the optional floor stand is not used, a sturdy table capable of supporting 25 kg (55 lbs.) is considered suitable.

The printer occupies a flat surface area 654 mm (25.75 in.) wide by 584 mm (23 in.) deep, including a cable clearance of 76 mm (3 in.). See Figure 2-1 for visual dimensions.

Regardless of the supporting device, care must be taken to ensure that neither the weight of the printer nor other types of pressure are exerted on the paper chute which could deform it. Additionally, an unobstructed paper feed path below or behind the printer must be provided. If the paper basket accessory is not selected, some method of holding the printed output must be devised.

Besides the correct support, a necessary consideration is to provide adequate ventilation. The printer requires approximately 50 mm (2 in.) for proper ventilation. Particular attention should be paid to ensure that the sides which contain both the intake fans and exhaust louvers are clear.

No printing device should be operated in an environment of excessive humidity.

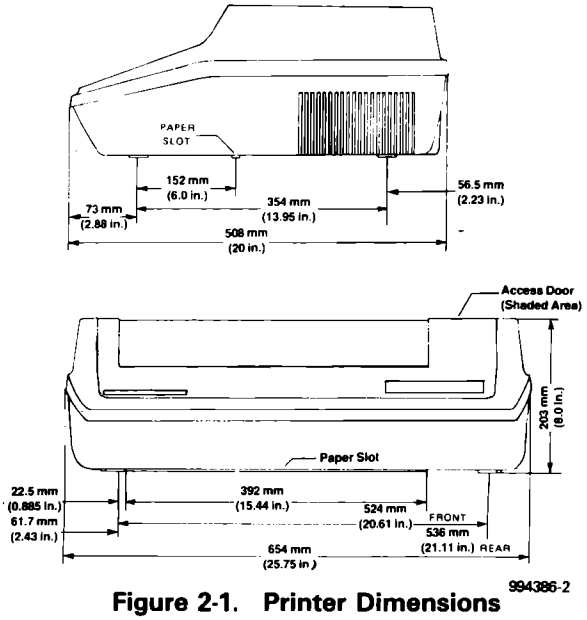


Figure 2-1. Printer Dimensions

2.3 UNPACKING AND SETTING UP

Remove the printer from its shipping carton and place it in its intended operating location. Follow steps 1 through 9 below.

1. Examine the shipping carton for damage. Note the nature of the damage (if any) and follow local procedures for reporting damaged shipments to the carrier that delivered your terminal.

2. Place the shipping carton on the floor and open the top flaps.

3. Remove the loose items and set them aside.

4. Two persons should grip the printer close to each end, lift the printer from the shipping carton, and place it on a table or on the optional terminal stand.

5. Remove the plastic bag containing supplies from the shipping carton.

6. Lift open the access door (see Figure 2-1) and remove the cardboard printhead retainer. To open the access door, grip the slightly recessed area below the control panel and pull up. (It is not labeled.) Older models do not have the recess but are opened the same way.

7. Manually slide the printhead from stop to stop. Ensure that the printhead and its attached wire rope move freely and that the wire rope is not unstrung.

8. Close the access door.

9. If applicable, the printer should be secured to the accessory floor-mounting stand. Follow the installation instructions furnished with the stand. *If the printer is mounted on a metallic surface, the printer must be grounded to that surface for correct operation.*

2.4 PAPER BASKET INSTALLATION

Accessory paper baskets for the Model 810 printer are available in two versions. One basket attaches to the rear of the printer. The other basket attaches to the terminal stand. *If any other paper-holding device is used, it must be grounded to the printer for correct operation.*

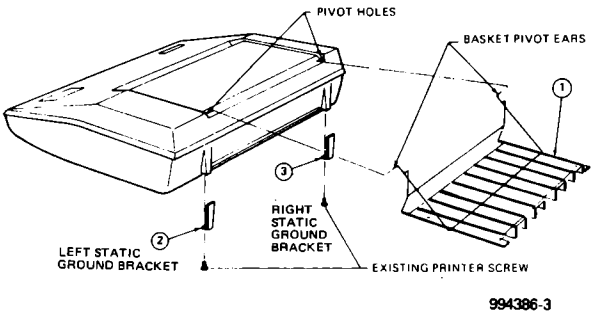
2.4.1 Terminal Paper Basket

The paper basket kit (TI Part No. 994442-0001) is installed on the Model 810 printer as follows (see Figure 2-2):

1. Using a ¼-inch nutdriver or wrench, remove the two screws which attach the rear paper chute to the printer.

2. Attach the left and right static ground brackets to the printer, using the two screws removed in *step* 1. *The static ground brackets are essential for correct printer operation. They are factory installed on all units manufactured after January 1, 1981.*

3. Attach the basket to the printer by slightly compressing inward the basket pivot ears, and insert the ears into the existing pivot holes at the rear of the printer cover.



1. PAPER BASKET
2. BRACKET, LEFT—STATIC GROUND
3. BRACKET, RIGHT—STATIC GROUND

Figure 2-2. Terminal Paper Basket Installation

2.4.2 Terminal Stand Paper Basket

This basket is used with Model 810 printers mounted on the accessory terminal stand (TI Part No. 999841-0001). To install this kit (TI Part No. 999839-0001), proceed as follows (see Figure 2-3):

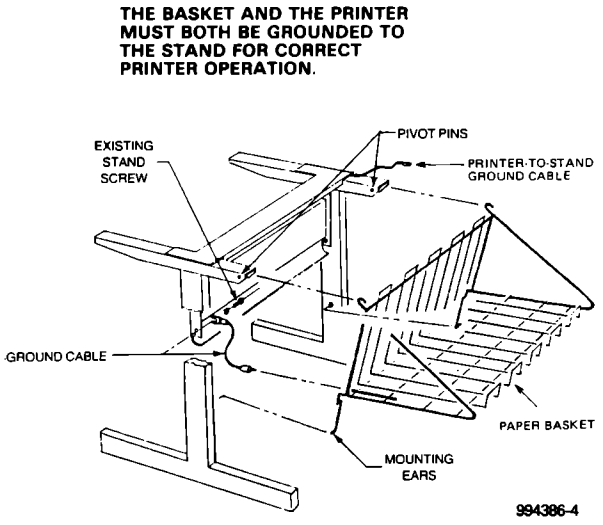


Figure 2-3. Stand Paper Basket Installation

1. Using a ¼-inch nutdriver or wrench, remove the existing screw from the stand.

2. Attach the static ground cable lug (furnished in the basket kit) to the stand using the screw removed in *step* 1.

3. Attach the paper basket to the stand by hooking the basket onto the pivot pins at the rear. Then rotate the basket downward, slightly compress the basket mounting ears, and insert them into the holes provided on the inside of the legs.

4. Connect the ground cable banana plug into the tube provided on the basket.

5. Make sure that the printer-to-stand ground cable (furnished in the accessory terminal stand kit, TI Part No. 999841-0001, is properly installed.

2.5 CONNECTING POWER

2.5.1 Grounding Requirements

The Model 810 is supplied with a 1.8 meter (six-foot) three-conductor power cord. Install the terminal near a three-prong grounding wall receptacle which is capable of accommodating the three-conductor plug on the power cord. If an extension cord must be used, it must also be the three-wire grounding type.

WARNING

Do not use a receptacle that will not accommodate the three-conductor plug. Do not cut the grounding prong from the plug. An electrical shock hazard may result.

For your personal safety and correct operation, this terminal must be grounded by plugging the power cord into a three-prong receptacle, grounded in accordance with the National Electrical Code and local codes and ordinances. Any of the following conditions can pose a possible safety hazard or result in terminal malfunction.

- Open safety ground or ground impedance greater than 1 ohm
- Safety ground connected to neutral anywhere other than the service entrance
- Safety ground connected to conduit or water pipe
- Hot and neutral connections reversed in receptacle (100 V, 120 V systems)

If a properly wired wall receptacle is not available, it is the user's responsibility and obligation to have such a receptacle installed by a qualified electrician.

For satisfactory operation, it is recommended that the printer not be installed on the same ac branch circuit with copying machines, water coolers, or similar appliances which produce power-line transients. If malfunctions occur as a result of such devices, it is the user's responsibility to relocate the printer to a different circuit or to install appropriate transient-suppression devices.

2.5.2 Line Voltage Selection

The standard 810 printer operates on any of four line voltage ranges: 100, 120, 220, or 240 Vac. To adapt the printer to one of these voltages, refer to Figure 2-4 and proceed as follows:

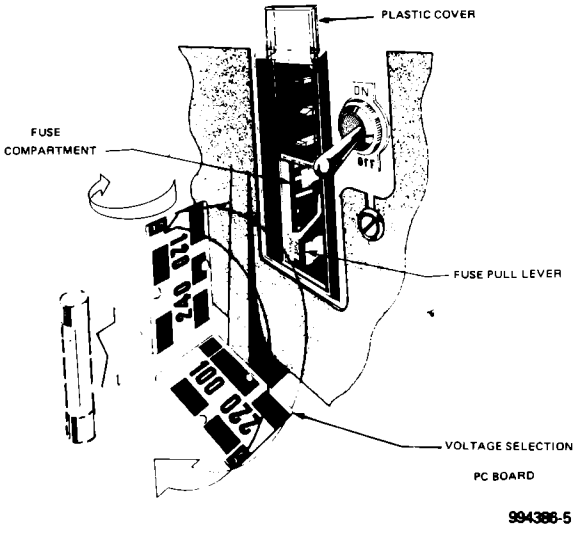


Figure 2-4. Line Voltage Selection

CAUTION

To prevent possible damage to the printer, do not switch power on until the correct line voltage is selected. Make a voltmeter check between logic/safety ground of the Model 810 printer and the equipment interfaces to the Model 810 printer. For large ground potential differences or faults from ac "hot" to logic/safety, grounds should be made before connecting the communications cable.

1. Check the ac line voltage at the power receptacle.

2. At the rear of the printer, disconnect the power cord and slide the clear plastic cover up to gain access to the fuse compartment.

3. Remove the line fuse by pulling outward and upward on the FUSE PULL lever.

4. Rotate the FUSE PULL lever fully upward and use a ball-point pen or similar device to remove the small printed circuit board (PCB).

5. Select the operating voltage to match available power (line voltage must be within +10% to −15% of the voltage selected).

6. Orient the small PCB so that the selected voltage marking is at the top and faces the fuse area.

7. Push the PCB firmly into its slot (only the selected voltage marking should be visible after the PCB is installed).

8. Push the FUSE PULL lever down, select the correct fuse from the following table, and place the fuse in the fuse holder.

Voltage Range	Fuse Type	TI Part Number
100 or 120 V	5.0 ampere, 250V	416434-0503
220 or 240 V	2.5 ampere, 250V	416434-0004

CAUTION

To prevent possible damage to the printer, be sure to use the correct fuse value for the voltage available.

9. Slide the clear plastic cover down.

10. Check that the ON/OFF switch is in the OFF position (down).

11. Connect the power cord to the Model 810 connector and then to the power source receptacle.

2.6 RIBBON INSTALLATION

The Model 810 printer uses a 13-mm (0.5-in.) wide nylon ribbon (TI Part No. 996241-0001 or equivalent) mounted on two 82.5-mm (3.75-in.) spools. To install the ribbon, refer to Figure 2-5 and proceed as follows:

1. Make sure the power switch (at left rear of printer) is set to OFF (down).

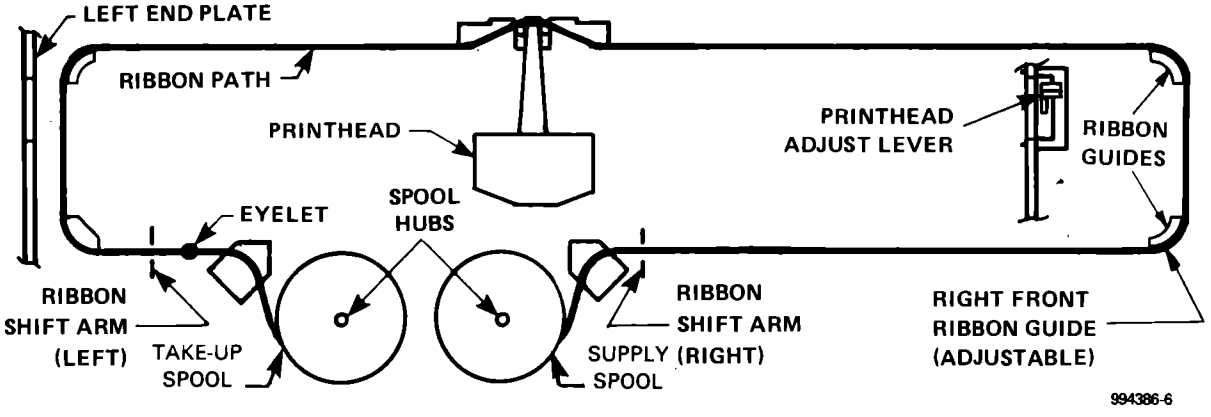


Figure 2-5. Ribbon Installation

2. Lift open the access door.

3. Ensure the new ribbon is attached to both spools (supply and takeup spools).

4. If the original printhead clearance is to be maintained, note the position of the printhead adjust lever. To move the printhead away from the platen, move the printhead adjust lever slightly to the right and toward the front of the printer.

5. Place the empty spool on the left spool hub with the feed-out side toward the front of the printer. Feed the ribbon out along the ribbon path as shown in Figure 2-5.

NOTE

Ensure that the ribbon-reversing eyelet is located between the left ribbon shift arm and the left spool hub; otherwise, the ribbon will not reverse. Also ensure that the ribbon is inside the left side plate (to prevent drag on the ribbon).

6. Place the full supply spool on the right spool hub and rotate the hubs as necessary to remove slack.

7. Be sure that the ribbon is centered in the slot on the right ribbon shift arm. If the ribbon is not centered, refer to Section 8 for adjustment procedures.

8. If the original printhead clearance is desired, return the printhead adjust lever to the position noted in *step* 4. Otherwise, perform the printhead adjustment procedure outlined in Section 3.

2.7 PAPER LOADING

The 810 printer uses continuous form paper with standard perforations on both sides. Paper widths from 76.2 to 381 mm (3 to 15 in.) can be accommodated. Using either the rear chute or bottom chute (see Figure 2-6), multiple-part forms (one original and up to five copies) with the following weight specifications can be used with the Model 810 printer:

Single-Part Forms:	15 to 20 pounds
Multiple-Part Forms:	Original: 12 to 15 pounds Copies: 9 to 12 pounds, last copy 15 pounds
Carbon Paper:	7½ pounds with medium hardness

Card stock up to 0.178 mm (0.007 in.) thick can be used as a single part or as last copy only when using the bottom chute. In any case, total form thickness should not exceed 0.533 mm (0.021 in.). The rear chute is recommended for single part forms only, although some multiple-part forms can be fed from the rear. To load paper in the printer, refer to Figure 2-6 and proceed as follows:

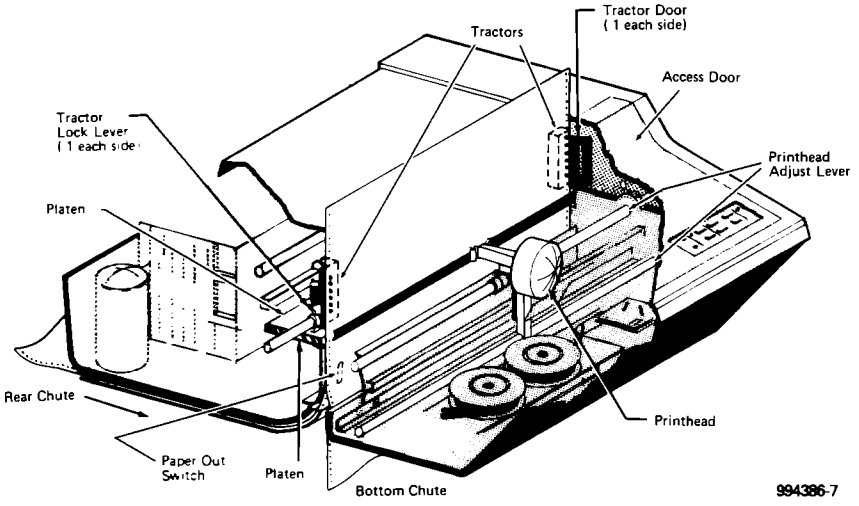


Figure 2-6. Paper Loading

NOTE

It is not necessary to switch power off when loading paper.

CAUTION

All metallic parts in the paper supply and take-up system must be grounded to the printer for correct operation.

1. Lift open the access door.

2. If the left feed tractor is not locked in the desired position (normally at the extreme left margin), loosen the lock lever and adjust the left tractor to the desired position. Tighten the lock lever.

3. Open the doors on both paper feed tractors.

4. Using the printhead adjust lever, move the printhead *away* from the platen.

5. Load paper through the **rear chute** as follows (or proceed to *step* 6 for bottom loading):

   a. Place the paper supply behind the printer.

NOTE

If the Model 810 printer is mounted on a table and the paper supply is placed on the floor, be sure the rear edge of the printer is located slightly past the edge of the table top so the paper can feed freely into the printer.

   b. Feed paper, printing side down, into the paper chute at the rear of the printer until paper appears at the platen.

   c. Proceed to *step* 7.

6. Load paper through the **bottom chute** as follows:

   a. Align the Model 810 printer bottom chute with the slot in the table or stand.

   b. Place the paper supply under the table or stand. Align the paper path to prevent paper edges from rubbing against the table slot or the ends of the bottom chute.

   c. Feed paper, printing side forward, into the bottom chute until paper appears at the platen.

7. Loosen the lock lever on the right tractor. Adjust to accommodate the paper width.

CAUTION

To prevent possible damage to the printhead, do not operate the printer without a ribbon or with paper too narrow for the printed line width. If the full 132-column line is used, the paper must be at least 378 mm (14-7/8 inches) wide for the standard 10 cpi spacing and at least 216 mm (8-1/2 in.) wide for the optional (FCO and VCO printers only) 16.5 cpi compressed print spacing.

8. Place the top of the paper in both tractors and make sure that the paper perforations engage in the corresponding tractor pins.

9. Close the tractor doors. Adjust the right tractor to remove slack in the paper and tighten the lock lever.

10. Ensure that the paper supply is aligned with the paper chute (paper must not rub the sides of the chute) and the PAPER OUT switch (Figure 2-6) is actuated.

11. Reset the printhead adjust lever and close the access door.

NOTE

Before placing your Model 810 printer into service, study the **Operating Instructions** in Section 3 of this manual.

Section 3

Operating Instructions (Manual Control)

3.1 INTRODUCTION

All operator controls and indicators on the Model 810 printer are located on the control panel (partially located under the access door) except for the *power ON/OFF switch and the printhead adjust lever.*

Figure 3-1 illustrates the location of the operator controls and indicators. The power ON/OFF switch is located on the left rear corner of the printer and the printhead adjust lever is located on the right side under the access door.

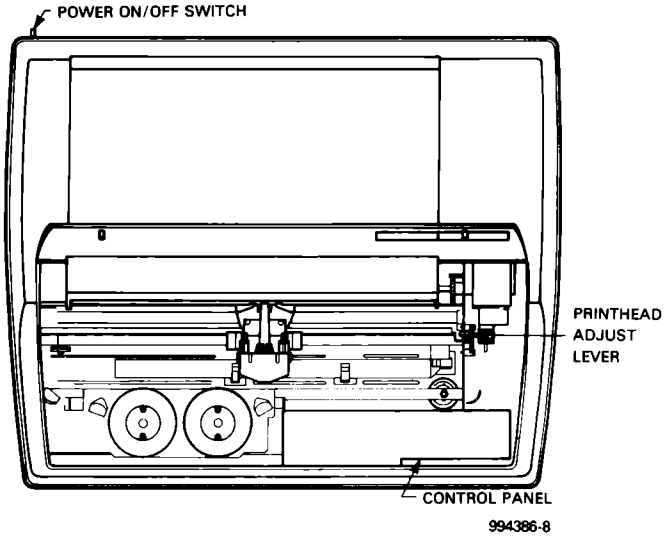


Figure 3-1. Model 810 Printer Operator Controls

3.2 OPERATOR CONTROLS AND INDICATORS

The control panel provides five switches, each of which has an alternate function (marked in red) in the vertical format programming mode. These alternate functions are active only when the printer is placed in the TEST/VFC mode by pressing the TEST/VFC switch on the auxiliary control panel. Figure 3-2 shows the layout of the control panel.

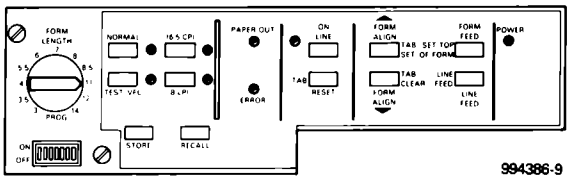


Figure 3-2. Model 810 Printer Control Panel

3.2.1 PAPER-OUT Indicator

This indicator glows steadily when activated by a paper-out condition. The audible tone (bell) also beeps five times. The paper-out indicator is cleared when paper is loaded and the RESET switch is pressed.

3.2.2 ERROR Indicator

The ERROR indicator has two functions:

- It glows steadily when a parity error is detected. (A special parity error symbol "◆" is also printed.)
- The indicator blinks for a printhead carriage fault. This fault is usually caused by the microprocessor losing encoder pulses. Power to the printhead carriage motor is switched off and the audible tone (bell) beeps five times.

The ERROR indicator is cleared by pressing the RESET switch.

3.2.3 ONLINE Switch and Indicator

Pressing this switch places the printer ONLINE and causes the ONLINE indicator to light. The ONLINE condition permits the printer to receive data from the communications line. The printer may also go ONLINE through receipt of the remote ASCII control code, DC1 (this code automatically returns the printhead to the left margin).

Pressing the switch a second time takes the printer OFFLINE. In this state, the printer goes busy in relation to the communications line but retains the data in the buffer. A DC3 command issued from a remote device can place the printer OFFLINE (this also causes the printhead to return to the left margin).

3.2.4 RESET/TAB Switch

If the problem has been corrected, the RESET function of this switch clears the paper-out condition or either of the two error conditions (see **ERROR Indicator**). The printhead realigns after a carriage fault condition is cleared.

The alternate TAB function of this switch is active only in the *vertical format control mode.** When active, pressing the switch advances the paper to the next preset vertical tab.

3.2.5 FORM ALIGN▲/TAB SET Switch

The normal FORM ALIGN▲ function of this pushbutton switch causes the paper to move up 0.355 mm (0.014 in.). If the switch is pressed and held, three small steps occur. Then, to accelerate paper movement, full line feeds are executed. This switch is active when the printer is ONLINE or OFFLINE.

The alternate TAB SET function of this switch is active only in the *vertical format control mode.** When active, pressing the switch *sets* a vertical tab at the present line.

3.2.6 FORM ALIGN▼/TAB CLEAR Switch

The normal FORM ALIGN▼ function of this pushbutton switch causes the paper to move down 0.355 mm (0.014 in.). If the switch is pressed and held, paper continues to move down in small increments. The switch is active when the printer is ONLINE or OFFLINE.

* To operate in this mode (Vertical Format Control) press the TEST/VFC switch on the auxiliary control panel.

The alternate TAB CLEAR function of this switch is active only in the *vertical format control mode.** When active, pressing the switch *clears* the vertical tab at the present line.

3.2.7 FORM FEED/SET TOP OF FORM Switch

The normal FORM FEED function of this pushbutton switch causes the paper to move to the preset top of the next form. Contents of the line buffer are printed before paper motion occurs. This switch is active when the printer is OFFLINE or ONLINE.

The alternate SET TOP OF FORM function of this switch is active only in the *vertical format control mode.** When active, pressing the switch sets the top of form (or "reads" the FORM LENGTH switch setting from the auxiliary control panel, if this option is installed in your printer).

3.2.8 LINE FEED/LINE FEED Switch

Each time this pushbutton switch is pressed, the paper moves up one line (twelve steps for six lines per inch and nine steps for eight lines per inch). If the line buffer is not empty, its contents are printed before paper motion occurs. This switch is active only OFFLINE. The normal and alternate functions of the switch are identical.

3.2.9 POWER Indicator

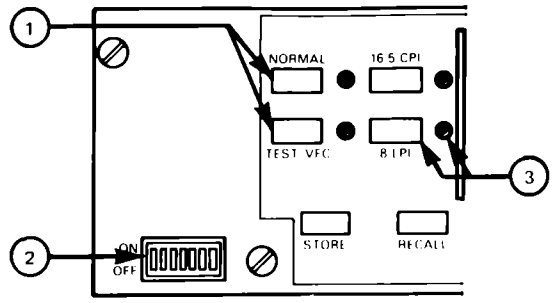
The POWER indicator lights when power is applied to the printer and the five-volt supply activates.

3.3 AUXILIARY CONTROLS AND INDICATORS

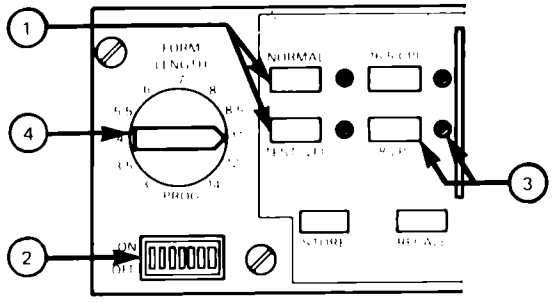
Model 810 printer versions are identified by the configuration codes listed in Table 3-1. The code also identifies the type of control panel provided with each printer version. Figure 3-3 illustrates and functionally describes each panel, its controls, and indicators.

Table 3-1. Control Panel Configurations

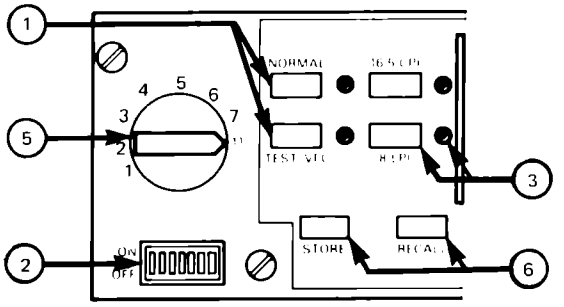
Printer Version	TI Part Number	Configuration Code
Basic	994292-0001	BSC
Forms Length Control	994292-0002	FLC
Vertical Format Control	994292-0003	VFC
Forms Length and Compressed Print	994293-0001	FCO
Vertical Format Control and Compressed Print	994293-0002	VCO



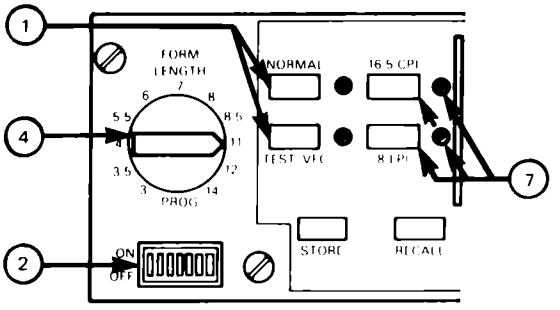
BASIC (994292–0001)BSC



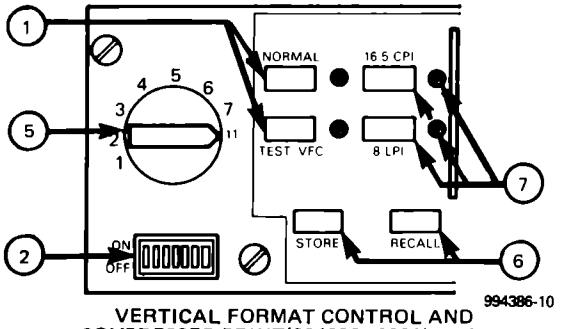
FORMS LENGTH (994292–0002) FLC



VERTICAL FORMAT CONTROL
(994292–0003) VFC



FORM LENGTH AND COMPRESSED PRINT
(994293–0001) FCO



VERTICAL FORMAT CONTROL AND
COMPRESSED PRINT(994293–0002) VCO

Figure 3-3. Control Panel Options

3.3.1 NORMAL and TEST/VFC Switches ①

Pressing the NORMAL switch enables the printer to receive data. By pressing the TEST/VFC switch, selecting the serial interface mode, and pressing the ONLINE switch, a cyclical character test pattern (barberpole) is printed. With the TEST/VFC mode selected and the printer OFF-LINE, the alternate function switches TAB, TAB SET, TAB CLEAR, SET TOP OF FORM, and LINE FEED on the control panel are enabled for vertical format control programming.

3.3.2 PENCIL Switches ②

Switches 1, 2, and 3 select baud rates (see Section 3.4.7) or the optional parallel input (PLT and LBP printer). Switches 4 and 5 select odd, even, or ignore parity (see Section 3.4.8). Switch 6 activates the automatic line feed override feature. Switch 7 activates the automatic top-of-form perforation skip override feature; automatic perforation skip causes the printer to skip three lines before the top of the next form. CHANGES IN PENCIL SWITCH SETTINGS DO NOT TAKE EFFECT UNTIL THE PRINTER GOES OFFLINE.

3.3.3 8 LPI Switch/Indicator ③

Pressing this switch selects either eight or six lines per inch. Lines per inch are also software programmable through the communications line (see Section 4). The indicator lights when the printer is in the 8 LPI mode.

3.3.4 FORM LENGTH Rotary Switch (FLC and FCO Printers Only) ④

This 12-position rotary switch permits selection of any one of the following 11 fixed form lengths: 3, 3.5, 4, 5.5, 6, 7, 8, 8.5, 11, 12, and 14 inches. In the PROG position this switch permits programming form lengths from the control panel (from 4 to 112 lines). THE PROGRAM (NONSTORABLE) IS LOST WHEN POWER TO THE PRINTER IS REMOVED.

3.3.5 VFC SWITCH (VFC and VCO Printers Only) ⑤

This eight-position rotary switch selects one of the eight stored vertical format programs. These eight channels are software programmable (see Section 4).

3.3.6 STORE and RECALL Switches (VFC and VCO Printers Only) ⑥

Pressing the STORE switch stores manually programmed vertical tabs, form length, and lines-per-inch spacing in the selected VFC channel. Pressing the RECALL switch causes the format program stored in the selected VFC channel to be recalled into working memory. STORE and RECALL are active only when the printer is in the TEST/VFC mode. Both are software programmable through the communications interface (see Section 4).

3.3.7 16.5 CPI Switch and Indicator (VFC and VCO Printers Only) ⑦

Pressing the 16.5 CPI switch selects the 16.5 CPI compressed print mode and lights the 16.5 CPI indicator light. Pressing this switch a second time returns the printer to the standard 10 CPI print mode. The printhead returns to the left margin each time a change is made in the character-per-inch selected. Characters-per-inch are software programmable through the communications interface (see Section 4).

3.4 OPERATING PROCEDURES

Before the Model 810 printer is placed in service, the operator must determine the following.

- Printer configuration: BSC, FLC, VFC, FCO, VCO. Check the label on the underside of the access door, or identify the printer by the control panel installed (see Figure 3-3).
- Baud rate of the received serial data, or whether parallel data (optional on LBP and PLT printers only) is to be received.
- Parity selection: ODD, EVEN, or ignored.

Perform the procedures in the following paragraphs that apply to your printer configuration and your printing requirements. The title of each paragraph identifies (in parentheses) the printer configuration to which it applies.

3.4.1 Power-Up Procedure (All Printers)

To switch the Model 810 on, proceed as follows.

1. Lift open the access door.
2. Check that printing ribbon and paper are correctly installed.
3. Set the power ON/OFF switch at the left rear of the printer to the ON (up) position.
4. Observe that the control panel ONLINE indicator is **not** lit and that the printhead is at the left margin.
5. Close the access door.

At this point the printer conforms to the following initial conditions:

- The printer is OFFLINE and in the normal mode.
- The form length is 279 mm (11 in.) for the BSC printer *and also for the FCO and FLC printers if the control panel FORM LENGTH switch is in the PROG position.* The FCO and FLC printers are set to the form selected by the FORM LENGTH switch. The VCO and VFC printers are set to the form length of the last vertical format stored or recalled.
- The line spacing is six lines per inch for the BSC, FCO, and FLC printers. *The VCO and VFC printers are set to the line spacing of the last vertical format stored or recalled.*
- The character spacing is ten characters per inch.
- All horizontal tabs are cleared from the working memory. (Horizontal tabs can be set only by software.)
- All vertical tabs are cleared from the working memory of the BSC, FCO, and FLC printers. *The VCO and VFC printers retain the vertical tab settings of the last vertical format stored or recalled.*
- The line counter is set to zero, causing the present line location to be the first line of the form for BSC, FCO, and FLC printers. The VCO and VFC printers retain the value of the line counter.

- The line buffer is empty (all previous printable characters have been cleared).

This completes the power-up procedure if:

- From previous operation the forms (paper) are aligned as desired, and the printhead adjust lever is correctly set.
- No changes to the above initial conditions are desired.
- The pencil switches (on the control panel) for the baud rate, parity, automatic line feed override, and automatic perforation skip override have been previously set as desired.

To change the printer from its initial condition status, perform the procedures that follow as applicable. After all procedures are completed, the printer is ready to receive data when placed ONLINE by the operator or by receiving a DC1 character through the communications line. All software commands can now be performed (to the degree permitted by the printer options) by the sending device (see Section 4).

3.4.2 Top-of-Form Adjustment (All Printers)

With power on, set the top of form as follows.

1. Check that ribbon and paper are correctly installed.
2. Press the auxiliary control NORMAL switch.
3. Press the FORM FEED switch on the control panel.
4. Press the FORM ALIGN ▲ switch or the FORM ALIGN ▼ switch until the printhead is at the approximate point where the first line of the form is to be printed.

NOTE

A more precise top-of-form adjustment can be made during the self-test or while data is being received by pressing the FORM ALIGN ▲ or FORM ALIGN ▼ switch until the next line printed is exactly aligned on the form. If the printed line appears to move away from the desired line location, press the other FORM ALIGN switch.

3.4.3 Printhead Adjustment (All Printers)

The printhead adjust lever controls the clearance between the platen and the face of the printhead. This clearance must be adjusted to accommodate the thickness of the forms used. With power on, adjust the printhead for optimum print quality as follows.

1. Lift open the access door.
2. Check that ribbon and paper are correctly installed.
3. Move the printhead adjust lever slightly to the right and completely toward the front of the printer.
4. If the self-test barberpole method is used, press the control panel TEST/VFC switch.

NOTE

The printhead adjustment can be made while the printer is ONLINE and data is being printed or while the self-test cyclical character pattern (barberpole) is being printed.

5. Ensure that the pencil switches are **not** set for parallel operation.
6. Press the control panel ONLINE switch to start printing.
7. Move the printhead adjust lever toward the rear of the printer until print quality is satisfactory.
8. If smudging occurs, the printhead is too *close* and must be backed off.
9. Move the printhead adjust lever until the nearest detent engages.
10. If the self-test barberpole method is used, press the control panel NORMAL switch.

11. Reset the pencil switches on the control panel to the previously set positions.

12. Close the access door.

3.4.4 Self-Test Diagnostic (All Printers)

With power on, perform the self-test as follows.

1. Lift open the access door.

2. Check that ribbon and paper are correctly installed.

3. Press the control panel TEST/VFC switch.

NOTE

The self-test always prints complete 132-character lines. Do not operate the printer without paper of the appropriate width.

4. Ensure that the pencil switches are **not** set for parallel operation (switch 1 must be OFF).

5. Press the control panel ONLINE switch and observe that the cyclical character pattern (barberpole) starts printing.

6. Ensure the entire 64-character (or optional 95-character) set is printed for each line and that each line shifts one column position from adjacent lines.

7. After several lines have been printed and checked, press the control panel NORMAL switch and observe that the barberpole stops printing.

8. Close the access door.

3.4.5 Lines-per-Inch Spacing (All Printers)

With power on and if the eight lines per inch spacing is desired, proceed as follows.

1. Lift open the access door.

2. Momentarily press the control panel 8 LPI switch.

3. Observe that the 8 lpi indicator lights.

4. Close the access door.

To return to six lines per inch spacing (initial condition), repeat the above procedure except observe that the 8 lpi indicator light goes out.

3.4.6 Characters-per-Inch Spacing (FCO, VCO)

With the power on and if the optional 16.5 characters per inch spacing (compressed print) is desired, proceed as follows.

1. Lift open the access door.

2. Momentarily press the control panel 16.5 CPI switch.

3. Observe that the 16.5 cpi indicator lights before the next line is printed.

4. Close the access door.

3.4.7 Baud Rate/Parallel Input Selection (All Printers)

To select the baud rate (or parallel input for PLT and LBP printers), proceed as follows.

1. Lift open the access door.

2. Using a ball-point pen or similar device, set the control panel pencil switches 1, 2, and 3 to the baud rate of the serial data to be received, or to the optional parallel input as listed in Table 3-2.

3. Close the access door.

Table 3-2. Control Panel Baud Rate Selections

Baud Rate		Pencil Switches		
Standard	BRO[1]	1	2	3
110	110	OFF	OFF	OFF
150	200	ON	OFF	OFF
300	300	OFF	ON	OFF
1200	1200	ON	ON	OFF
2400	2400	OFF	OFF	ON
4800	600	ON	OFF	ON
9600	9600	OFF	ON	ON
parallel[2]		ON	ON	ON

[1]Baud rate option (BRO) is available as an extra feature.
[2]Self-test (barberpole printout) is inoperable when pencil switches are set for parallel input.

3.4.8 Parity Selection (All Printers)

Select parity as follows.

1. Lift open the access door.
2. Set the control panel pencil switches as listed in Table 3-3 (also refer to Figure 3-3).
3. Close the access door.

3.4.9 Automatic Line Feed Override (All Printers)

Lift open the access door and set the control panel pencil switch 6 to ON for automatic line feed override or to OFF for automatic line feed after carriage return. Close the access door.

3.4.10 Automatic Perforation Skip Override (All Printers)

Lift open the access door and set the control panel pencil switch 7 to ON in order to override the automatic (three-line) perforation skip or to OFF for automatic (three-line) perforation skip. Close the access door.

3.4.11 Form Length Setting (BSC)

On the BSC printer the operator cannot set form lengths manually from the control panel. The printer is initialized during power-up with a 279 mm (11 in.) form length that can only be changed by a form length setting software command.

NOTE

A form length set by software is lost when power is removed from the printer.

Table 3-3. Control Panel Parity Selections

Function	Pencil Switches 4	5
Ignore Parity	OFF	OFF
Odd Parity	ON	ON
Even Parity	ON	OFF

3.4.12 Vertical Tab Setting (All Printers)

All printers have a working (nonstorable) memory in which vertical tabs can be set and retained as long as power is applied to the printer. With the power on, set vertical tabs as follows.

1. Lift open the access door.
2. If the form is not aligned as desired, perform a top-of-form adjustment.
3. Press the control panel FORM FEED switch and verify form length setting is correct. Refer to paragraphs on setting form length, if required.
4. Press the control panel NORMAL switch.
5. Press the control panel LINE FEED switch until the line to be tab-set is at the printhead.
6. Press the control panel TAB SET switch.
7. Repeat *steps* 5 and 6 as necessary to set all desired tabs.
8. Press the control panel NORMAL switch.
9. Press the control panel FORM FEED switch.
10. Verify your tab settings as follows:
    a. Press the control panel TEST/VFC switch.
    b. Press the control panel TAB switch and observe that your desired (tab-set) line is at the printhead. If the desired (tab-set) line is not at the printhead, press the control panel TAB CLEAR switch (this clears unwanted tabs from working memory).
    c. Repeat *step* b as necessary to verify that only desired tabs are finally set.
    d. After the last desired tab is verified, press the control panel TAB switch and observe that the next form is

aligned as desired in *step* 1 (or the top of form is at the reference mark).

e. Repeat *step* b as necessary to clear unwanted tabs from working memory.

f. Press the control panel NORMAL switch.

11. Close the access door.

3.4.13 Vertical Tab Clearing (All Printers)
With the printer power on, tabs can be cleared as follows.

1. Press the control panel FORM FEED switch.
2. Lift open the access door.
3. Press the control panel TEST/VFC switch.
4. Press the control panel TAB switch.
5. If the tab at this line location is to be cleared, press the control panel TAB CLEAR switch.
6. Repeat *steps* 4 and 5 as necessary to clear all unwanted tabs.
7. When the top of the next form is reached, press the control panel NORMAL switch.
8. Close the access door.

NOTE

On the BSC, FCO, and FLC printers, all vertical tabs can be simultaneously cleared simply by switching the power off. This resets these printers to the initial conditions when the printer power is again switched on.

3.4.14 Fixed Form Length Selection (FCO, FLC)
On the FCO and FLC printers, any one of 11 fixed form lengths can be selected. Selecting a fixed form length clears any previous form length settings (whether set by the operator or by software) from the working memory. With printer power on, select a fixed form length as follows.

1. Lift open the access door.
2. If the form is not aligned as desired, perform a top-of-form adjustment as outlined.
3. Press the control panel TEST/VFC switch.
4. Set the control panel FORM LENGTH rotary switch to the desired fixed form length position (also refer to Figure 3-3).
5. Press the control panel SET TOP OF FORM switch.
6. Press the control panel NORMAL switch.
7. Close the access door.

3.4.15 Programming Form Length (All Printers except BSC)
On the FCO, FLC, VFC, and VCO printers, any form length from 4 to 112 lines may be programmed. Programming the form length clears any previous form length (whether set by the operator or by software) from the working memory. With printer power on, program the form length as follows.

1. Lift open the access door.
2. If the form is not aligned as desired, perform a top-of-form adjustment as previously outlined.
3. Press the control panel TEST/VFC switch.
4. Set the control panel FORM LENGTH rotary switch to PROG (FCO and FLC printers only).
5. Press the control panel SET TOP OF FORM switch (this sets the line counter to zero).

6. Press the control panel LINE FEED switch until the top of the next form is aligned as desired (or the paper perforation is at the reference mark).

7. Press the control panel SET TOP OF FORM switch.

8. Press the control panel NORMAL switch (this sets the form length).

9. Close the access door.

3.4.16 Storing Vertical Format (VFC, FCO)

The VFC and VCO printers are equipped with vertical format control which can store a different vertical format in each channel of an eight-channel memory. Vertical formats can be stored by the operator or by software. The vertical format information that can be stored consists of the form length, vertical tab locations, and lines-per-inch spacing. *The stored vertical formats are retained even when printer power is* **off**. With printer power **on**, a vertical format is first entered into working memory and then stored as follows.

1. Lift open the access door.

2. If the form is not aligned as desired, perform a top-of-form adjustment as previously outlined.

3. Press the control panel TEST/VFC switch.

4. If eight lines per inch spacing is desired, momentarily press the control panel 8 LPI switch and observe that the 8 LPI indicator lights.

5. Press the control panel SET TOP OF FORM switch (this sets the line counter to zero).

6. Press the control panel LINE FEED switch until the line to be tab-set is at the printhead.

7. Press the control panel TAB SET switch.

8. Repeat *steps* 6 and 7 as necessary to set all desired tabs.

9. Press the control panel LINE FEED switch until the next form is aligned as desired (or the paper perforation is at the reference mark).

10. Press the control panel SET TOP OF FORM switch.

11. Press the control panel NORMAL switch and then press the TEST/VFC switch.

12. Verify your vertical format setting as follows.
    a. Press the control panel TAB switch and observe that the desired (tab-set) line is at the printhead. If your desired (tab-set) line is not at the printhead, press the control panel TAB CLEAR switch (this clears unwanted tabs from memory).

    b. Repeat *step* a as necessary to verify that only desired tabs are set.

    c. After the last desired tab is verified, again press the control panel TAB switch and observe that the top of the next form is aligned as desired (or the paper perforation is at the reference mark). If not, press the control panel TAB CLEAR switch.

    d. Repeat *step* c as necessary to clear unwanted tabs from memory.

13. Set the control panel VFC rotary switch to the desired channel.

14. Momentarily press the control panel STORE switch.

15. Press the control panel NORMAL switch.

16. Close the access door.

3.4.17 Recalling Vertical Format (VFC, VCO)

The VFC and VCO printers are equipped with vertical format control which permits recalling previously stored vertical formats into the working memory by the operator or by software. With printer power **on**, a vertical format in any one of

the eight channels of memory can be recalled into the working memory by the operator as follows.

1. Lift open the access door.
2. Set the control panel VFC rotary switch to the desired channel (also refer to Figure 3-3).
3. Press the control panel TEST/VFC switch.
4. Momentarily press the control panel RECALL switch.
5. Press the control panel NORMAL switch.
6. Perform the top-of-form adjustment.
7. Close the access door.

3.4.18 Power-Down Procedure (All Printers)

To switch off the printer requires setting the power ON/OFF switch (at the left rear of the printer) to OFF. Remember that when power is again applied to the printer, it resets to certain initial conditions, according to the configuration of the printer. If conditions other than the initial conditions are to be retained, they must be noted and reentered in the printer when power is again applied. For more complete information on the initial conditions of each printer configuration, refer to the power-up procedure.

Section 4

Operating Instructions (Software Control)

4.1 INTRODUCTION

This section presents information and procedures required to control the Model 810 printer through the communications interface. All printer functions which can be controlled by the sending device are described in tabular form. More complex functions requiring a sequence of control codes are further described in step-by-step procedures.

4.2 COMMANDS (WITHOUT LINE BUFFER OPTION)

Table 4-1 describes the action taken by the 810 in response to various received control characters. In the second column of Table 4-1, the ASCII control code characters sent to the printer are underlined. The letter "**N**" represents a number to be sent as noted. The letter "**n**" represents an ASCII code character that produces the required binary equivalent from Table 4-2. The plus (+) sign in Table 4-1 indicates that the character which follows is sent next in the command sequence.

All characters received by the printer are stored in a first-in-first-out (FIFO) buffer. When the printing mechanism is not busy, data characters are transferred from the FIFO to the line buffer. The contents of the line buffer are printed when any of the following actions occurs.

- The printer receives a carriage return (CR) character or any of the paper movement characters: line feed (LF), vertical tab (VT), form feed (FF), or tab-to-line (DC2).

  Paper movement characters are treated as line terminators. The following line begins at the left margin, just as though the paper movement character had been followed by a carriage return.

- The printer receives the 133rd printable character.

- The printer receives a deselect (DC3) character.

- The operator switches the printer OFFLINE (deselecting the printer) and then presses the printer LINE FEED switch.

- The operator presses the printer FORM FEED switch.

4.3 COMMANDS (WITH LINE BUFFER OPTION)

Table 4-3 describes the action taken by the Model 810 printer equipped with the Line Buffer option in response to various received control characters. In the second column of Table 4-3, the ASCII control code characters which are to be sent to the printer are underlined. The letter "**N**" represents a number which is to be sent as noted. The letter "**n**" represents an ASCII code character that produces the required binary equivalent from Table 4-2. The plus (+) sign indicates that the character which follows is to be sent next in the command sequence.

All characters received by the printer are stored in a FIFO buffer. When the printing mechanism is not busy, data characters are transferred from FIFO to the line buffer. The contents of the line buffer are printed when any of the following actions occurs.

Table 4-1. Software Commands (for Printers without Line Buffer Option)

Command	ASCII Code Characters Received	Printer Action Taken
Carriage Return	CR (See Note 1)	This command causes data, if any, in the line buffer to be printed. Because of the bidirectional printing capability of the printer, a carriage return is not executed. Instead, the carriage stops upon completion of printing a line. When the next line is received, the carriage is positioned to print forward or backward, whichever direction requires the least carriage movement.
Delete	DEL	This command clears the line buffer. If the NDE (no delete) option has been installed, this command will be ignored.
Deselect	DC3 (See Note 6)	This command deselects the printer, causing it to ignore all incoming data and control characters except DC1 (select) after printing out the contents of the line buffer.
Form Feed	FF	This command causes data, if any, in the line buffer to be printed and advances the paper to the top of the next form.
Form Length Set	ESC + 2 + n (See Note 3)	This command sets the form length used by the Form Feed (FF) command to n lines (from 4 to 112 lines).
Horizontal Tab	HT	This command causes spaces to be entered in the line buffer up to the next horizontal tab location, where printing will begin.
Horizontal Tab Set	ESC + 3 + n_1 + n_2 ... + n_k + NUL (See Notes 3 and 5)	This command clears all existing horizontal tabs and sets new tabs at columns n_1, n_2 ,..., and n_k (column 1 through 126).
Line Feed	LF	This command causes data, if any, in the line buffer to be printed and advances the paper one line space.
Line Width Set	ESC + : + n (See Note 3)	This command causes the printer to print n columns wide (from 2 to 126 columns). Line width is automatically set to 132 columns at power-up.
Line Width 132	ESC + ;	This command causes the printer to print lines 132 columns wide. (Line width is automatically set to 132 columns at power-up.)
Null	NUL	This command terminates the tab setting sequence for both horizontal and vertical tabs, otherwise it is ignored.
Recall	ESC + 9 + N (See Note 4)	This command recalls the stored vertical format information in the optional VFC channel N memory to the working memory. If the VFC option is not installed, this command is ignored. (See Note 2.)

Note 1: Underlined characters represent the ASCII code.
Note 2: Vertical format information includes line/inch, form length, tabs. The form length recalled takes effect after the first form feed.
Note 3: The number "n" as used in the DC2, DC4, ESC + 1, ESC + 3, and ESC + : commands represents a seven-bit binary number. See Table 4-2 for the ASCII character code which will transmit the desired binary number.
Note 4: The number "N" as used in the ESC + 8 and ESC + 9 commands represents the ASCII code number (one through eight) which corresponds to the selected VFC channel.
Note 5: The first column "n" is designated as column zero.
Note 6: The DCO strappable option disables this feature.

Table 4-1. Software Commands (for Printers without Line Buffer Option) (Concluded)

Command	ASCII Code Characters Received	Printer Action Taken
Select	DC1 (See Note 6)	When power is applied to the printer, this command selects the printer, enabling it to receive data.
Store	ESC + 8 + N (See Note 4)	This command stores vertical format information from the working memory in the optional VFC channel N memory. If the VFC option is not installed, this command is ignored. (See Note 2.)
Tab to Address	DC4 + n (See Notes 3 and 5)	This command causes spaces to be entered in the line buffer from the present column up to column n (through column 126); n must be greater than the present column. If n is less than the present column this command will be ignored.
Tab to Line	DC2 + n (See Note 3)	This command causes the paper drive system to slew to the line specified by n (line 4 through 112) after printing contents of the line buffer (n must be greater than the present line). If n is less than the present line, this command will be ignored.
Vertical Tab	VT	This command causes data, if any, in the line buffer to be printed and advances the paper to the next vertical tab location or top of form, whichever occurs first. If no vertical tabs are set, this command causes the paper to be advanced to top of form.
Vertical Tab Set	ESC + 1 + n_1 + n_2 + ... + n_k + NUL	This command clears all existing vertical tabs and sets tabs at lines n_1, n_2, ..., and n_k (where n is less than or equal to line 112).
6 LPI	ESC + 4	Sets the paper drive system to 6 lines per inch. (The paper drive system is automatically set to 6 lines per inch at power-up.)
8 LPI	ESC + 5	This command sets the paper drive system to 8 lines per inch.
10 CPI	ESC + 6	This command sets the carriage system to 10 characters per inch. (The carriage system is set to 10 characters per inch at power-up.)
16.5 CPI	ESC + 7	This command sets the carriage system to 16.5 characters per inch.
Expanded Print (EXP)	SO	With the Expanded Print Option installed this command sets the carriage system to the Expanded Print mode. The SO control character will be recognized only if it is the first character of the new line.

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Note 1: Underlined characters represent the ASCII code.
Note 2: Vertical format information includes line/inch, form length, tabs.
Note 3: The number "n" as used in the DC2, DC4, ESC + 1, ESC + 3, and ESC + : commands represents a seven-bit binary number. See Table 4-2 for the ASCII character code which will transmit the desired binary number.
Note 4: The number "N" as used in the ESC + 8 and ESC + 9 commands represents the ASCII code number (one through eight) which corresponds to the selected VFC channel.
Note 5: The first column "n" is designated as column zero.
Note 6: The DCO strappable option disables this feature.

- The printer receives a carriage return (CR) character.

  With the decodes carriage return (DSC) option enabled, the printer receives a carriage return (CR) character or any of the paper movement characters: line feed (LF), vertical tab (VT), or form feed (FF).

  Paper movement characters are treated as line terminators with the DSC option enabled. Tab-to-line (DC2 + n) is independent of the DSC option. This command must be followed by a carriage return for correct operation.

- The printer receives the 132nd printable character.
- The printer receives a deselect (DC3) character.
- The operator switches the printer OFFLINE (deselecting the printer) and then presses the printer LINE FEED switch.
- The operator presses the printer FORM FEED switch.

Table 4-2. Software Control Column or Line "*n*" Number Equivalents

For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character
1	SOH	33	!	65	A	97	a
2	STX	34	"	66	B	98	b
3	ETX	35	#	67	C	99	c
4	EOT	36	$	68	D	100	d
5	ENQ	37	%	69	E	101	e
6	ACK	38	&	70	F	102	f
7	BEL	39	'	71	G	103	g
8	BS	40	(	72	H	104	h
9	HT	41	)	73	I	105	i
10	LF	42	*	74	J	106	j
11	VT	43	+	75	K	107	k
12	FF	44	,	76	L	108	l
13	CR	45	-	77	M	109	m
14	SO	46	.	78	N	110	n
15	SI	47	/	79	O	111	o
16	DLE	48	0	80	P	112	p
17	DC1	49	1	81	Q	113	q
18	DC2	50	2	82	R	114	r
19	DC3	51	3	83	S	115	s
20	DC4	52	4	84	T	116	t
21	NAK	53	5	85	U	117	u
22	SYN	54	6	86	V	118	v
23	ETB	55	7	87	W	119	w
24	CAN	56	8	88	X	120	x
25	EM	57	9	89	Y	121	y
26	SUB	58	:	90	Z	122	z
27	ESC	59	;	91	[	123	{
28	FS	60	<	92	\	124	|
29	GS	61	=	93	]	125	}
30	RS	62	>	94	^	126	~
31	US	63	?	96	_		
32	SPACE	64	@	96	`		

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Table 4.3 Software Commands (for Printers with Line Buffer Option)

Command	ASCII Code Characters Received[1]	Printer Action Taken
Carriage Return	CR	CR causes data, if any, in the line buffer to be printed. Because of the bidirectional printing capability of the printer, a carriage return is not executed. Instead, the carriage stops upon completion of printing a line. When the next line is received, the carriage is positioned to print forward or backward, whichever direction requires the least carriage movement.
Delete	DEL	DEL clears the line buffer.
Deselect	DC3 (See Note 6)	DC3 deselects the printer, causing it to ignore all incoming data and control characters, except DC1 (select), after printing out the contents of the line buffer.
Form Feed	FF	FF causes data, if any, in the line buffer to be printed when the DSC option is enabled and advances the paper to to the top of the next form.
Form Length Set	ESC + 2 + *n* + CR (See Note 3)	This command sequence sets the form length used by the *form feed* (FF) command to *n* lines (from 4 to 112 lines).
Horizontal Tab	HT (See Note 7)	HT causes spaces to be entered in the line buffer up to the next horizontal tab location, where printing will begin.
Horizontal Tab Set	ESC + 3 + n_1 + n_2 ... + n_x + NUL + CR (See Notes 3 and 5)	This command sequence clears all existing horizontal tabs and sets new tabs at columns n_1, n_2, ..., and n_x (column 1 through 126).
Line Feed	LF	LF causes data, if any, in the line buffer to be printed when the DSC option is enabled and advances the paper one line space.
Null	NUL	NUL terminates the tab setting sequence for both horizontal and vertical tabs; otherwise, it is ignored.
Recall	ESC + 9 + *N* + CR (See Note 4)	This command sequence recalls into the working memory the vertical format information stored in the optional VFC channel *N* memory (see Note 2). If the VFC option is not installed, this command is ignored.
Select	DC1 (See Note 6)	When power is applied to the printer, DC1 selects the printer, enabling it to receive data.
Store	ESC + 8 + *N* + CR (See Note 4)	This command sequence stores vertical format information from the working memory into the optional VFC channel *N* memory (see Note 2). If the VFC option is not installed, this command is ignored.
Tab to Address	DC4 + *n* (See Notes 3 and 7)	This command sequence causes spaces to be entered in the line buffer from the present column up to column *n* (through column 126); *n* must be greater than the present column. If *n* is less than the present column, this command is ignored.
Tab to Line	DC2 + *n* + CR (See Note 3)	This command sequence causes the paper drive system to slew to the line specified by *n* (line 4 through 112) after printing contents of the line buffer; *n* must be greater than the present line. If *n* is less than the present line, this command is ignored.
Vertical Tab	VT	VT causes data, if any, in the line buffer to be printed when the DSC option is enabled and advances the paper to the next vertical tab location or to top of form, whichever occurs first. If no vertical tabs are set, this command causes the paper to be advanced to top of form.
Vertical Tab	ESC + 1 + n_1 + n_2 + ... + n_x + NUL + CR	This command sequence clears all existing vertical tabs and sets new tabs at lines n_1, n_2 + ..., and n_x (where *n* is less than or equal to line 112).
6 LPI	ESC + 4 + CR	This command sequence sets the paper drive system to 6 lines per inch. (The paper drive system is automatically set to 6 lines per inch at power-up.)
8 LPI	ESC + 5 + CR	This command sets the paper drive system to 8 lines per inch.
10 CPI	ESC + 6 + CR	This command sets the carriage system to 10 characters per inch. (The carriage system is set to 10 characters per inch at power-up.)
16.5 CPI	ESC + 7 + CR	This command sets the carriage system to 16.5 characters per inch.
Expanded Print (EXP)	SO	With the Expanded Print option installed, SO sets the carriage system to the *expanded print* mode. SO is recognized only *if it is the first character of the new line.*

NOTES

1. Underlined characters represent the ASCII code.
2. Vertical format information includes lines per inch, form length, tabs. The form length recalled takes effect after the first form feed.
3. The number "*n*" as used in the DC2, DC4, ESC + 1, and ESC + 3, and ESC + : commands represents a seven-bit binary number. See Table 4-2 for the ASCII character code which will transmit the desired binary number.
4. The number "*N*" as used in the ESC + 8 and ESC + 9 commands represents the ASCII numbers from one through eight which correspond to the selected VFC channel.
5. The first column "*n*" is designated as column zero.
6. The DCO strappable option disables this feature.
7. Terminate each line with a carriage return when using horizontal tabbing. Printable character count does not include spaces entered automatically in the line buffer.

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4.4 SOFTWARE (REMOTE) CONTROL

Step-by-step procedures for remote control of printer functions requiring more complex sequences of control codes are outlined below. Note that underlined characters represent the ASCII code.

4.4.1 Software Form Length Setting

Any form length from four lines up to the maximum 112 lines may be set. If a parity is selected, a parity bit must be added to the seven-bit number "*n*" as the most significant (eighth) bit. When received by the printer, the following sequence causes the form length to be set at the line number represented by "*n*".

1. ESC
2. 2
3. *n* (the binary equivalent of the number of lines in the desired form length)

NOTE

Use Table 4-2 to select the ASCII character which produces the required binary equivalent.

4. CR (the software form length setting command must be terminated with a carriage return if the printer is equipped with the line buffer option)

Example:

ESC + 2 + @ sets the form length at 64 lines. The ASCII character "@" produces a binary 100 0000 (decimal 64).

4.4.2 Software Horizontal Tab Setting

When received by the printer, the following sequence causes all previous horizontal tabs to be cleared and new horizontal tabs to be set at the columns represented by "*n*" (where "n_1" is the first tabbed column and "n_k" is the last tabbed column). The first column "*n*" is designated as column zero. Horizontal tabs may be set at columns 1 through 126. If a parity is selected on the printer, a parity bit must be added to the character code (seven-bit character or binary number "*n*") as the most significant (eighth) bit.

1. ESC
2. 3
3. *n* (the binary equivalents of the columns n_1 through n_k *where the horizontal tabs are to be set*)

NOTE

Use Table 4-2 to select the ASCII character which produces the required binary equivalent.

4. NUL
5. CR (the software horizontal tab setting command must be terminated with a carriage return if the printer is equipped with the line buffer option)

Example:

ESC + 3 + SOH + 4 + T + t + NUL sets horizontal tabs at columns 1, 52, 84, and 116. The ASCII code characters *SOH, 4, T,* and *t* produce the binary numbers 000 0001 (decimal 1), 011 0100 (decimal 52), 101 0100 (decimal 84), and 111 0100 (decimal 116), respectively, where the line begins at column zero.

4.4.3 Software Line Width Setting

When received by the printer, the following sequence causes the line width to be set at the number of columns represented by "*n*". Any line width up to the maximum 126 columns may be set. If parity is selected on the printer, a parity bit must be added to the seven-bit number "*n*" as the most significant (eighth) bit.

NOTE

The software line width setting command is ignored by the printer if the Line Buffer option is installed.

1. ESC
2.

3. *n* (the binary equivalent of the number of columns in the desired line width)

NOTE

Use Table 4-2 to select the ASCII character which produces the required binary equivalent.

Example:

ESC + : + P sets the line width at 80 columns. The ASCII character *P* produces a binary 101 0000 (decimal 80).

4.4.4 Software Vertical Format Recall

The following sequence recalls the vertical format information stored in the optional VFC channel memory (channels 1 through 8) into the working memory after clearing the previous vertical format information from the working memory. The form length of the channel takes effect following the first form feed operation.

NOTE

If the VFC option is not installed, this command is ignored.

1. ESC
2. 9
3. *N* (the ASCII code character for the channel selected)
4. FF (form feed)
5. CR (the software vertical format recalled command must be terminated with a carriage return if the printer is equipped with the Line Buffer option)

Example:

ESC + 9 + 7 + FF recalls into the working memory the vertical format stored in VFC channel 7.

4.4.5 Software Vertical Format Store

The following sequence stores the vertical format information from the working memory into the selected channel. *The vertical format information in the working memory is not cleared.*

NOTE

If the VFC option is not installed, this command is ignored.

1. ESC
2. 8
3. *N* (the ASCII character for the VFC channel into which the vertical format information from the working memory is to be stored)
4. CR (the software vertical format store command must be terminated with a carriage return if the printer is equipped with the Line Buffer option)

Example:

ESC + 8 + 3 stores the vertical format information from the working memory into VFC channel 3.

4.4.6 Software Vertical Tab Setting

When received by the printer, the following sequence causes all previous vertical tabs to be cleared and new vertical tabs to be set at the lines represented by "*n*" (where "n_1" is the first tabbed line and "n_k" is the last tabbed line). Vertical tabs may be set at any line up to and including the 112th line. If a parity is selected on the printer, a parity bit must be added to the seven-bit number "*n*" as the most significant (eighth) bit. Commands to set tabs at lines beyond the 112th line are ignored.

1. ESC
2. 1
3. *n* (the binary equivalents of the lines "n_1" through "n_k" where the vertical tabs are to be set)

NOTE

Use Table 4-2 to select the ASCII character which produces the required binary equivalent.

4. NUL

5. CR (the software vertical tab setting command must be terminated with a carriage return if the printer is equipped with the Line Buffer option)

Example:

ESC + 1 + DLE + 4 + T + t + NUL sets vertical tabs at lines 16, 52, and 84. The ASCII characters *DLE, 4, T,* and *t* produce the binary numbers 001 0000 (decimal 16), 011 0100 (decimal 52), 101 0100 (decimal 84), and 111 0100 (decimal 116) respectively. The binary number 111 0100 (decimal 116) is ignored since it is beyond the 112-line maximum.

4.4.7 Software Expanded Print Setting

The Expanded Print option doubles the width of each printable character using an 18 × 7 dot matrix instead of the standard 9 × 7 matrix. This corresponds to five characters per inch when the printer is normally in the 10 cpi mode or 8.25 characters per inch when the printer is normally in the 16.5 cpi (compressed print) mode.

The expanded print mode can be entered only by sending the software command *shift out* (SO) to the printer. The SO command is recognized only if it is the *first character of a new line.* Any line width setting is divided in half, resulting in a maximum line width of 66 characters. The carriage system stays in the *expanded print* mode for one line of printable characters and then returns to the previously set print mode.

Section 5

Interface Information (Printers without Line Buffer Option)

5.1 STANDARD INTERFACE

As shown in Figure 5-1, the transmitting device sends asynchronous data to the printer. The data consists of control and printable characters. When the printer receives the data, it stores both the control and printable characters in the FIFO buffer. The processor determines whether each character is a control or a printable character. Printable characters are stored in the print buffer; control characters are acted upon by the processor, changing the operation of the printer.

Characters from the print buffer are printed by the Model 810 at a rate of 150 characters per second (cps). Printing begins either when the processor receives a line termination character [line feed (LF), carriage return (CR), vertical tab (VT), form feed (FF), or tab-to-line (DC2)] or when the 133rd printable character is read from the FIFO after 132 printable characters have been stored in the print buffer. The average rate at which characters are read from the FIFO is slower than the print rate because of the time required to line-feed the paper. If the rate at which characters are received by the FIFO exceeds the rate at which they are read out, the FIFO accumulates characters.

With printers using the EIA or TTY interface, a BUSY signal is sent when 249 characters are stored in the FIFO. The printer can still accept up to seven more characters after the BUSY signal. With printers using the parallel (PLT) interface, a BUSY signal is sent when 256 characters are stored in the FIFO; in this case no characters can be received after the BUSY signal. A BUSY signal also is sent if any of the following conditions occurs: an encoder error, a paper-out condition, or the printer is placed OFFLINE. The transmitting device must not send data after it receives the BUSY signal. The BUSY signal is not synchronized with the data.

The printer stops sending the BUSY signal (caused by a full FIFO buffer) when the number of control and printable characters stored in the FIFO drops to 121 or less. Pressing RESET clears the BUSY signal caused by an encoder error or paper-

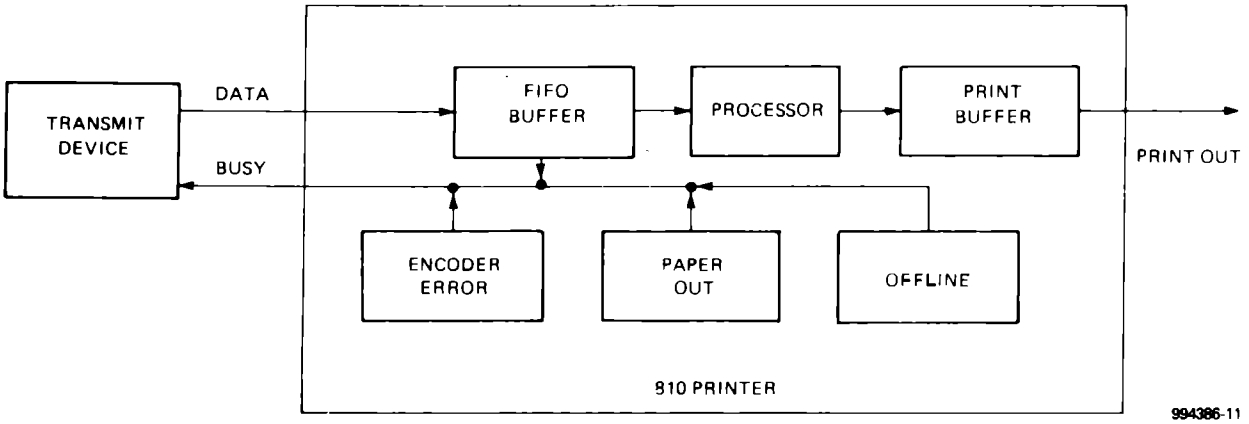


Figure 5-1. Busy Signal Generation Block Diagram (Printers without Buffer Option)

out condition. Placing the printer ONLINE clears the BUSY signal caused by the OFFLINE condition.

When continuous data transmission is desired at the 1200 baud rate, the BUSY signal may be ignored if an average of 37 characters per line is printed per form length. This average may be calculated by dividing the number of characters printed by the total number of lines per form length. Continuous data transmission precludes the use of forms control functions.

The following paragraphs contain signal interface information for the standard serial interface (EIA) as well as for the optional parallel (PLT) and TTY interfaces.

TI Part Number	Interface
994401-0002	PLT
994401-8002 (Field Installed)	
994402-0001	TTY
994402-8001 (Field Installed)	

5.2 CABLING AND GROUNDING

When standing behind the printer, the communications interface connectors are located at the left rear (Figure 5-2). All printers have an *EIA Standard RS-232-C* interface connector for serial input. Parallel or TTY interface connectors are available as options. Cables for various input devices are available as options. Refer to Appendix H for cabling requirements to the indicated input devices.

The logic (signal) ground is connected to the safety (chassis) ground by a jumper from E6 to E7 on the Motherboard (Figure 5-3). The logic ground can be isolated from the safety ground by removing this jumper (ISC option). To gain access to the ground jumper, remove the printer cover, the electronics cover, and the printed circuit boards as instructed in the paragraphs on Battery Replacement.

When using the standard serial interface, satisfactory printer operation cannot be guaranteed when signal cable length exceeds the *EIA standard RS-232-C* recommendation of 15.25 meters (50 feet). With proper design of the cable and its drivers, satisfactory operation of cable lengths up to 305 meters (1000 feet) can be achieved. Beyond this distance the current loop interface option or limited distance modems should be considered.

WARNING

Long signal cables can pose a safety hazard. Such cables must be adequately protected against lightning strikes or accidental shorting to power conductors. Routing of the cable through grounded metallic conduit, with no power conductor in the same conduit, or installation of suitable protective devices at each end of the cable are possible methods of preventing operator injury or equipment damage. These precautions are particularly important if any portion of the signal cable is installed outdoors.

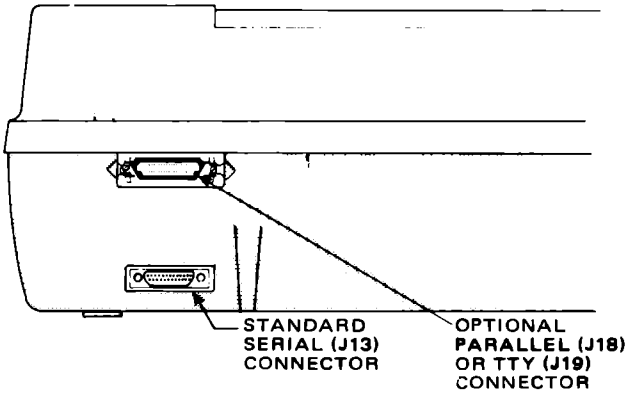


Figure 5-2. Communications Interface Connectors 994386-12

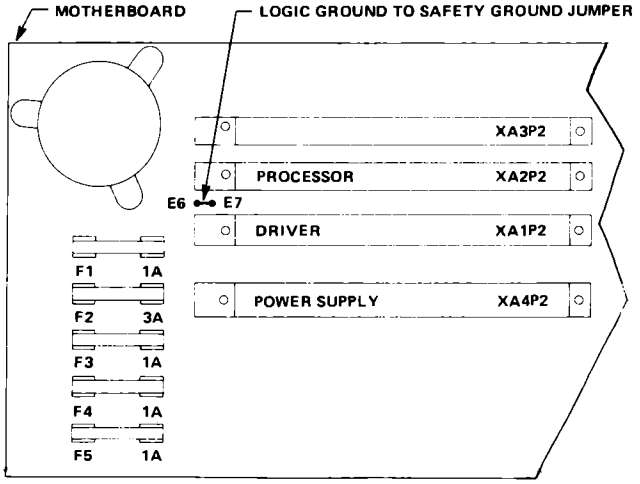


Figure 5-3. Ground Jumper Location on the Motherboard 994386-13

5.3 SERIAL INTERFACE

The serial interface signals at the Model 810 printer communications connector J13 are defined in Table 5-1.

5.3.1 Baud Rate

The selectable data transmission rates of the Model 810 printer are 110, 150, 300, 1200, 2400, 4800, or 9600 baud. The baud rate is selected by the first three of the seven pencil switches on the auxiliary control panel. See Section 3 for pencil switch settings. With the Baud Rate (BRO) option, the following data transmission rates are replaced: 150 with 200 and 4800 with 600.

5.3.2 Signal Levels and Terminations

Serial interface signal levels are defined by *EIA Standard RS-232-C* as follows:

	−25 to −3 −Vdc	−3 to +3 +Vdc	+3 to +25 Vdc
Data Signal	MARK	Not Defined	SPACE
Timing or Control Function	OFF	Not Defined	ON

The terminator load impedance is a noninductive 3000 to 7000 ohm dc resistance. Any open circuit driver voltage will not exceed 25 Vdc.

5.3.3 Asynchronous Data Format

Each character sent to the 810 on the received data line consists of one start bit, seven data bits, one parity bit, and one or two stop bits as shown in Figure 5-4.

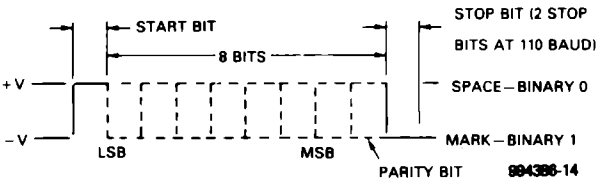


Figure 5-4. Asynchronous Data Format

5.3.4 Timing. The printer accepts data when the transmitting device raises both the *data set ready* and the *carrier detect* line to a positive level. The printer holds the *data terminal ready* line at a positive level when ONLINE or at a negative level when OFFLINE. With the DNB option enabled, the printer holds the *data terminal ready* line at a positive level when ONLINE and NOT BUSY, or at a negative level when OFFLINE or BUSY.

Table 5-1. Serial Interface Connector Signals (J13)

J13 Pin No.	Signal Name	Designation EIA	Designation C.C.I.T.T.	Source	Function
1	Protective Ground	AA	101	None	Chassis ground
2	Transmitted Data	BA	103	Printer	Held to negative EIA level in the test mode
3	Received Data	BB	104	Input Device	Received serial data
4	Request to Send	CA	105	Printer	Held to a negative EIA level
5	Clear to Send	CB	106	Input Device	(Not Used)
6	Data Set Ready	CC	107	Input Device	Must be at positive EIA level for the printer to receive data
7	Signal Ground	AB	102	None	Return path for data and control signals
8	Carrier Detect	CF	109	Input Device	Must be at positive EIA level for the printer to receive data
9	+12 Volts	—	—	Printer	May be used as bias voltage for inputs to printer (1000-ohms source impedance)
10	−12 Volts	—	—	Printer	May be used as bias voltage for inputs to printer (1000-ohms source impedance)
11	Reverse Channel	SCA	120	Printer	Held to negative EIA level when *standard* printer is busy, and to positive EIA level when *standard* is not busy; these levels are inverted in IRC printer
20	Data Terminal Ready	CD	108.2	Printer	Held to positive EIA level when *standard* printer is ONLINE or when the DNB printer is ONLINE and not busy; and to negative EIA level when *standard* printer is OFFLINE, or when DNB printer is OFFLINE or BUSY.

The *reverse channel* line sends printer-BUSY status to the transmitting device. The *reverse channel* line is held at a positive level when the printer is free to accept data; when the printer becomes BUSY, it sets the *reverse channel* line to the negative level. With the IRC option enabled, these signal levels are inverted (ready = negative level; busy = positive level). The printer accepts the character which causes the BUSY condition (and up to seven more characters) but ignores any subsequent characters until the BUSY condition is cleared. The basic EIA interface timing is shown in Figure 5-5.

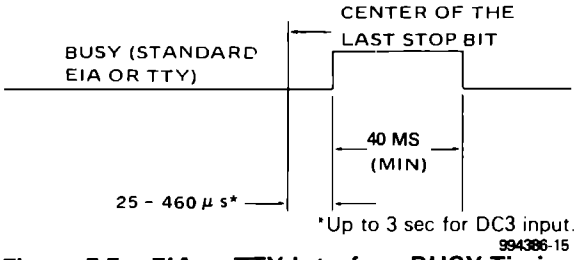


Figure 5-5. EIA or TTY Interface BUSY Timing

5.3.5 Parity Checking. The bit immediately before the stop bit in the asynchronous data format is the parity bit. Characters received with incorrect parity are printed as "◆", and the control panel ERROR indicator lights. A parity error in a format statement terminates the statement.

5.4 PARALLEL INTERFACE (OPTIONAL)

The optional parallel interface (PLT) signals at connector J18 are defined in Table 5-2.

5.4.1 Signal Levels and Terminations

For a high input signal to the 810, the transmitting device must be able to source 0.320 milliamperes at +2.4 Vdc. For a low input signal, the transmitting device must be able to sink 14 milliamperes at +0.4 Vdc. For a low output, the printer can sink up to 14 milliamperes at +0.4 Vdc. Data lines are terminated in the printer by 1000 ohms to +5 Vdc. *Data strobe* is terminated in the printer by 470 ohms to 5 Vdc.

Table 5-2. Parallel Interface Connector Signals (J18), PLT Printers

Signal Pin[1]	Return Pin[2]	Signal Name	Source	Description
1	19	Data Strobe	Input Device	0.5 μs pulse (minimum) used to clock data from the input device to the printer logic
2	20	Data 1	Input Device	Input data levels: a high represents a binary one; a low represents a binary ZERO; all printable characters (i.e., codes having a ONE in Data 6 or Data 7) are stored in the print buffer; control characters (i.e., codes having a ZERO in both Data 6 and Data 7) are used to define control functions.
3	21	Data 2	Input Device	
4	22	Data 3	Input Device	
5	23	Data 4	Input Device	
6	24	Data 5	Input Device	
7	25	Data 6	Input Device	
8	26	Data 7	Input Device	
9	27	Data 8	Input Device	
10	28	Acknowledge	Printer	A pulse LOW indicates a character has been received, and the printer is ready to accept another character
11	29	Busy	Printer	A signal HIGH indicates the printer cannot receive data
12	–	PE (Paper Out)	Printer	A signal HIGH indicates the printer is out of paper
13	–	SLCT (Online)	Printer	A signal HIGH indicates the printer is selected
16	–	Logic Ground	Printer	Logic ground
17	–	Chassis Ground	Printer	Chassis ground (protective)
18	–	+5 Vdc	Printer	For test purposes
31	30	REMRST[3]	Input Device	A signal LOW terminates a form feed or vertical tab motion
32	14	Fault[3]	Printer	A signal LOW indicates a fault condition

NOTES

1. Connector pins, other than those listed, are not used.
2. Signal pins with return pins indicate twisted pairs.
3. This signal is not available in parallel interface cables (Part No. 994359-0001), revisions E, F, and G.

5.4.2 Parallel Interface Timing

The basic, parallel interface timing is shown in Figure 5-6.

5.4.3 Data Strobe Acknowledgement

A *data strobe* pulse following an *acknowledge* pulse stores the parallel data in the FIFO buffer. If the printer is BUSY, the *data strobe* stores the parallel data in the FIFO buffer if that data is strobed at minimum 10.5 μs intervals.

5.5 TTY CURRENT LOOP INTERFACE (OPTIONAL)

The optional TTY current loop interface uses a four-wire, passive, neutral current loop which does not interfere with the standard EIA serial interface. Data can be received from either interface, provided the other interface is in a spacing condition or its connector is unplugged. The TTY current loop interface signals at connector J19 are defined in Table 5-3.

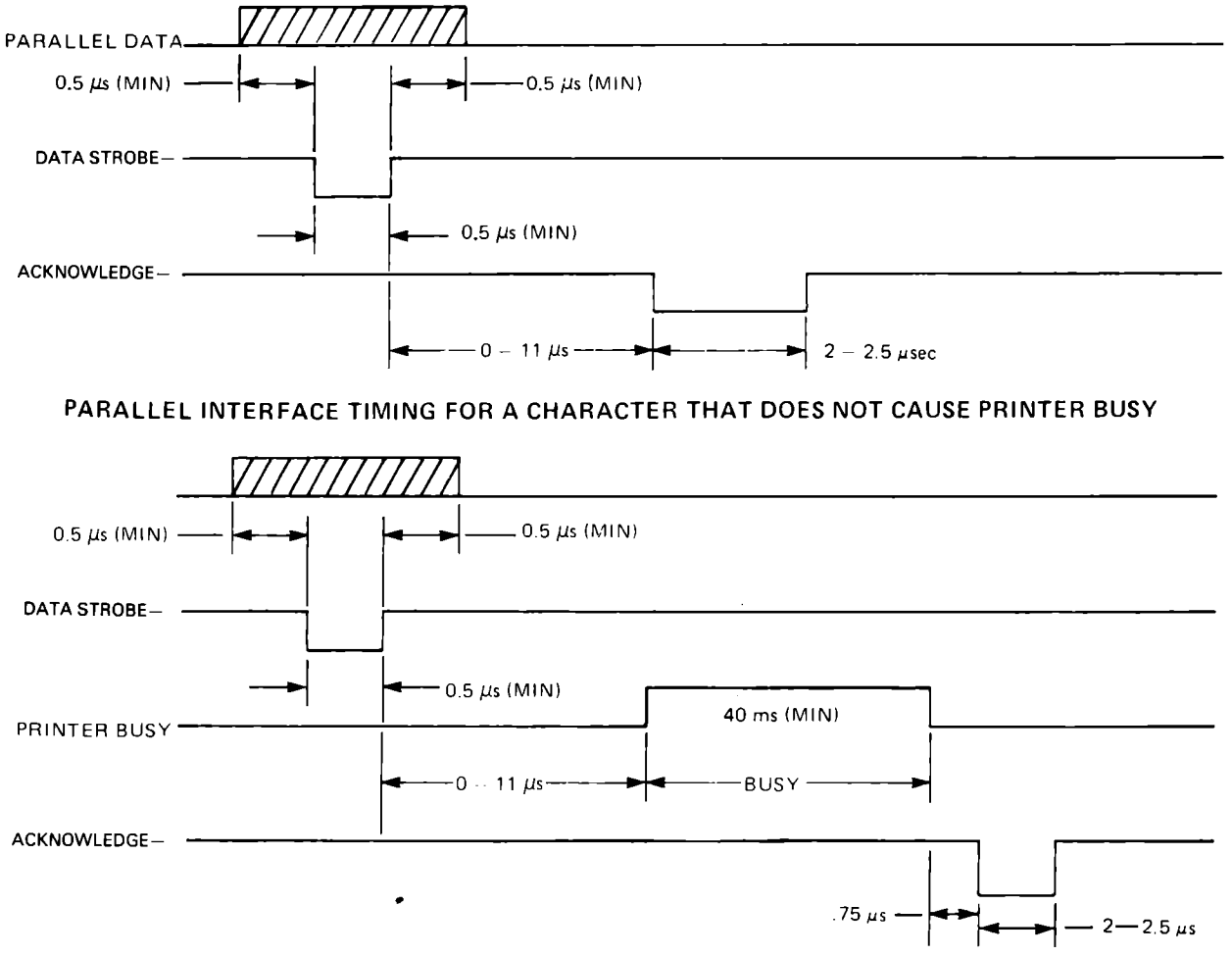


Figure 5-6. Parallel (PLT) Interface BUSY Timing

Table 5-3. TTY Current Loop Interface Signals (J19)

PIN	SIGNAL NAME	FUNCTION
1	TTY Transmitted Data	Low impedance (marking) between pins 1 and 2 when the TTY printer is ready to accept data; high impedance (spacing) when the TTY printer is busy
2	TTY Transmitted Data Return	
3	Ground	Provides chassis ground
4	TTY Received Data Return	Senses changes in current (data) through pins 4 and 5; HIGH current for marking; LOW current for spacing
5	TTY Received Data	

5.5.1 Signal Levels and Terminations

The TTY current loop receiver senses current levels from the sending device and converts them to the corresponding EIA voltage levels. The drop across the receive inputs is 3 volts maximum at 20-mA loop current. The marking/spacing decision threshold is nominally 10 ($\pm$6) mA. The TTY current loop transmitter switches the current supplied by the sending device. The input to the transmitter is the *EIA reverse channel* (SCA) signal, representing the printer READY or BUSY status. The voltage drop across the transmitter terminals is less than 1.5 volts at 20-mA loop current. The maximum spacing leakage current is 500 μA at 45 Vdc. The transmitter output is ON or marking (low impedance) when the TTY printer is ready to accept data, and OFF or spacing (high impedance) when the TTY printer is busy.

5.5.2 Basic TTY Interface Timing

The asynchronous data format shown in Figure 5-4 also applies to the TTY current loop. The basic TTY interface timing is shown in Figure 5-5.

5.6 RS-422 SERIAL INTERFACE (OPTIONAL)

The optional RS-422 serial interface uses a four-wire active balanced signal arrangement for transmitted status and received data.

The RS-422 signals are available at both J13, the standard RS-232C connector, and at J19, the auxiliary interface connector. The RS-422 interface signals are defined in Table 5-4.

5.7 RS-422 SIGNAL CONVENTION

RS-422 circuits are balanced or "differential." That is, the binary state of a signal is indicated by the polarity of one conductor with respect to a second paired conductor which provides a dedicated return path for the interface signal current. While the voltage of each conductor typically is referenced to earth ground, any electrical disturbance theoretically induces the same voltage with respect to earth on both conductors so that the net effect at the receiver input terminals is zero. This allows reliable communication at distances up to 1219 m (4000 ft) at data rates up to 9600 baud.

Two signal pairs are provided. One signal pair designated Send + and Send – is used to transmit status, and another pair designated Receive + and Receive – is used to receive data. RS-422 follows a negative logic convention to define the significance of a signal in terms of the voltage polarity of one conductor with respect to the second conductor within a pair, as shown in Table 5-5.

Table 5-4. RS-422 Interface Signals

PIN	J13	J19
1	Protective Ground	
2	Transmitted Data	
3	Received Data	
4	Request to Send	
5	Clear to Send	
6	Data Set Ready	
7	Signal Ground	Signal Ground
8	Carrier Detect	
9	+ 12 Volt Bias	
10	– 12 Volt Bias	
11	READY/BUSY (REV. CH)	
15	RS-422 Receive +	RS-422 Receive +
17	RS-422 Receive –	RS-422 Receive –
19	RS-422 Send +	RS-422 Send +
20	Data Terminal Ready	
24	RS-422 Send –	
25		RS-422 Send –

Table 5-5. RS-422 Logic Convention

Transmit	Receive	MARK	SPACE
Send +	Receive +	Negative	Positive
Send –	Receive –	Positive	Negative

Section 6

Interface Information (Printers with Line Buffer Option)

6.1 LINE BUFFER OPTION INTERFACE

The Line Buffer option assures that the Model 810 can receive up to 132 printable characters when not busy. This is done with a 132-printable-character counter and a line-termination decoder which groups printable characters into one-line blocks. The line buffer sends a BUSY signal when 132 printable characters are counted or when it decodes a delete (DEL) or a line termination character [line feed (LF), carriage return (CR), vertical tab (VT), or form feed (FF)].

Characters are received by the printer in the asynchronous data format. The BUSY signal is synchronized to occur in the middle of the stop bit of the character which caused the BUSY signal. The BUSY signal is cleared when the FIFO buffer is empty or when printing begins. Printing begins when 132 printable characters are counted or a CR character is received. With the DSC option enabled, printing also begins when LF, VT, or FF is received. The FIFO buffer may become full when a large number of control characters are sent along with printable characters. A BUSY signal is sent when the FIFO buffer becomes full with 249 characters. The BUSY signal caused by the full buffer condition clears when the number of control and printable characters stored is reduced to 121 or less.

In addition to the BUSY conditions described above, a BUSY signal is sent for an encoder error, a paper-out condition, or a printer OFFLINE condition. Pressing the RESET button clears the BUSY signal caused by an encoder error or paper-out condition. Placing the printer ONLINE clears the BUSY signal caused by the OFFLINE condition.

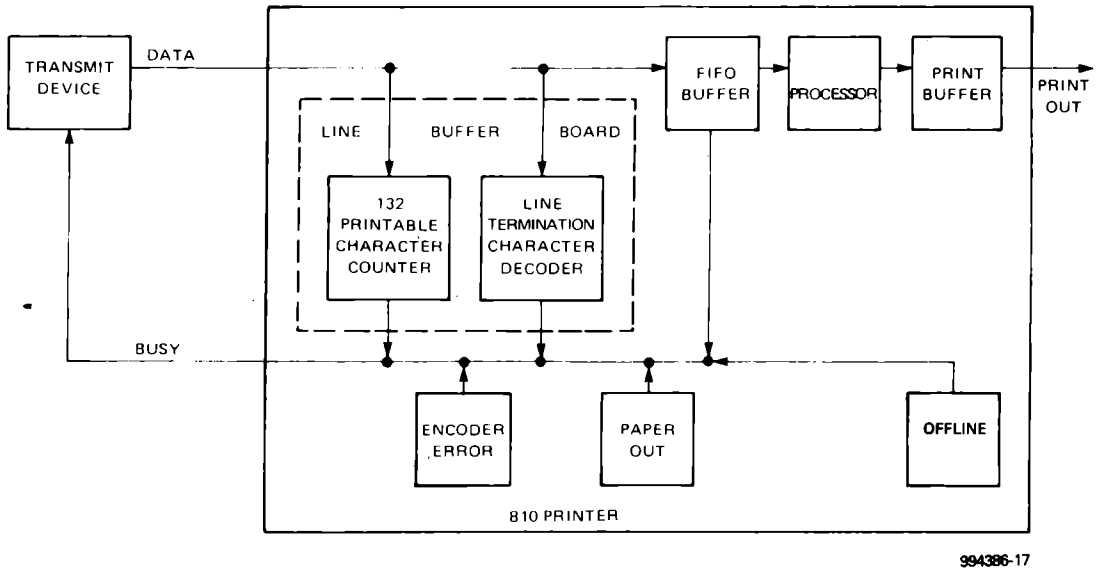


Figure 6-1. Busy Signal Generation Block Diagram (Printers with Line Buffer Option)

The following paragraphs contain signal interface information for the optional EIA (LBE), parallel (LBP), and current loop (LBT) interfaces.

TI Part Number	Interface
994511-0001	LBE
994511-8001 (Field Installed)	
994512-0001	LBT
994512-8001 (Field Installed)	
994513-0001	LBP
994513-8001 (Field Installed)	

6.2 CABLING AND GROUNDING

When viewed from the back, the communications interface connector (or connectors) is located at the left rear of the printer (Figure 5-2). All printers have an *EIA Standard RS-232-C* interface connector for serial input. A parallel or a TTY interface connector is available as an option. Cables for various input devices also are available as options. Refer to Appendix H for cabling requirements to the indicated input devices.

The logic (signal) ground is connected to the safety (chassis) ground by a jumper from E6 to E7 on the Motherboard (Figure 5-3). The logic ground can be isolated from the safety ground by removing this jumper. To gain access to ground jumper, remove the printer cover, the electronics cover, and the printed circuit boards as instructed in the paragraphs on Battery Replacement.

Refer to the section on Grounding and Cabling regarding cable length.

6.3 SERIAL INTERFACE (LBE OPTION)

The serial interface signals at connector J13 are defined in Table 6-1.

6.3.1 Baud Rate

The selectable data transmission rates on the Model 810 printer are 110, 150, 300, 1200, 2400, 4800, or 9600 baud. The baud rate is selected by the first three of the seven pencil switches on the control panel. See Section 3 for pencil switch settings. With the Baud Rate option (BRO), the following data transmission rates are replaced: 150 with 200 and 4800 with 600.

Table 6-1. Serial Interface Connector Signals (J13), LBE Printers

J13 Pin No.	Signal Name	Designation		Source	Function
		EIA	C.C.I.T.T		
1	Protective Ground	AA	101	None	Chassis ground
2	Transmitted Data	BA	103	Printer	Held to negative EIA level in the test mode
3	Received Data	BB	104	Input Device	Received serial data*
4	Request to Send	CA	105	Printer	No connection
5	Clear to Send	CB	106	Input Device	(Not Used)
6	Data Set Ready	CC	107	Input Device	Must be at positive EIA level for the printer to receive data
7	Signal Ground	AB	102	None	Return path for data and control signals
8	Carrier Detect	CF	109	Input Device	Must be at positive EIA level for the printer to receive data
9	+ 12 Volts	—	—	Printer	May be used as bias voltage for inputs to printer (1000-ohms source impedance)
10	− 12 Volts	—	—	Printer	May be used as bias voltage for inputs to printer (1000-ohms source impedance)
11	Reverse Channel	SCA	120	Printer	Held to negative EIA level when *standard* printer is BUSY, and to positive EIA level when *standard* is not busy; these levels are inverted in IRC printer
20	Data Terminal Ready	CD	108.2	Printer	Held to positive EIA level when *standard* printer is ONLINE or when the DNB printer is ONLINE and not busy; and to negative EIA level when *standard* printer is OFFLINE, or when DNB printer is OFFLINE or BUSY.

*With the gated EIA (GED) option enabled the received data line is held LOW during a busy condition, preventing the printer from receiving data.

6.3.2 Signal Levels and Terminations

Serial interface signal levels are defined by *EIA Standard RS-232-C* as follows:

	−25 to −3Vdc	−3 to +3Vdc	+3 to −25Vdc
Data Signal	MARK	Not Defined	SPACE
Timing or Control Function	OFF	Not Defined	ON

The terminator load impedance is a noninductive 3000 to 7000 ohm dc resistance. Any open circuit driver voltage will not exceed 25 Vdc.

6.3.3 Asynchronous Data Format

Each character sent to the printer on the received data line consists of one start bit, seven data bits, one parity bit, and one or two stop bits as shown in Figure 6-2.

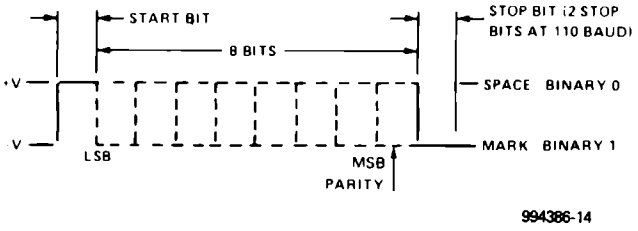


Figure 6-2. Asynchronous Data Format

6.3.3.1 Timing. The 810 accepts data when the device has raised both the *data set ready* and the *carrier detect* line to a positive level. The printer holds the *data terminal ready* line at a positive level when ONLINE, or at a negative level when OFFLINE. With the DNB option enabled, the printer holds the *data terminal ready* line at a positive level when ONLINE and not BUSY, or at a negative level when OFFLINE or BUSY.

The *reverse channel* line sends printer BUSY status to the transmitting device. The line is held at a positive level when the printer is free to accept data; when the printer becomes BUSY, it sets the *reverse channel* line to the negative level. With the IRC option enabled, these signal levels are inverted (ready = negative level; busy = positive level). With the GDS and/or GED options enabled, the printer accepts the character which causes BUSY but ignores all subsequent characters until ready. With both options disabled, the printer continues to accept characters until the FIFO is full but the printable character count may be in error, causing erratic operation. For optimum performance, the sending device should stop transmitting immediately when the BUSY signal occurs. The basic LBE interface timing is shown in Figure 6-3.

6.3.3.2 Parity Checking. The bit immediately before the stop bit in the asynchronous data format is the parity bit (see Figure 6-2). Characters received with incorrect parity are printed as " ◆ " symbols, and the control panel ERROR indicator lamp activates. A parity error in a format statement terminates the statement.

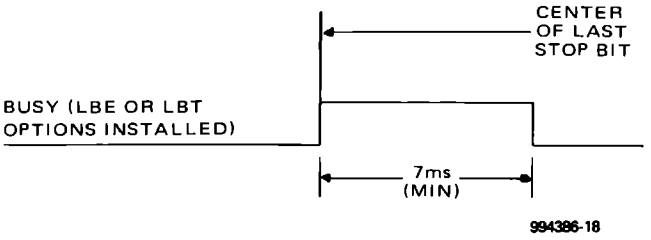


Figure 6-3. EIA (LBE Option) and TTY (LBT Option) BUSY Timing

6.4 PARALLEL INTERFACE (LBP OPTION)

The optional parallel interface (LBP) signals at connector J18 are defined in Table 6-2.

Table 6-2. Parallel Interface Connector Signals (J18), LBP Printers

Signal Pin[1]	Return Pin[2]	Signal Name	Source	Description
1	19	Data Strobe	Input Device	0.5μs pulse (minimum) used to clock data from the input device to the printer logic
2	20	Data 1	Input Device	Input data levels: a high represents a binary ONE; a low represents a binary ZERO; all printable characters (i.e., codes having a ONE in Data 6 or Data 7) are stored in the print buffer; control characters (i.e., codes having a ZERO in both Data 6 and Data 7)are used to define control functions
3	21	Data 2	Input Device	
4	22	Data 3	Input Device	
5	23	Data 4	Input Device	
6	24	Data 5	Input Device	
7	25	Data 6	Input Device	
8	26	Data 7	Input Device	
9	27	Data 8	Input Device	
10	28	Acknowledge	Printer	A pulse LOW indicates that a character has been received and that the printer is ready to accept another character
11	29	Busy	Printer	A signal HIGH indicates that the printer cannot receive data
12	—	PE (Paper Out)	Printer	A signal HIGH indicates that the printer is out of paper
13	—	SLCT (On Line)	Printer	A signal HIGH indicates that the printer is selected
15	33	OSCXT (External Clock)	Printer	125 kHz signal for external use
16	—	Logic Ground	Printer	Logic ground
17	—	Chassis Ground	Printer	Chassis ground (protective)
18	—	+5 Vdc	Printer	For test purposes
31	30	REMRST	Input Device	A signal LOW terminates a form feed or vertical tab motion
32	14	Fault	Printer	A signal LOW indicates a fault condition
34	35	Line Count	Printer	Isolated reed-relay contacts close upon each line feed

NOTES
1. Connector pins, other than those listed, are not used.
2. Signal pins with return pins indicate twisted pairs.

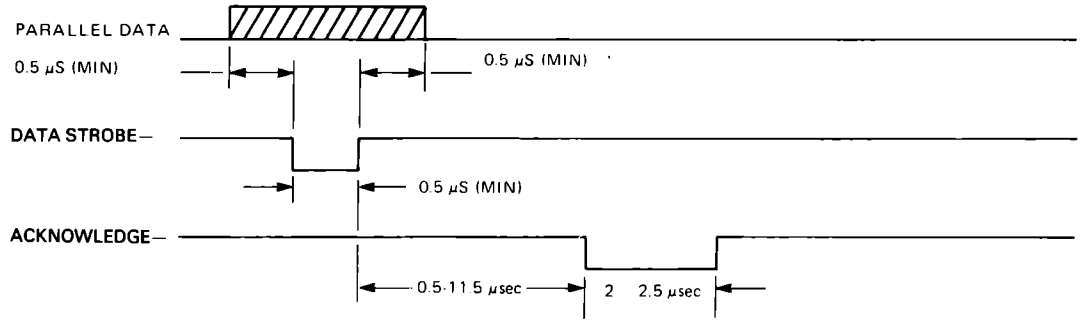
6.4.1 Signal Levels and Terminations

For a high input signal to the 810 printer, the transmitting device must be able to source 0.320 milliamperes at +2.4 Vdc. For a low input signal, the transmitting device must be able to sink 14 milliamperes at 0.4 Vdc. For a high output from the printer, the printer is able to source up to 0.320 milliamperes at +2.4 Vdc. For a low output, the printer is able to sink up to 14 milliamperes at +0.4 Vdc. Data lines are terminated in the printer by 1000 ohms to +5 Vdc. *Data strobe* is terminated in the printer by 470 ohms to +5 Vdc.

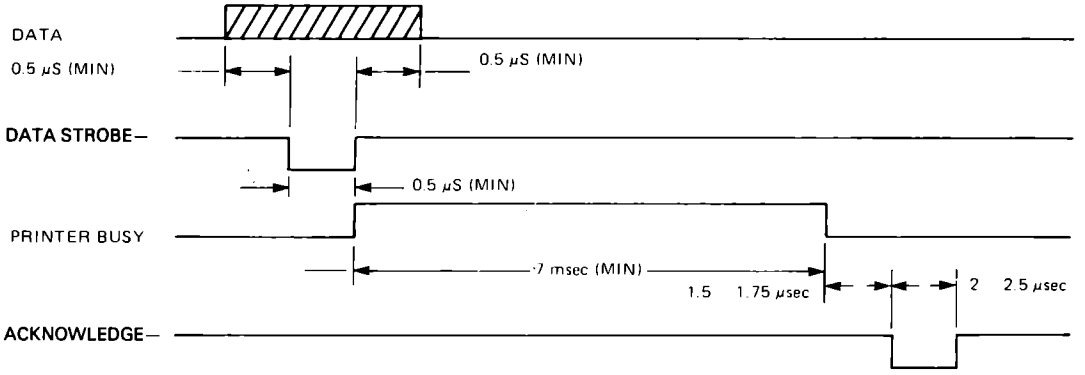
6.4.2 Basic Parallel Timing

The basic parallel interface timing for Line Buffer option printers is shown in Figure 6-4.

Basic Parallel Timing. The basic parallel interface timing is as shown below.



PARALLEL INTERFACE TIMING FOR A CHARACTER THAT DOES NOT CAUSE PRINTER BUSY



PARALLEL INTERFACE TIMING FOR A CHARACTER THAT CAUSES PRINTER BUSY

994386-19

Figure 6-4. Basic Parallel (LBP) Interface BUSY Timing, Line Buffer Option

6.4.3 Data Strobe Acknowledgment

A *data strobe* pulse following an *acknowledge* pulse stores the parallel data in FIFO buffer provided the data is strobed at minimum 11.5 μs intervals. With the gated data strobe (GDS) option enabled, the *data strobe* pulse will not store the parallel data in the FIFO buffer when the printer is BUSY unless BUSY is caused by OFFLINE. In this case, the printer continues to accept characters but recognizes only DC1.

6.5 TTY CURRENT LOOP INTERFACE (LBT OPTION)

The TTY current loop option uses a four-wire, passive, neutral current loop. When using the TTY current loop interface, the EIA interface cable must be disconnected from the printer. The TTY current loop interface signals at connector J19 are defined in Table 6-3.

Table 6-3. TTY Current Loop Interface Signals with Line Buffer Option

PIN	SIGNAL NAME	FUNCTION
1	TTY Transmitted Data	Low impedance (marking) between pins 1 and 2 when the TTY printer is ready to accept data; high impedance (spacing) when the TTY printer is busy
2	TTY Transmitted Data Return	
3	Ground	Provides chassis ground
4	TTY Received Data Return	Senses changes in current (data) through pins 4 and 5; HIGH current for marking; low current for spacing.
5	TTY Received Data	

With the half-duplex (HDP) option enabled, the TTY *received data return* line is shorted to the TTY *transmitted data* line. This permits two-wire, half-duplex, operations with the TTY *received data* line and the TTY transmitted *data return* line. Current is sent into the TTY *received data* line and returned via the TTY *transmitted data return* line.

6.5.1 Signal Levels and Terminations

The TTY current loop receiver senses current levels from the transmitting device and converts them to the corresponding TTL voltage levels. The voltage drop across the receive inputs is 3 volts maximum at 20 mA loop current. The marking/spacing decision threshold is nominally 10 ± 6 mA. The TTY current loop transmitter switches the current supplied by the transmitting device.

The input to the transmitter is the EIA *reverse channel* signal (SCA), representing the printer READY or BUSY status. The voltage drop across the transmitter terminals is less than 1.5 volts at 20 mA loop current. The maximum spacing leakage current is 500 μA at 45 Vdc. The transmitter output is ON or marking (low impedance) when the TTY printer is ready to accept data, and OFF or spacing (high impedance) when the TTY printer is BUSY.

6.5.2 Timing

The asynchronous data format shown in Figure 6-2 also applies to the TTY current loop. The basic TTY interface timing is shown in Figure 6-3.

Section 7

Theory of Operation

7.1 INTRODUCTION

This section discusses the principles of operation including a system block diagram, a discussion of dot matrix printing, and an overview of the major printer subsystems. The theory of operation of the Model 810 describes the printer functions at a printed circuit board level.

7.2 PRINCIPLES OF OPERATION

Figure 7-1 introduces the key electromechanical and electronic subsystems of the Model 810 printer. These subsystems include the Electronic Control Subsystem (paragraph 7.2.1), the Printhead Carriage Subsystem (paragraph 7.2.2), the Paper Feed Subsystem (paragraph 7.2.3), the Power Supply (paragraph 7.2.4), and the Line Buffer Option Interface (paragraph 7.2.5). The Electronic Control Subsystem includes a TMS 8080A microprocessor containing firmware programs to define printer operation as commanded by the control panel switches and/or incoming signals from a sending device. When the printer is online, this subsystem interprets incoming data, control panel signals, and feedback signals from the Printhead Carriage Subsystem. The Electronic Control Subsystem also generates all necessary timing and control signals fed to the Printhead Carriage and Paper Feed subsystems.

The Printhead Carriage Subsystem produces carriage motion, drive signals to generate characters via the dot matrix printhead (based on commands from the microprocessor), and feeds carriage

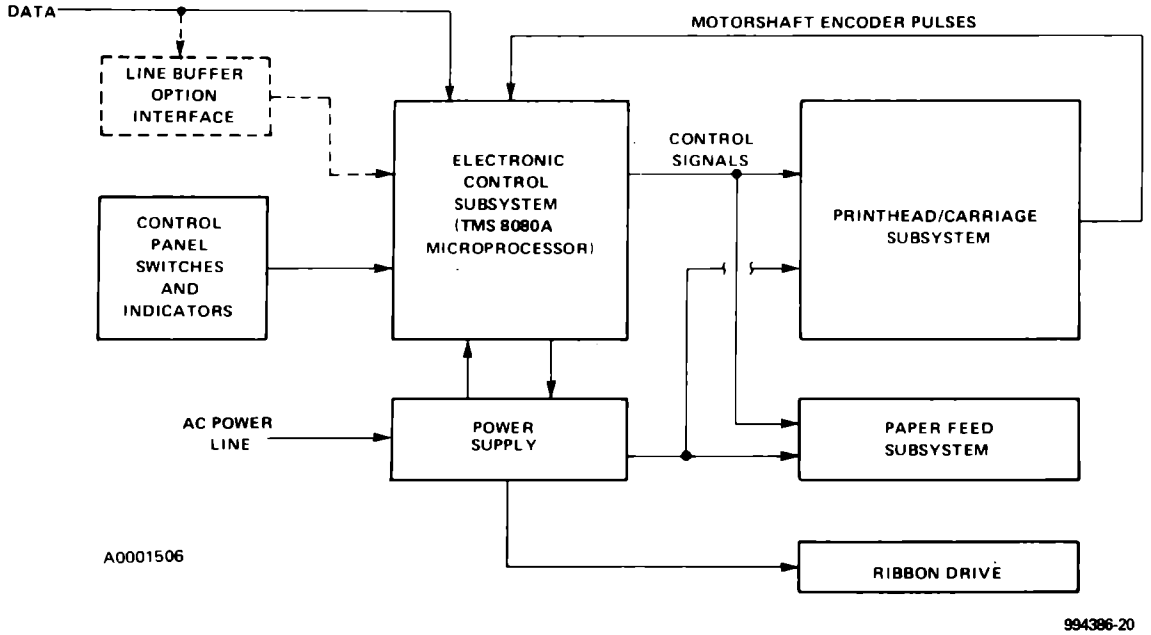


Figure 7-1. Model 810 Printer Simplified Block Diagram

position encoder pulses back to the microprocessor. The Paper Feed Subsystem controls paper motion.

The Power Supply provides all ac, dc, and regulated dc voltages necessary to operate the printer. The optional line buffer interface monitors input data from the EIA, TTY, and parallel input ports and controls the BUSY and ACKNOWLEDGE signals which modify the basic read-only memory (ROM) firmware.

7.2.1 Electronic Control Subsystem

This subsystem, TI Part No. 994244, consists of an 8080A microprocessor system; serial and parallel communications interfaces; control panel and device board interface; and speed counter, printhead timing, and carriage encoder logic. It is located on the processor board and illustrated in Figure 7-2.

The microprocessor system consists of a Texas Instruments 8080A microprocessor, 256 bytes of random-access memory (RAM), 4K bytes of read-only memory (ROM), 2K bytes of optional ROM, 1K bytes of optional programmable read-only memory (PROM), a special-purpose TMS 5501 I/O device, and a 256-character first-in first-out (FIFO) buffer.

The RAM provides a 256-byte workspace for the microprocessor. It holds one line of 132 characters to be printed, saves the register contents during interrupt cycles (referred to as a "pushdown stack"), and provides temporary storage for the flag registers.

The ROM contains the dot patterns for the printable characters, the firmware programs, and the routines required to perform the printer functions. Portions of firmware programs that are customer-application dependent are stored in optional PROMs. The FIFO buffer stores input characters received during the period the printer is busy printing.

The 8080A communicates with other components of the microprocessing system through a 16-bit parallel address bus and an eight-bit parallel data bus. (Refer to Appendix D for detailed information.) After power-up, the microprocessor system scans the control panel switches to determine the control functions (ONLINE, FORM FEED, NORMAL or TEST mode, etc.) required by the switch settings. Incoming data from the sending device is fed into the printer through the EIA Interface or the (optional) TTY or parallel interfaces. All serial data comes in through the TMS 5501 I/O and timing device (see Appendix E for detailed information) and is then fed to the FIFO buffer via the

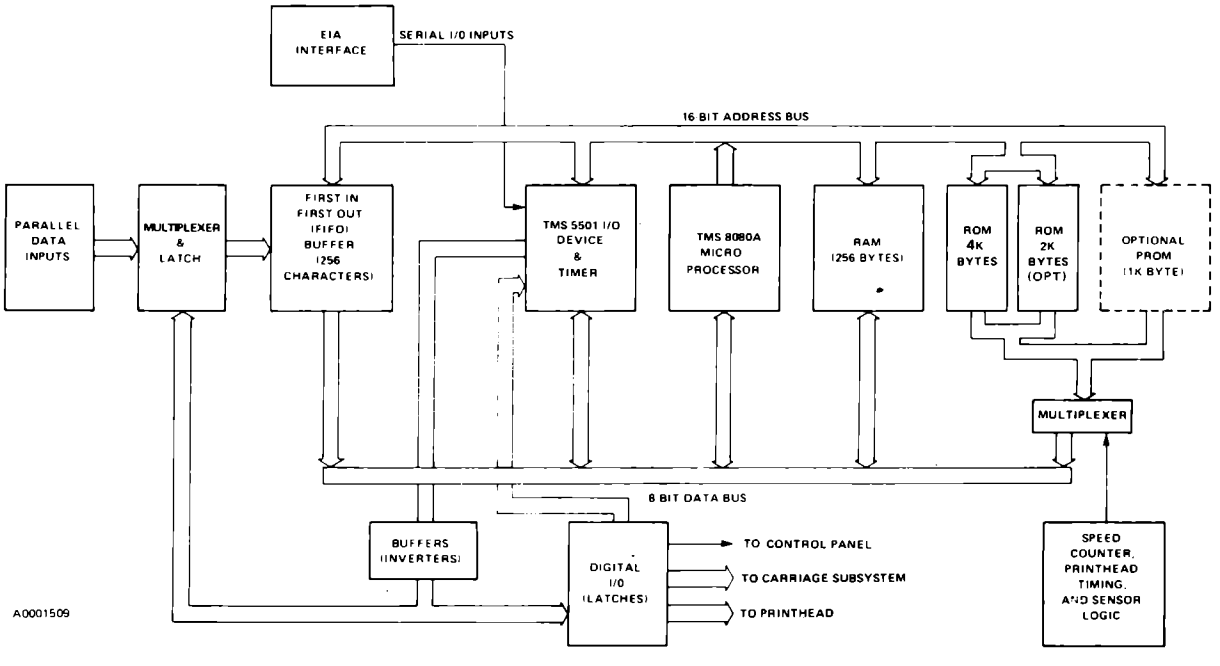


Figure 7-2. Electronic Control Subsystem Block Diagram

eight-bit data bus. Data is stored in the FIFO buffer until print time. Parallel data is fed through a multiplexer latch circuit and loaded directly into the FIFO buffer.

At print time, the microprocessor analyzes the characters stored in the FIFO buffer one by one to determine if they are printable characters (alphabet, numerals, and punctuation marks), control characters [line feed (LF), carriage return (CR), horizontal tab (HT), etc.], or four special characters (DC2, DC4, ESC, or NUL) which alter the operating characteristics of the printer.

The characters are then fed back over the eight-bit data bus through the TMS 5501 to the print buffer (a 132-character space) in the RAM. The microprocessor reads the ASCII characters in the print buffer one at a time to determine the address in the ROM that contains the dot pattern required to form the desired character. Each one × seven vertical column of the nine × seven matrix required to form the character is read from the ROM; fed through the I/O and timing device and the inverters; and then goes to I/O latches which control the printhead drivers. The microprocessor then commands these drivers (a part of the Printer/Carriage Subsystems) to drive the printhead and print the character one column at a time. During this process, the microprocessor is also controlling carriage and paper motion.

7.2.1.1 Firmware Program Overview. The Model 810 software programs, referred to as firmware, are stored in the ROM. Application-dependent software programs are stored in optional PROMs. At power-up, the microprocessor is reset to hexadecimal address 0000 and begins executing instructions to perform the following tasks.

1. Clear the RAM.
2. Initialize flags, states, constants, and variables.
3. Clear the TMS 5501 and unmask interrupts.
4. Initialize control latches.
5. Start the fail-safe timer.
6. Align the stepper motor to phase A.
7. Align the carriage to the left bumper.
8. Initialize the printer options.

7.2.1.2 NORMAL or TEST Mode. The system then moves into either the NORMAL or TEST mode, depending on the control panel switch setting. It next begins to loop through the background software programs without stopping (NORMAL mode) until an interrupt is received. The major subroutines in this loop initiate tasks such as paper motion, carriage motion, and printing. These tasks are completed by interrupt-driven software with the microprocessor system returning to the background loop during its spare time.

The sending device communicates to the software in the form of commands. The complete set of commands is given in Tables 7-1 through 7-3. Software commands control all physical movement of the printing mechanism.

7.2.2 Printhead Carriage Subsystem

This subsystem moves the printhead at a controlled velocity across the width of the line and provides drive current to drive the printhead solenoids. The elements of this subsystem are:

1. Printhead and printhead carriage.
2. Dc servo motor with shaft encoder.
3. Power drive circuits for dc servo motor and printhead solenoids.
4. Capstan, wire rope, and tensioning mechanisms.
5. Printhead-to-platen positioning mechanism.

Drawing number 994183 in Section 9 shows the mechanical relationship of these components. The power drive circuits for the dc servo motor are a part of the driver printed circuit board as shown in Figure 7-3.

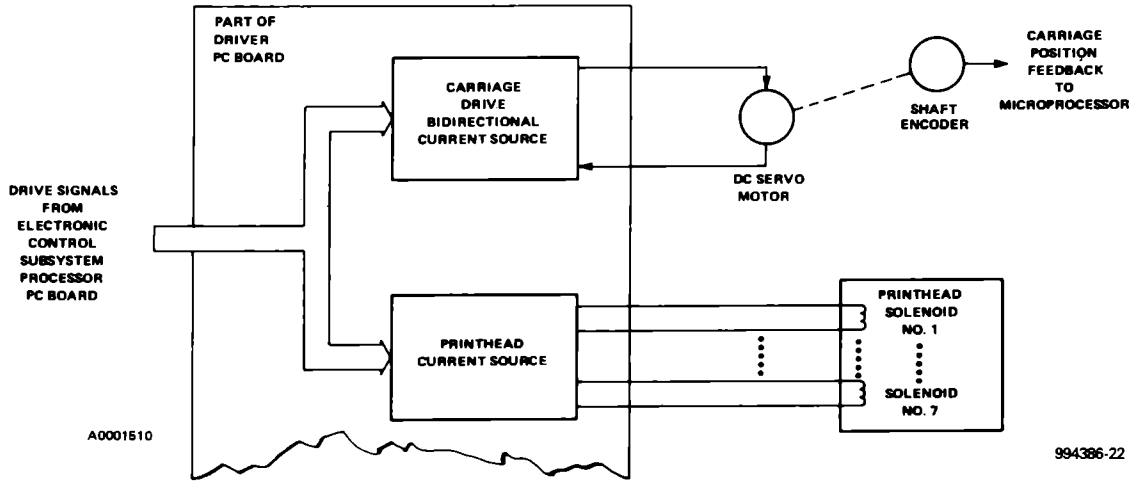


Figure 7-3. Printhead Carriage Subsystem Block Diagram

7.2.2.1 Dot Matrix Printing Mechanism. A dot matrix mechanism prints characters in a nine × seven dot pattern on paper through an inked ribbon. The Model 810 is a "smart", bidirectional, impact-type printer, and is capable of printing one original and up to five copies. The printhead is in continuous horizontal motion as the characters are being formed.

This mechanism consists of a printhead assembly, carriage drive, paper drive, and ribbon drive. (See Section 9 for location of these items.)

7.2.2.2 Dot Matrix Printing Mechanics. This paragraph describes how the printing mechanism prints characters in a nine × seven dot matrix (nine horizontally and seven vertically). The printhead carriage position and velocity are controlled by the microprocessor which maintains a record of the carriage position. The microprocessor determines this position by incrementing or decrementing a counter (depending on direction of carriage motion) for each output pulse from the encoder mounted on the shaft of the carriage drive servo motor.

Each character space is divided into 12 equal increments on the horizontal axis (8.33 mils wide). The character uses nine spaces with three spaces between characters. Figure 7-4 illustrates how the letter "E" is formed on the dot matrix. Note the seven horizontal grid lines (corresponding to the seven print wires) and five vertical columns. The

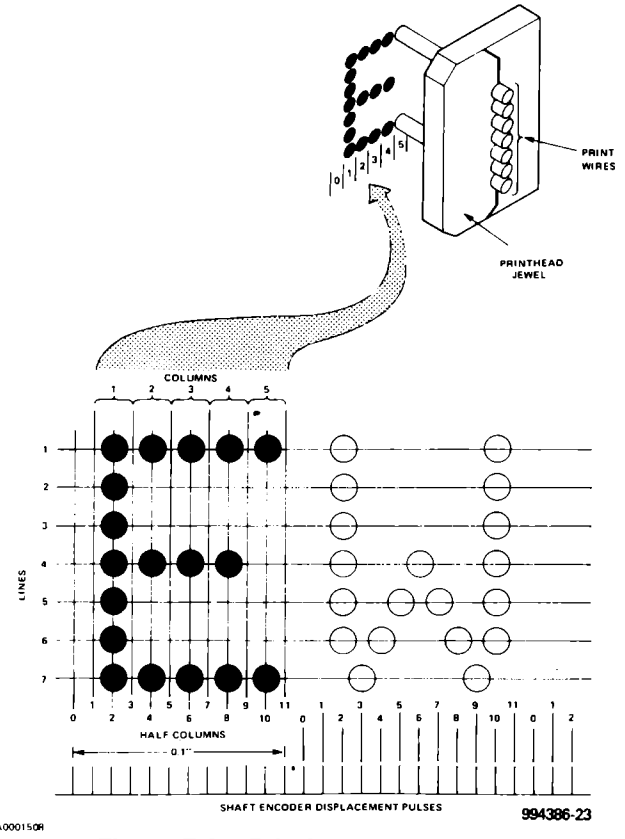


Figure 7-4. Printing the Letter "E"

five vertical columns are subdivided into half columns, providing a total of nine vertical columns.

The letter "E" begins in half-column 2 by firing all the solenoids. The first, fourth, and seventh solenoids are fired on half-columns 4, 6, and 8; and the first and seventh solenoids are fired on half-column 10 (thus forming the letter "E"). The next three half-columns are empty, and the letter "W" starts on half-column 2.

The printhead is in continuous horizontal motion when the solenoids are fired. The carriage generates an encoder pulse as each of the 12 space increments is passed. There are 12 encoder pulses per character (e.g., an encoder pulse is associated with each vertical column in Figure 7-4). Each pulse provides an interrupt to the byte from a ROM (which contains the dot pattern for that column). This pattern is then sent to the printhead drive circuits, which fire the solenoids required to form the desired character dot pattern. Due to recovery time, a solenoid cannot be fired on consecutive encoder pulses; it is limited to firing on every other encoder pulse.

For maximum efficiency, a carriage return is not used. Instead, the microprocessor examines the next line of data in the line buffer and calculates the distance from the present carriage position to either end of the next line. The microprocessor then commands the drive electronics to move the printhead carriage to the position of the first or last character in the next line (whichever is closer), and prints this line starting on the end selected.

7.2.2.3 Printhead Assembly. Figure 7-5 illustrates the printhead consisting of a frame and seven solenoids arranged radially around it. Each solenoid actuates a tungsten wire. The free end of the wires passes through a synthetic ruby wire guide at the front of the printhead. This guide spaces the wires to form a vertical one × seven column.

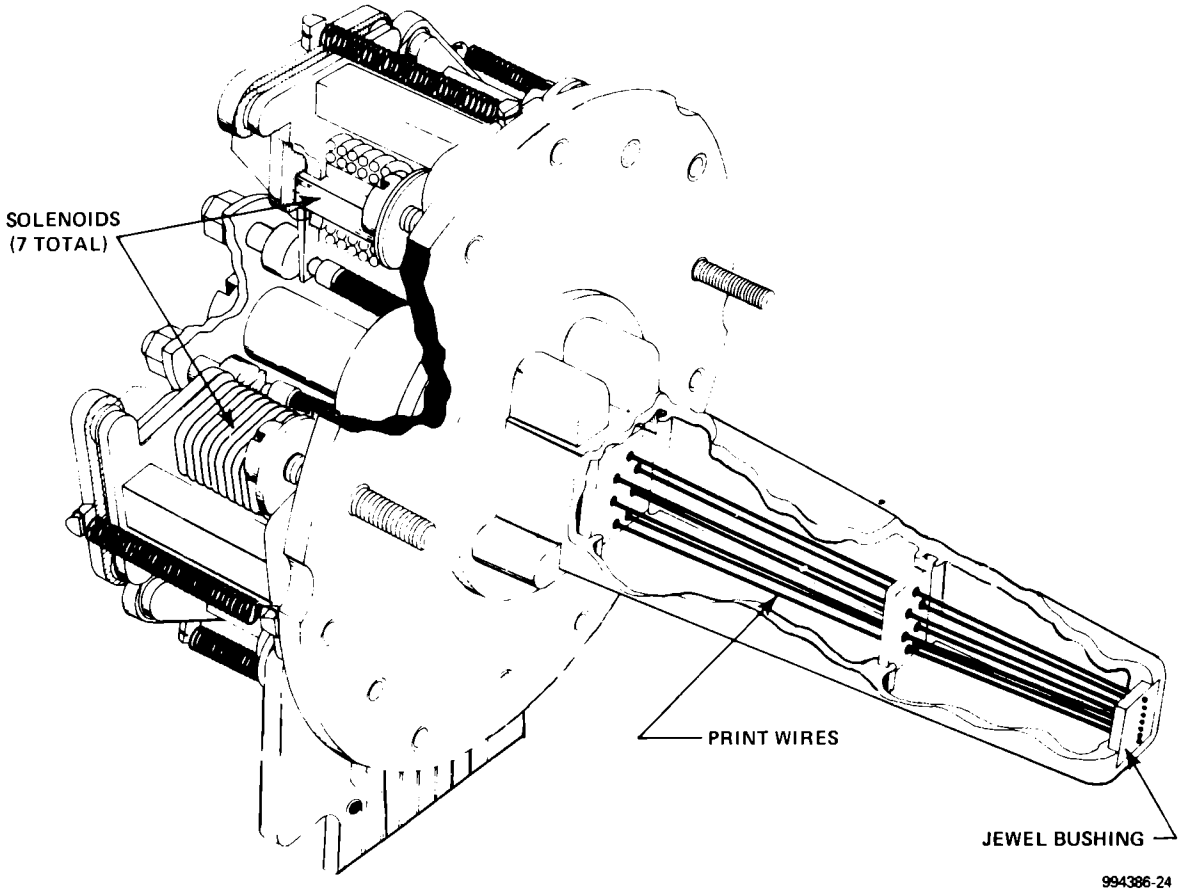


Figure 7-5. Typical Model 810 Printer Printhead Assembly

In operation, the solenoids drive the wires with sufficient force to print an impression on an original plus five carbon copies (standard 12-pound bond paper with 7½-pound carbons). The printhead operates at 900 Hz, resulting in a 150 character-per-second (cps) print rate. Continuous operation of this device is possible without forced air cooling.

7.2.2.4 Printhead Drive. These driver circuits provide drive current for the printhead solenoids. Drive signals from the Electronic Control Subsystem are fed to the printhead current switches (A1-A7). These switches provide current pulses whose sequence and duration are controlled by the microprocessor. Appendix K, Theory of Operation for the Driver Board, gives more detail.

7.2.2.5 Carriage Drive Assembly. The carriage drive is a closed-loop electromechanical assembly which properly positions the printhead as it prints each line of characters. The carriage supports the printhead assembly and is guided by rods attached to the printer frame (see Section 9 for location). These guide rods maintain proper spacing between the platen and the printhead as it moves across the page.

Bidirectional printing eliminates the need for a carriage return after each line. The Electronic Control Subsystem has a two-line buffer that examines the next line (after printing a line) to determine which direction should be used to print the next line. This achieves minimum carriage positioning time (hence the term "smart printer").

Maximum carriage travel is 345 mm (13.6 inches) with velocity control over the full range of travel.

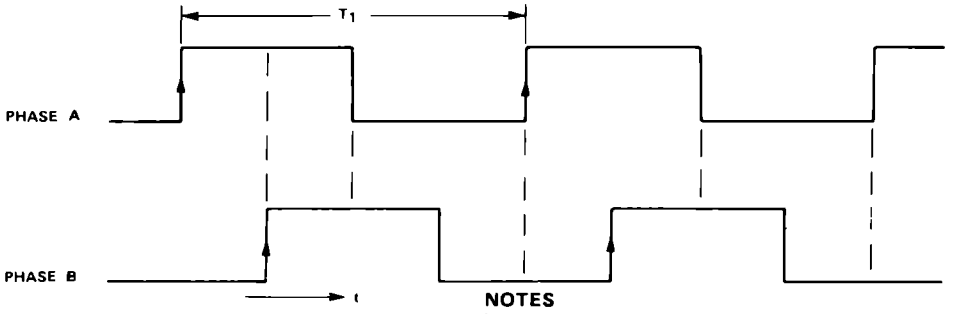
The carriage drive operates at character throughput rates up to 150 cps. A dc servo motor controlled by the microprocessor positions the carriage. An optical encoder on the motor shaft provides signals from which velocity, position, and direction of carriage movement are obtained.

7.2.2.6 Carriage Drive. The dc servo motor mechanically positions the carriage for printing. The shaft encoder attached to the rear shaft of the dc servo motor generates the pulse train used by the processor to determine the location of the printhead on the paper. This pulse train is also used to determine carriage velocity and direction of travel.

Operating modes of the carriage subsystem are initializing, forward or reverse printing, and forward or reverse slewing.

1. *Initializing Mode.* This mode is used during a power-up sequence or when changing from normal to compressed print modes. During initialization, the carriage is slowly moved to the left until it strikes a rubber bumper. The processor detects this condition through the loss of encoder pulses.

   This known physical location is stored by the processor and becomes the basis for determining future carriage location through incrementing or decrementing position counters when encoder pulses are received. Two encoder outputs that are in phase quadrature determine the carriage direction. These outputs are shown in Figure 7-6. The phase relationship between two signals determines the



NOTES

1. In normal print mode the encoder produces 288 pulses per revolution which equals a 1.8 kHz pulse train at normal print velocity of 15 inches per second.
2. In compressed print mode the encoder produces 475 pulses per revolution which equals a 1.8 kHz pulse train at compressed print velocity of 9.1 inches per second.

994386-25

Figure 7-6. Carriage Motor Shaft Encoder Phase Relationship for Left-to-Right Carriage Motion

direction of rotation. The time between encoder pulses (t_1) is inversely proportional to the carriage velocity. This can therefore be used by the processor to determine when to turn the motor on or off which helps regulate carriage velocity.

2. *Forward or Reverse Printing Mode.* In the forward or reverse printing mode, the carriage is accelerated to 381 mm (15 inches) per second for normal printing or 231 mm (9.1 inches) per second for compressed printing. A velocity profile of this mode is shown in Figure 7-7.

   During the time interval t_1 (Figure 7-7), the motor is driven from a constant-current, 3A source to produce a linear carriage acceleration of 25.40 meters (1000 inches) per second^2 (nominal). At time t_1 the motor drive current is reduced to 1.5A to change the acceleration rate to 127 mm (5 inches) per second^2 (nominal). At time t_2, the processor determines that carriage velocity is greater than required and turns off the drive current source. The motor coasts down to the regulating point, where the processor again turns on the 1.5A constant-current source. In this manner, the velocity is regulated at print speed during time interval t_3.

   A STOP command at t_3 reverses the current flow in the motor to decelerate the motor until t_4. At t_4 the motor is turned off and friction stops the carriage. Forward or reverse carriage velocity regulation cycles are identical except for direction of current flow in the motor.

3. *Forward or Reverse Slewing Mode.* The last carriage motion is the slew mode which is used to move rapidly over distances greater than two inches from the present carriage position to the next print position.

   The higher velocities in the slew mode are achieved by setting higher reference velocities in the processor program. Motor currents and acceleration rates are identical for the normal print mode. Since the acceleration rates are the same, the time required to reach slew velocity is 35 msec.

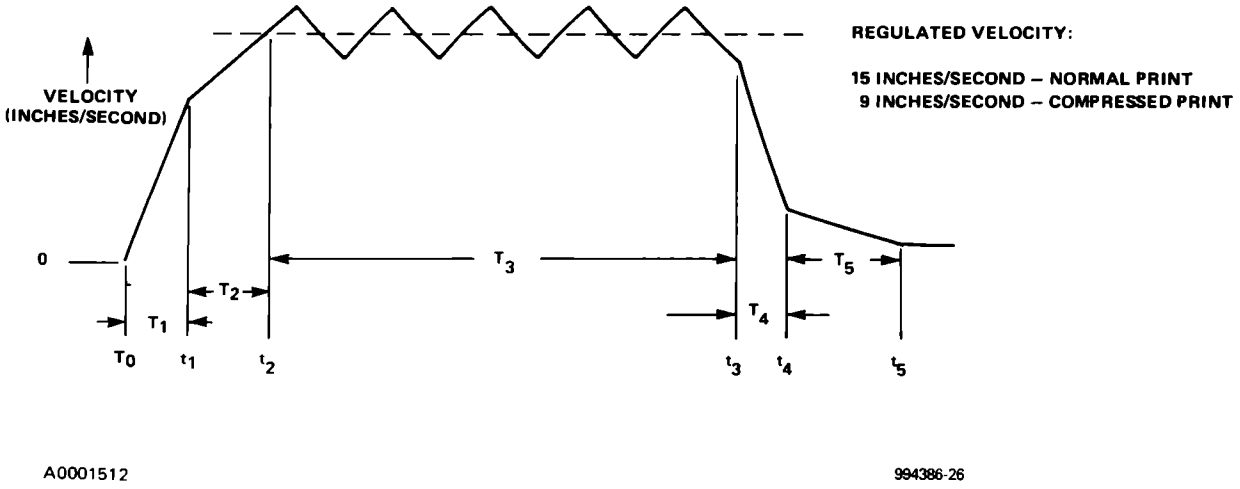


Figure 7-7. Carriage Velocity Profile in Print Mode

7.2.2.7 Paper Drive. This mechanism allows the form to be advanced through the printer in 0.014-inch increments. It consists of a stepper motor geared to the paper feed shaft which drives two pin-fed type paper tractors. This drive is mounted on the printer frame (see Section 9).

The operator may load paper either horizontally along the bottom rear of the printer or through a path entering vertically beneath the platen print surface. The FORM ALIGN ↑ and FORM ALIGN ↓ control panel switches allow the operator to align the form vertically with the printhead. The paper is driven by tractors that pull and guide the forms through the printer. These tractors are adjustable between widths of 3 to 15 inches and allow horizontal registration of the paper. Under control of the microprocessor, the paper drive advances the form through the printer in six lines per inch (1/6-inch steps) or eight lines per inch (1/8-inch steps).

The form thickness capacity is 0.053 mm (0.021 inch) maximum (sufficient for one original, five carbons, and five copies using standard 12-pound bond with 7.5 pound carbons).

A PAPER OUT sensor indicates to the microprocessor when the paper supply has been exhausted. When sensed, the microprocessor allows printing to continue until the end of the line is reached; then the control panel PAPER OUT lamp lights and a BUSY signal is sent to the transmitting device. Additionally, a bell rings five times to audibly call attention to the condition.

Paper can be loaded and the printer readied to print in less than 30 seconds. Power need *not* be turned off during paper loading; thus vertical format and horizontal tab information stored in the memory is not lost.

7.2.2.8 Ribbon Drive. This drive uses two standard spools (IBM type 1443 or equivalent) with the ribbon material and ink specified to be compatible with wire matrix printing. (Refer to Section 9 for location.) The ribbon has a minimum print capacity of seven million characters. The spools are located underneath the access door. The ribbon path is set at a slight diagonal to the printhead in order to print over as much ribbon surface as possible and obtain maximum life from the ribbon. The spools are driven by a dedicated motor which moves them through a swinging gear. The ribbon is reversed by changing the motor rotation direction when one of the eyelets (at either end of the ribbon) actuates a switch. The drive is turned off when printing ceases for one second.

7.2.3 Paper Feed Subsystem

This subsystem controls the paper motion in the Model 810 Printer. Paper advance is performed with a 15° variable-reluctance stepper motor geared to the paper feed tractor shaft. Each step of the paper advance motor moves the paper 0.36 mm (0.014 inch). Twelve steps achieve a full line advance in the six lines-per-inch mode. Nine steps move the paper a full line in the eight lines-per-inch mode.

Paper feed rate is seven inches per second in the slew mode. A line feed of eight lines-per-inch requires 25 msec. The six lines-per-inch mode requires 33 msec.

Limited reverse paper feed is possible via the unique electronic paper alignment system used on the Model 810. Reverse paper feeds are limited to one motor step (0.014 inch paper travel) each time the operator presses the FORM ALIGN ↓ switch.

The microprocessor controls the paper advance mechanism through the logic signals indicated in Figure 7-8. Proper sequencing and timing of the signals Phase A (PØA), Phase B (PØB), and Phase C (PØC) control the direction and rate of rotation. PSTEP and PFAST signals determine the magnitude of the constant-current source and the decay characteristics of the current wave forms. Paper slewing at 178 mm (seven inches) per second requires sequencing the phases at 500 pulses per second.

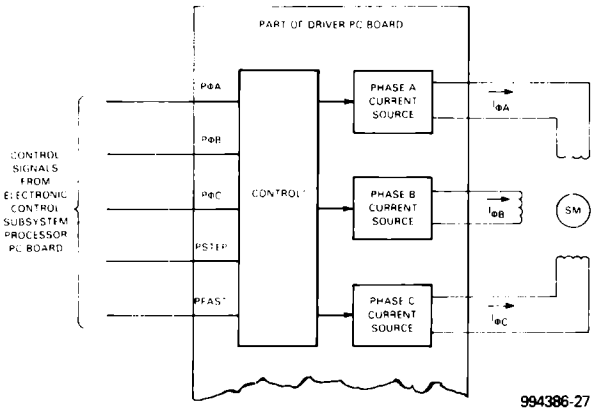


Figure 7-8. Paper Feed Subsystem Block Diagram

7.2.4 Power Supply

The power supply, TI Part No. 994534, provides the necessary regulated and unregulated voltage requirements for all printer subsystems. It also generates power-good and reset signals for initializing the microprocessor system when power is turned on. The power supply is physically distributed over the ac module, Motherboard, and power supply printed circuit board assembly (Figure 7-9).

The ac module (Figure 7-9) converts the ac line voltage to lower ac voltages required by the power supply board and fan. It also converts ac voltage to unregulated dc voltage used by other subsystems within the printer. The lower ac voltages are fed into the Motherboard and power supply board, where they are converted to various ac and dc voltages required to operate the printer. The following voltages are distributed to the subsystems through the Motherboard.

+28 Vac, 1A	+8 SW
+30 Vdc, 3A	−5 Vdc regulated, 10 mA
−75 Vdc, 0.5A	+12 Vdc regulated, 350 mA
+5 Vdc regulated, 4A	−12 Vdc regulated, 350 mA
	Power-Good/ Reset

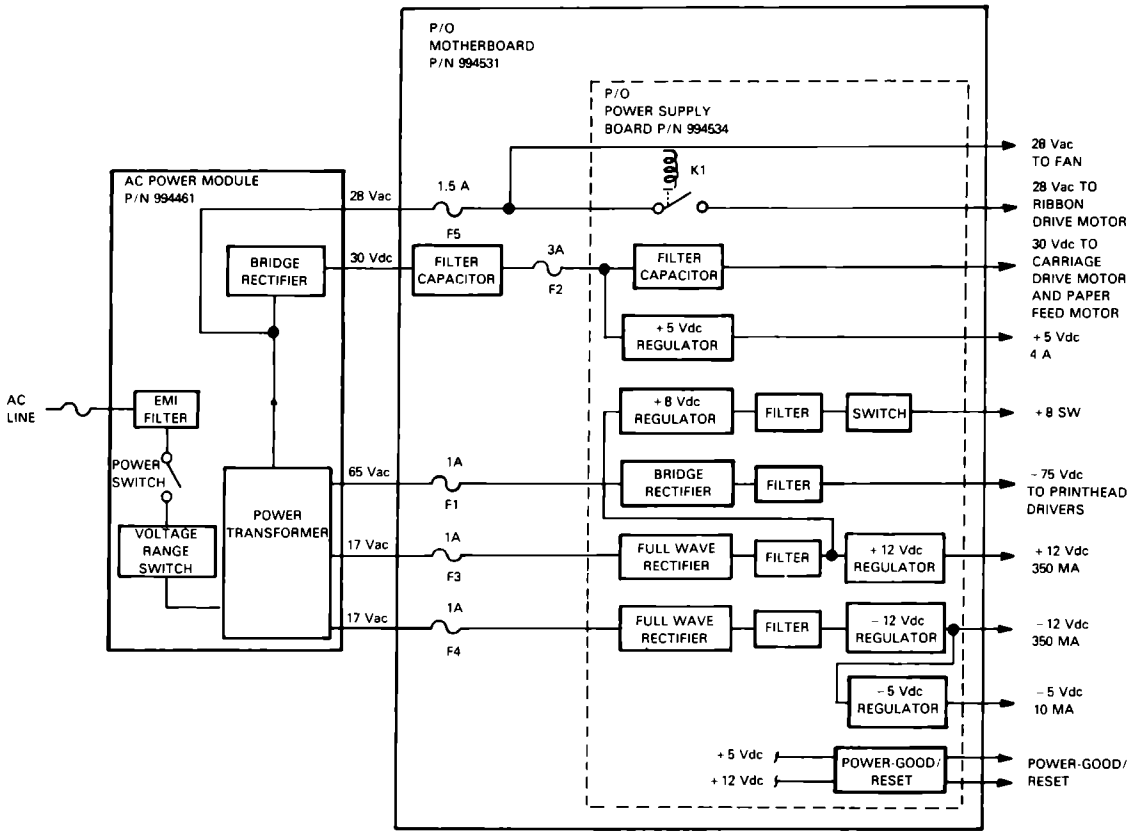


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Figure 7-9. Model 810 Printer Power Supply Block Diagram

The ac line is fused with either a 5.0 A fuse for 100 or 120 volts, or a 2.5 A fuse for 220 or 240 volts. (See Section 2 for information on line voltage selection.)

The secondary side of the power transformer has five fuses located on the Motherboard. Look at drawing number 994531, sheet 2, in Section 9 for location of these fuses or see Figure 5-3.

7.2.5 Line Buffer Option Interface

The Line Buffer Board, TI Part No. 994503, consists of a TTY interface, an EIA interface, a universal asynchronous receiver/transmitter (UART) which is the TMS 6011 (Appendix G), baud rate clock generator, control character decoder, 132-printable-character counter, BUSY signal generator, ACKNOWLEDGE signal timing logic, and software control which resides in 256 × eight bit PROM. (See Figure 7-10.)

The parallel data is stored in the FIFO (on the processor board) via the parallel data bus in two ways. If the parallel data comes in through the parallel interface port, it is stored in the FIFO by the data strobe signal (DTSTRB). If it comes from the UART, it is stored in the FIFO by the data ready signal (DR).

When the data is stored in the FIFO, the hardware control generates an acknowledge pulse to the parallel interface port and a data ready reset (DRR) signal to the UART. The control character decoder decodes carriage return (CR), line feed (LF), vertical tab (VT), form feed (FF), DC3, and delete (DEL) characters on the parallel data bus and sends a signal to the hardware control logic. The 132-printable-character counter generates a carry signal on the 132nd printable character. This carry signal is ORed with the signal from the control character decoder. The result sets the line buffer boards BUSY signal. The software control residing in the PROM implements the following hardware logic functions.

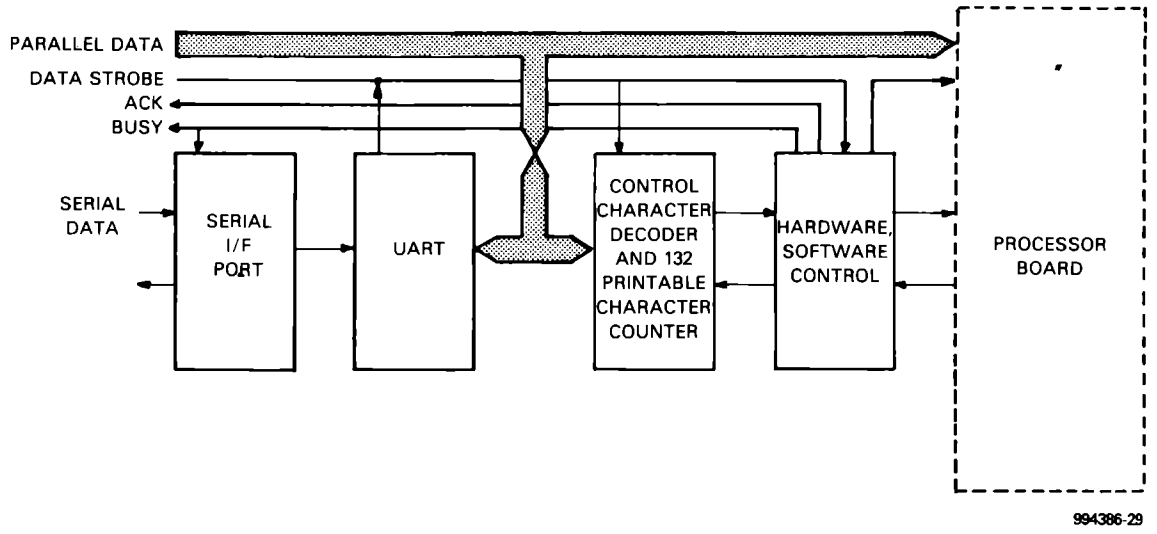


Figure 7-10. Simplified Line Buffer Interface Block Diagram

Incoming serial data from a sending device is fed into the UART through the EIA or TTY interface. The EIA serial data, when in use, overrides the TTY serial data. The serial data is converted into parallel data by the UART and buffered to the parallel data bus which then goes to the processor board.

The baud rate clock generator, which sets the UART receiver baud rate, is controlled by the software residing in the PROM. The UART and the parallel interface port have direct access to the parallel data bus.

- Clears the BUSY signal when the FIFO is empty
- Resets the 132-printable-character counter
- Sets the baud rate clock for the UART receiver

- Enables or disables the UART
- Sets the line width to 132 characters

7.3 THEORY OF OPERATION

This subsection presents a block diagram level discussion and circuit description at the printed circuit board level on the theory of operation of the Model 810 printer. Refer to the preceding subsection for printer subsystem level descriptions.

7.3.1 Overview

The Model 810 printer electronic subassemblies are contained on the ac power module, the Motherboard, and four printed circuit boards that plug into the Motherboard. The four boards include the processor board, the power supply board, the driver board, and the optional interface boards. The drawings in Section 9 show the physical location of these components, and Figure 7-11 illustrates their functional relationship.

NOTE

The major functional blocks at the subsystem level include the Electronic Control Subsystem, Printhead Carriage Subsystem, Paper Feed Subsystem, Power Supply, and the Line Buffer Option Interface. These blocks are described in subsection 7.2. Operation of control panel switches and indicators is described in Section 3.

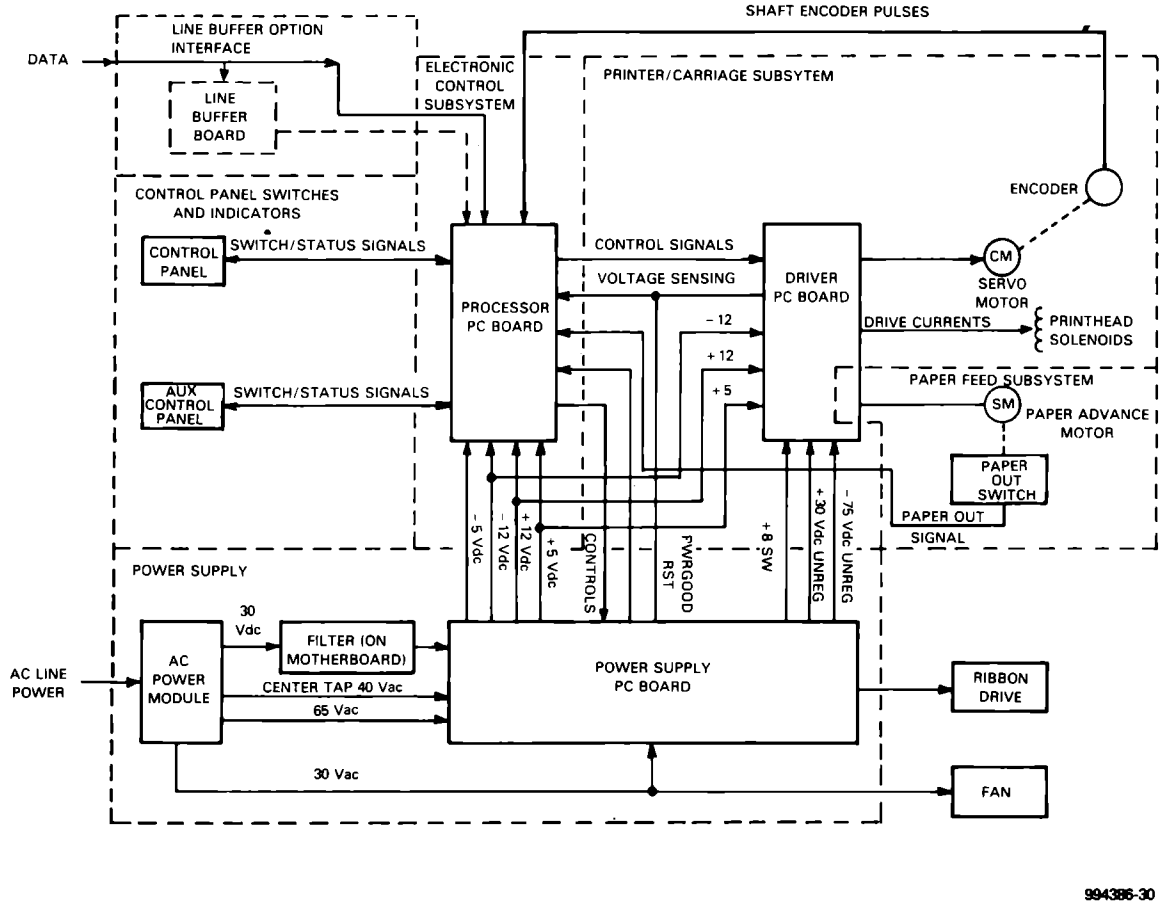
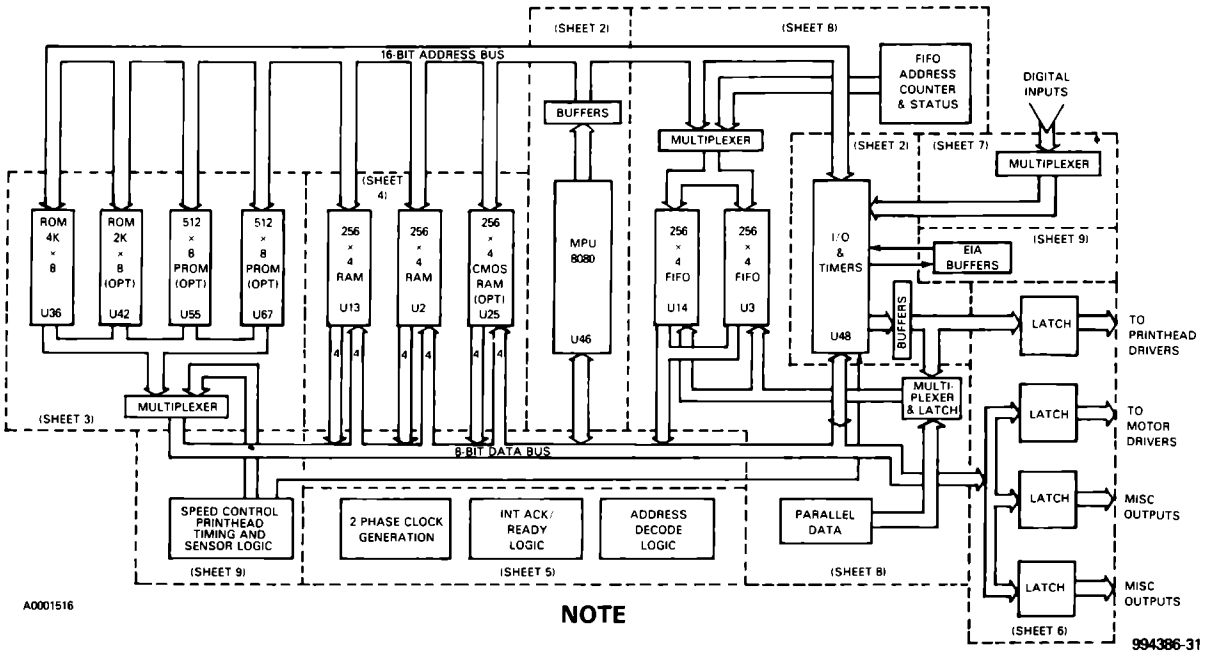


Figure 7-11. Model 810 Printer Simplified Electronics Block Diagram

The processor board (Figure 7-12) contains an 8080A microprocessor, a TMS 5501 I/O and timing device, RAM, ROM, and optional PROM memories. It also contains interface logic circuitry for interfacing with the control panels and driver board. The microprocessor and associated software or firmware programs control operations of the printer. The commands for them are received from the control panel switch settings, incoming data, control panel signals, or pulse feedback from the encoder. The microprocessor also generates the control and timing signals required by the driver board.

The power supply board supplies regulated +5 Vdc, −12 Vdc, and +12 Vdc for operation of both the processor and the driver boards. It also supplies +8 SW dc voltage, unregulated +30 Vdc, and unregulated −75 Vdc to the driver board. This board also generates power-good (PWRGOOD) and reset (RST) signals which indicate to the processor board that the regulated +5 and +12 volt supplies are above the minimum required levels. PWRGOOD also controls the +8 SW power to the driver board. Thus if PWRGOOD goes false (indicating an out-of-tolerance power supply), all of the power stages



(SHEET) numbers in the dashed-line blocks refer to the schematic 994247 sheet numbers in Section 10.

Figure 7-12. Processor PC Board, Detailed Block Diagram

The driver board contains the printhead, the carriage motor, and the paper feed motor driver circuits. These drive circuits receive control signals from the processor board and generate drive currents to the printhead, carriage motor, and paper feed motor.

The power supply provides all voltages (regulated and unregulated) necessary to operate the printer. Power is distributed to the printer through the Motherboard. The ac module provides 40 Vac center-tapped, 65 Vac, and unfiltered +30 Vdc to the power supply board, as well as 28 Vac to operate the cooling fan and the ribbon drive.

on the driver board are disabled—which prevents application of power to the motors and printhead during power-up or a power fault.

The bell and power control circuits for the ribbon drive motor are also located on the power supply board. Logic level signals from the processor board control the bell and ribbon drive.

7.3.2 Processor Board

The processor board, TI Part No. 994244, consists of an 8080A microprocessing system; serial and parallel communications interfaces; operator and

driver board interfaces; a carriage speed counter; and printhead, timing, and sensor logic. Figure 7-12 is a detailed block diagram of the processor board. The sheet numbers on the diagram refer to sheets of the detailed logic diagrams of the processor board, drawing number 994247, located in Section 10.

The processor board monitors all printer inputs. From these inputs, it also generates all necessary timing and control signals to effect data transfers, carriage motion, and paper motion, and to generate printable characters through the wire (dot) matrix printhead.

7.3.2.1 Microprocessor System. The microprocessor system consists of a Texas Instruments 8080A microprocessor (Appendix D), 256 bytes of RAM, 4K bytes of ROM, 1K bytes of PROM, a special-purpose TMS 5501 I/O and timing device (Appendix E), and a 256-character FIFO buffer.

The RAM provides memory workspace for the 8080A microprocessor. The RAM holds one line of 132 characters to be printed, provides up to 40 bytes of space for storing microprocessor register contents during interrupt cycles, and provides temporary storage for microprocessor flag registers.

During an interrupt cycle, the microprocessor register contents are stored in RAM (referred to as a "push-down stack"), which allows the microprocessor to use the internal registers while servicing the interrupt. When the microprocessor returns to normal operation, the pushdown stack is written back into the microprocessor register from RAM.

The ROM contains the dot patterns for printable characters as well as software or firmware programs—routines required to perform the various printer functions (e.g., generating the rotating character barberpole pattern during the self-test mode).

Optional PROMs are used for various language applications (Appendix C). The PROMs contain additional firmware which works with ROM-resident firmware to perform tasks required for other specific customer applications.

The TMS 5501 I/O and timing device receives all incoming serial data and converts it to parallel form. The 8080A firmware writes the data into the 256-byte FIFO buffer. The FIFO buffer stores the input characters while the printer is printing. See Appendix E for a detailed description of the TMS 5501 Multifunction Input/Output Controller.

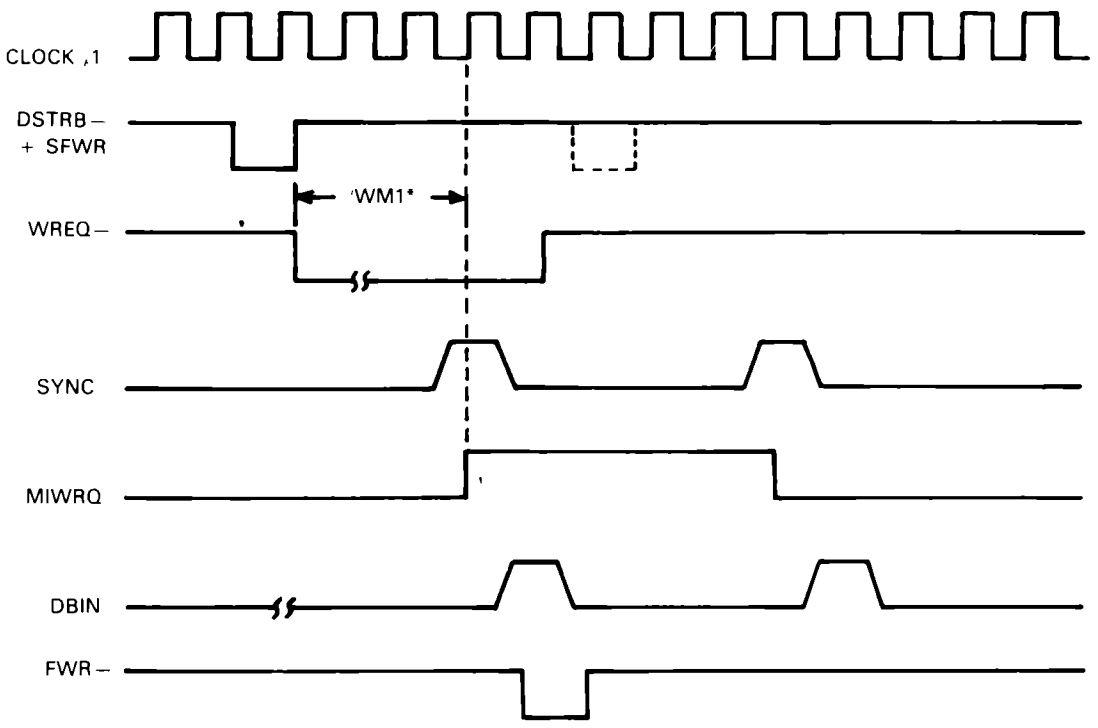
The 8080A communicates with all other components of the microprocessing system through a 16-bit parallel address bus and an 8-bit parallel data bus. When power is turned on, the microprocessor is initialized by the reset signal from the power supply. It then begins executing instructions starting at hexadecimal address 0000 (located in ROM). Paragraph 7.3.2.5 presents a description of the software and Appendix D is a detailed description of the TMS 8080A Microprocessor.

7.3.2.2 Communications Interfaces. The processor board monitors receive data from the serial EIA and the parallel data interfaces. Asynchronous serial data is received in accordance with ANSI Standard X3.16—1966 for character structure and parity sense, and ANSI Standard X3.15—1967 for bit sequence. Baud rate and serial/parallel operation are selected by the operator as described in Section 3. Whereas parallel data is written directly into the FIFO, serial data is routed through the TMS 5501 device, which converts it to parallel form. The 8080A program then writes the received character into the FIFO.

7.3.2.3 FIFO Buffer. The FIFO memory is implemented in hardware logic. It consists of an input register with selection of processor or parallel data (U5 and U16 on drawing number 994247, sheet 8, in Section 10), RAM memory (U3 and U14 on sheet 8), a counter to indicate the next available memory cell (U15 on sheet 8), up/down counters (U52 and U64 on sheet 8), and decoding circuits to remember the number of characters in the FIFO and to provide empty and full status signals. A write cycle is initiated by the parallel data strobe (DSTRB) or the serial FIFO write strobe (SFWR) clocking flip-flop (U73 on sheet 5). Figure 7-13 is a FIFO memory write cycle timing diagram. Storing of data in the FIFO is synchronized to occur during the microprocessor M1 or instruction fetch cycle in order to ensure that the FIFO is not being accessed by the 8080A microprocessor.

7.3.2.4 Printhead Carriage Control. The processor board generates signals for printhead carriage speed control, for vertical paper positioning, and for printing.

1. Carriage Positioning and Control. The microprocessor generates a carriage direction command (CMFWD), a motor on/off command (SCON), and an acceleration level control signal (ACC). These signals are active when low. A low level on all three causes the carriage to move forward (left to right) at high acceleration. The microprocessor tracks carriage position by counting sensor interrupts produced by the carriage motor encoder. A "zero" or reference position is established by initializing the carriage against a mechanical stop at the left margin.



*WM – = WAITING TIME FOR M1 CYCLE = 9 μsec MAX.

A0001517

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Figure 7-13. FIFO Memory Write Cycle Timing Diagram

2. Carriage Feedback Sensor System. As the carriage moves, its motor encoder produces a pair of pulsed signals with a 90° phase difference. These signals, TØA and TØB, are synchronized with clock signal CLK01A, and fed to a four-state controller to produce the count interrupt signal, SENSOR, and a direction indicator signal (FWT). (Refer to drawing number 994247, sheet 9, zones 4, 5, and 6). Figure 7-14 provides an encoder pulse state diagram. For normal printing the pulses occur at a rate of 120 per inch. With the compressed print option, a second pair of pulses at a rate of 198 per inch is also produced. The selection between these two is made by the signal COCHO and inverted OR/AND gates U23 on sheet 9, zones 7 and 8.

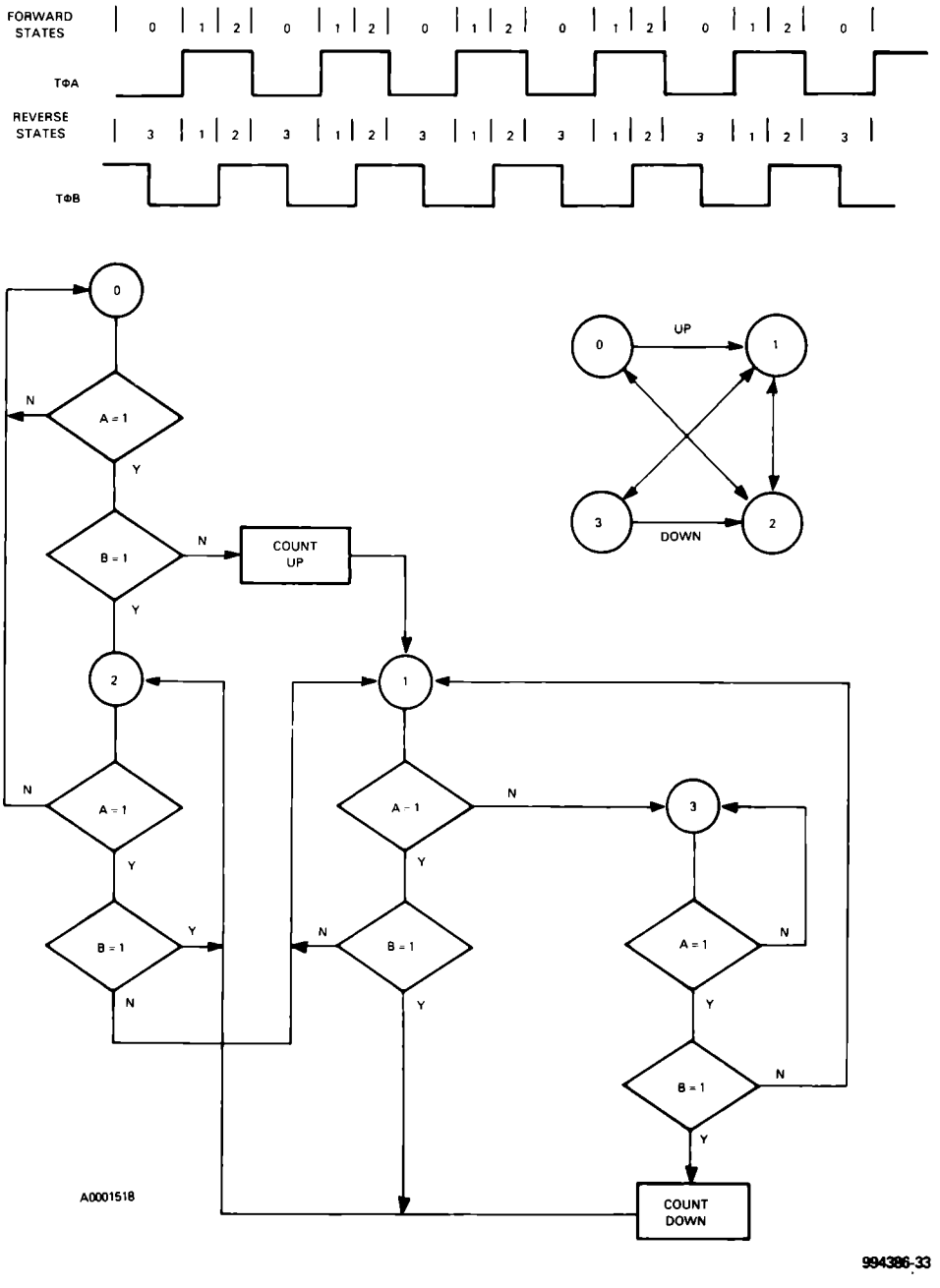


Figure 7-14. Carriage Motor Shaft Encoder State Diagram

3. Carriage Speed Control. The microprocessor sets the control signal (SCON) by comparing the actual speed measured by a reference counter (U44 on sheet 9) to a desired value. If the speed is too low, SCON is turned on (low). If the speed is too high, SCON is turned off. Counter U44, when enabled, counts with a resolution of 8 microseçonds. When a maximum count of 252 is reached or a sensor interrupt occurs, the counter is stopped by making CTEN low. The value stored in the counter is read by the microprocessor as part of the sensor interrupt routine which generates the signal RDCTR. This signal produces a counter reset (CLRCTR) pulse which enables the counter again on the next clock (CLK01). Since the sensor interrupt to read counter time is constant, the value of the reference counter is proportional to the time between sensor interrupts. Refer to the speed counter timing diagram in Figure 7-15.

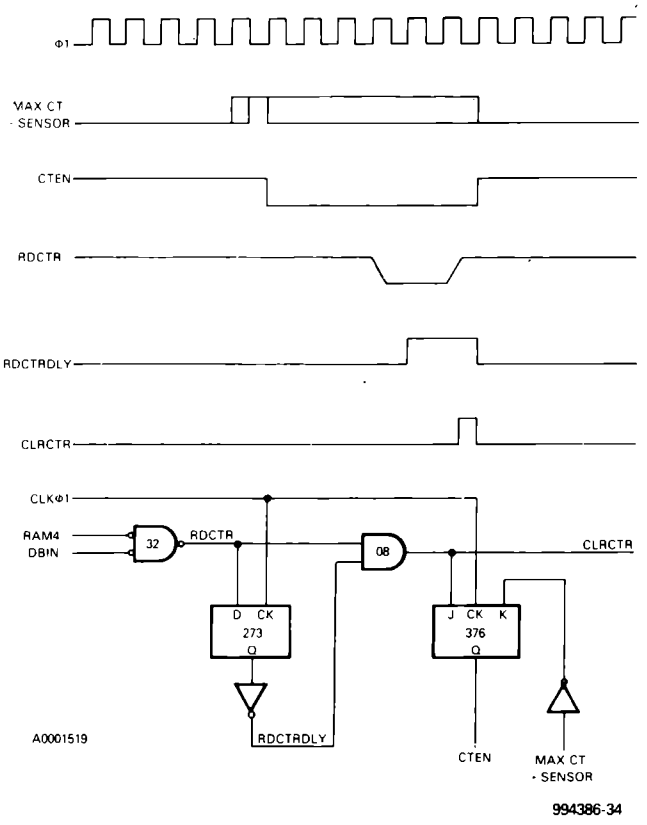


Figure 7-15. Carriage Speed Control Counter Timing Diagram

4. Character Printing. Figure 7-16 illustrates that the space allotted for printing each character is divided into twelve equal increments. Three of the increments space between characters when no commands are issued to the printhead solenoid drivers. Following the remaining nine sensor interrupts, the microprocessor transfers the appropriate dot pattern from the ROM to the printhead control latch (U28 on sheet 6) via signal CNTLI. This signal also clocks flip-flop U73 on sheet 5 producing a low on the printhead control signal, PHCTL, enabling the outputs of the printhead control latch. PHCTL returns to a high level when the reference counter reaches a count of 56 or 448 μsec after the microprocessor reads the reference counter. Since the CNTLI signal occurs about 45 μsec after RDCTR, the

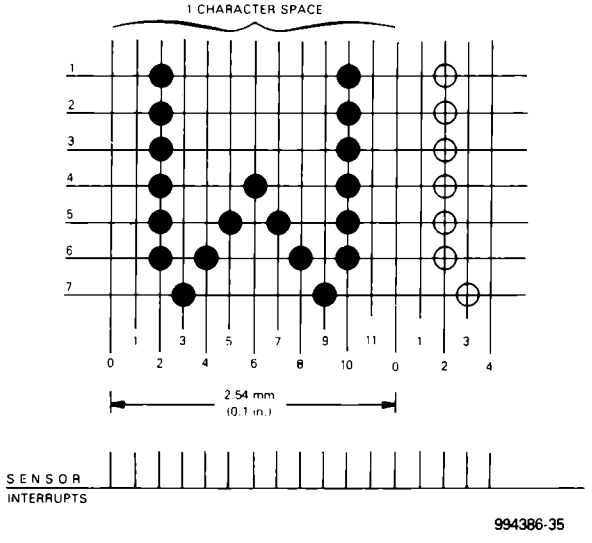


Figure 7-16. Forming the Character "W"

resulting solenoid control pulses are approximately 400 μsec in duration. Formation of the character "W" is illustrated in Figure 7-16. A complete timing diagram of one solenoid for both forward and reverse motion is shown in Figure 7-17.

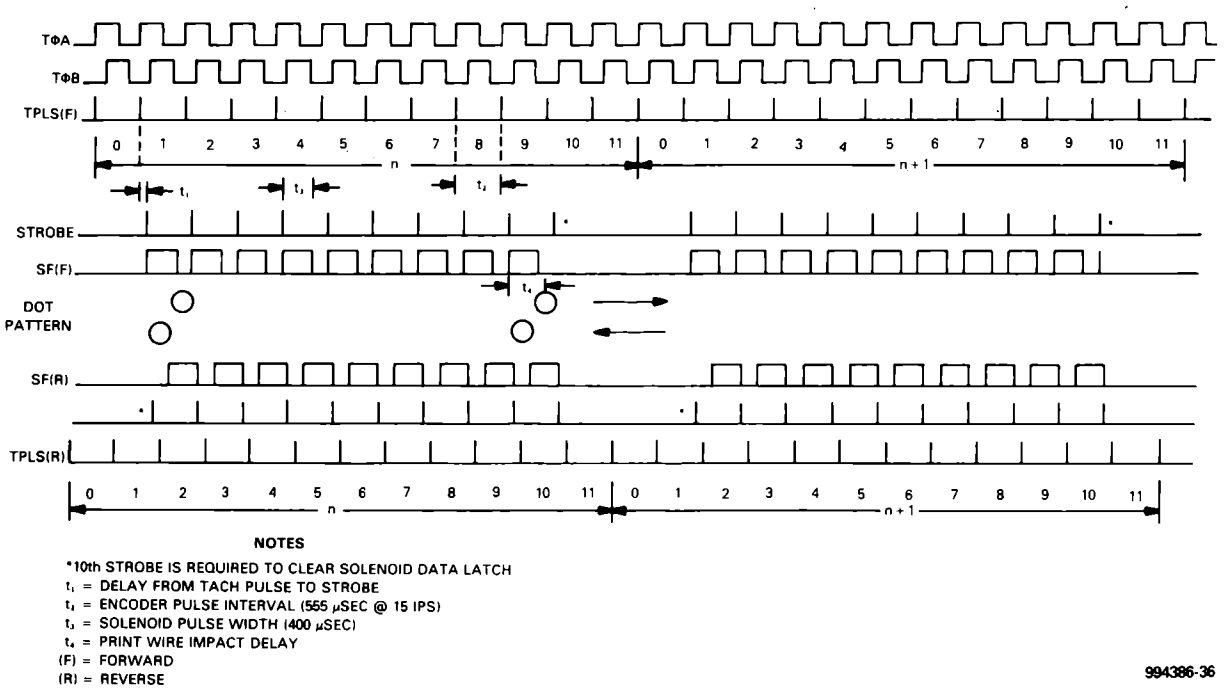


Figure 7-17. Printhead Solenoid Timing Diagram

7.3.2.5 Software. When power is applied to the printer, the 8080A is reset to hexadecimal address 0000 by the reset (RST) signal from the power supply. The microprocessor then begins executing instructions stored in ROM to perform the following tasks.

1. Clear RAM.
2. Initialize flags, states, constants, and variables.
3. Clear the TMS 5501 device and unmask interrupts.
4. Initialize the control latches and turn off ERROR, PAPER OUT, and BUSY lights.
5. Start the 24 msec fail-safe timer.
6. Align the stepper motor to phase A.
7. Align the carriage to the left bumper.
8. Initialize printer options.

The CPU then moves to the NORMAL or TEST mode, depending on the position of the control panel mode switch.

1. Background Loop and Major Subroutines (NORMAL mode). In NORMAL mode the microprocessor continues to loop through the background software waiting for an interrupt. The major subroutines in this loop initiate tasks such as paper motion, carriage motion, and printing. These

tasks are then completed by interrupt-driven software with the microprocessor returning to the background loop during spare time. (Refer to Figure 7-18, the Normal Print Mode Flowchart.)

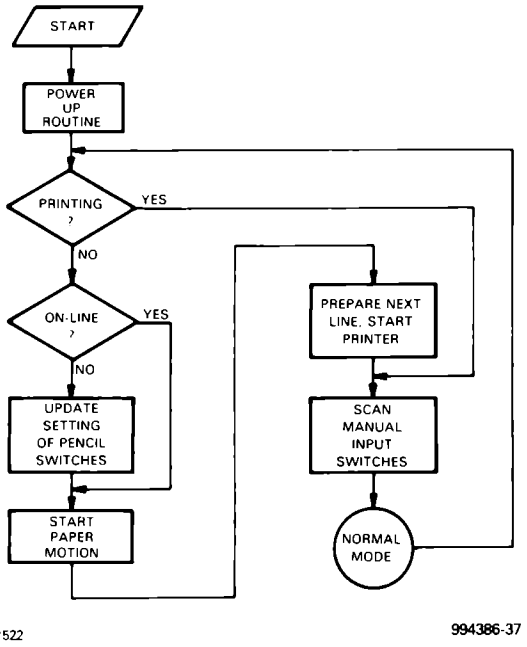


Figure 7-18. Normal Print Mode Flowchart

a. SCAN and IMPLEM. The SCAN subroutine reads the control panel switch and stores any inputs for implementation (IMPLEM subroutine) when printing of the current line is completed or immediately if the printer is not busy.

b. DOPMC. The DOPMC subroutine initiates any paper motion indicated by a character received over the line (LF, CR, VT, FF, or DC3). The actual paper motion is an interrupt-driven sequence handled by Timer 3 software.

c. E100. During the time required to complete paper motion, the E100 subroutine is called to prepare the next line for printing. E100 handles all characters with a series of accept states which select characters as printable and control, or as characters which alter the operating characteristics of the printer. Table 7-1 lists the accept states and the

Table 7-1. Printhead Subroutine E100 Accept States

State	Function	Sequence
ACPTS1	Normal state; handles control and printable characters	
ACPTS3	Escape handler	ESC
ACPTS3	Substates:	
	Go to 6 lines per inch	ESC, 4
	Go to 8 lines per inch	ESC, 5
	Go to 10 characters per inch	ESC, 6
	Go to 16.5 characters per inch	ESC, 7
ACPTS4	Horizontal tab to address	DC4, CHR
ACPTS5	Set vertical tabs	ESC, 1, CHR, ... CHR, NUL
ACPTS6	Set form length	ESC, 2, CHR
ACPTS7	Set horizontal tab	ESC, 3, CHR, ... CHR, NUL
ACPTS8	Vertical tab to address	DC2, CHR
ACPTS9	Change column count	ESC, :, CHR
ACPS10	Store VFU channel	ESC, 8, CHR
ACPS11	Recall VFU channel	ESC, 9, CHR

sequence of characters required to reach them. Figure 7-19 is a diagram of the accept states. E100 also arranges characters in the print buffer for the next line to be printed, computes the best direction and speeds for the carriage to reach the printing start point, and initiates carriage motion when paper motion is completed. Carriage motion and printing are then handled by interrupt-driven software (Sensor-Trap 2).

d. BAUDFX. If the printer is offline in the NORMAL mode, the microprocessor loops through the BAUDFX subroutine to update the pencil switch inputs on the control panel.

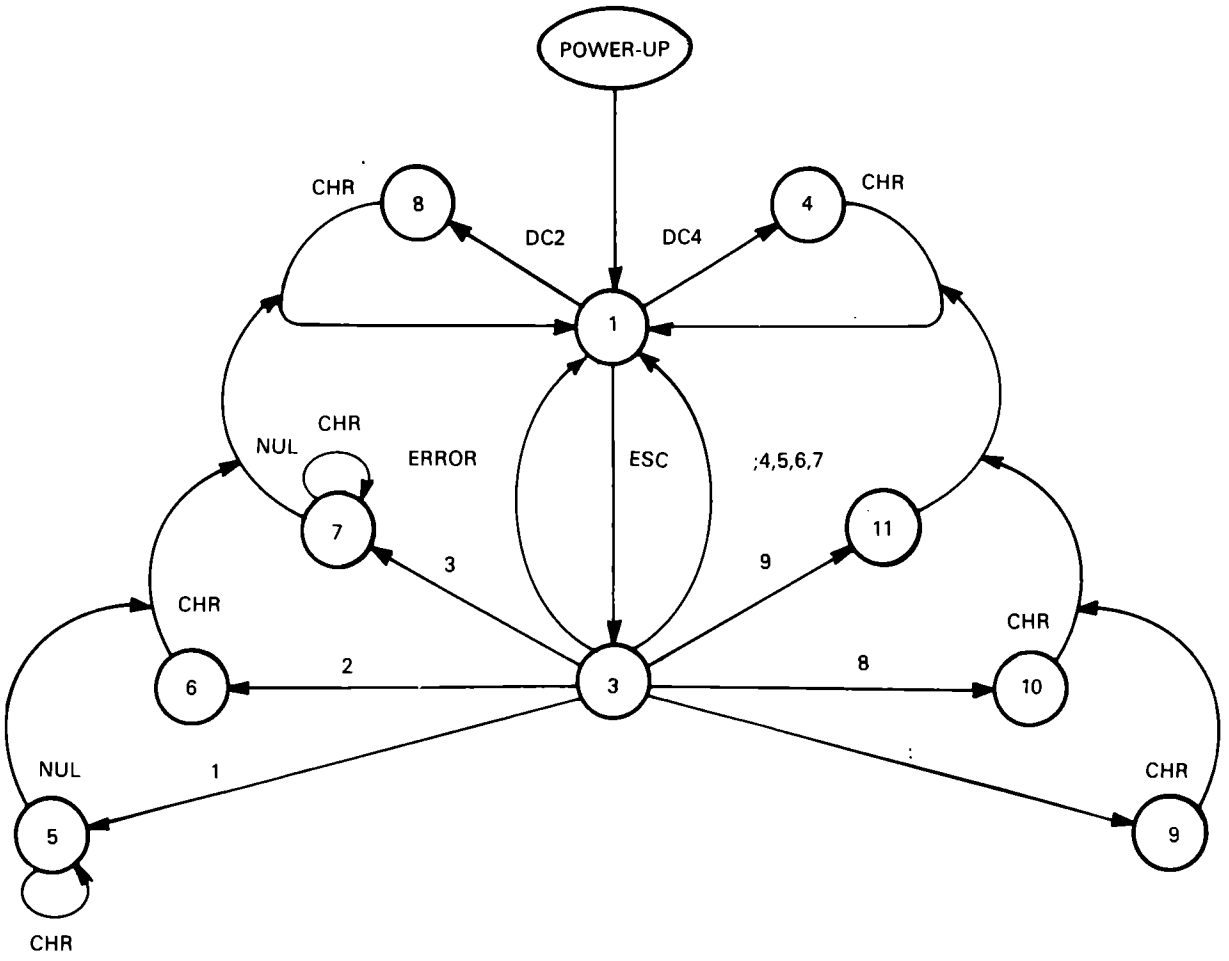


Figure 7-19. Printer Subroutine E100 Accept States State Diagram

2. Test Loop (TEST mode). In the TEST mode the microprocessor handles manual format inputs offline. The form length and vertical tabs may be altered and the manual Save and Recall switches for the VFU option are also active in this loop. Online in the TEST mode, the microprocessor uses the SCAN, IMPLEM, DOPMC, and E100 subroutines to print a rotating barberpole test pattern and also handle manual inputs. (Refer to the Test Mode Flowchart, Figure 7-20.)

3. Interrupt-Driven Software (Sensor-Trap 2). The sensor interrupt software controls all carriage motion, speed, and printing. Table 7-2 lists the function of each of the 12 carriage states and their maximum ex-

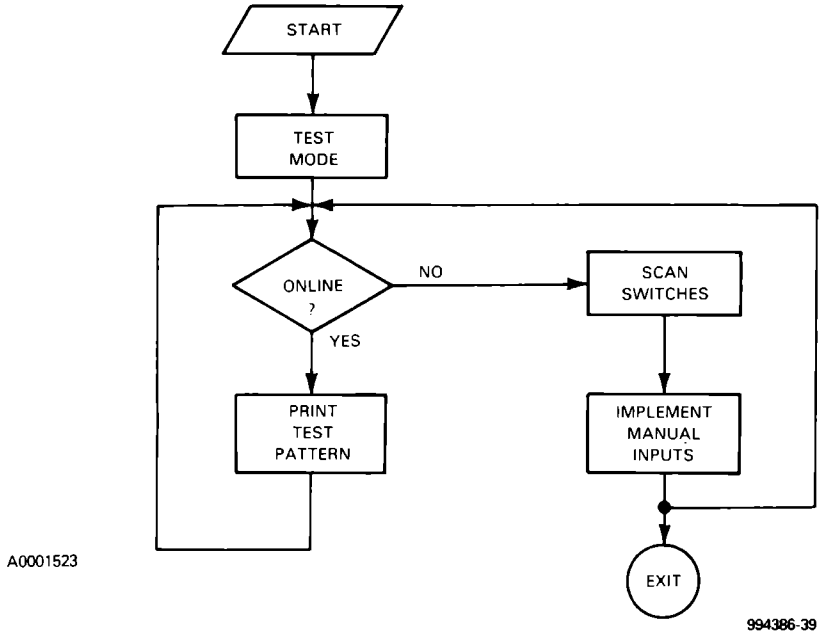


Figure 7-20. Test Mode Flowchart

Table 7-2. Carriage State Maximum Software Execution Times (Microseconds)

State	Standard Option	Full-ASCII Option	Katakana Option
CARST0 - STOP	148.5		
CARST1 CREEP	217		
CARST2 APPROACH START OF PRINTING	424	487	507.5
CARST3 PRINT	392	455	475
CARST4 SLEW	152		
CARST5 - DECELERATE TO PRINT SPEED	187		
CARST6 DECELERATE TO STOP	240		
CARST7 - BACK OFF	246.5		
CARST8 - DECELERATE AND REVERSE DIRECTION	218		
CARST9 - INTERIM	158		
CARS10 - IGNORE	192		
CARS11 - UPDATE CALCULATIONS	111.5		

ecution time. Table 7-3 lists the carriage motion reference speeds. A carriage state diagram is shown in Figure 7-21.

Table 7-3. Carriage Motion Reference Speeds

Reference	State	Speed (Inches/Second)
PRINT	CARST 2, 3	13.1
PRINT2	CARST 2,3	14.5
SLEWS	CARST 4	39.2
SLPRIN	CARST 5	16.9
BAKCRP	CARST 1, 7	5.5
STOPRF	CARST 6	9.4

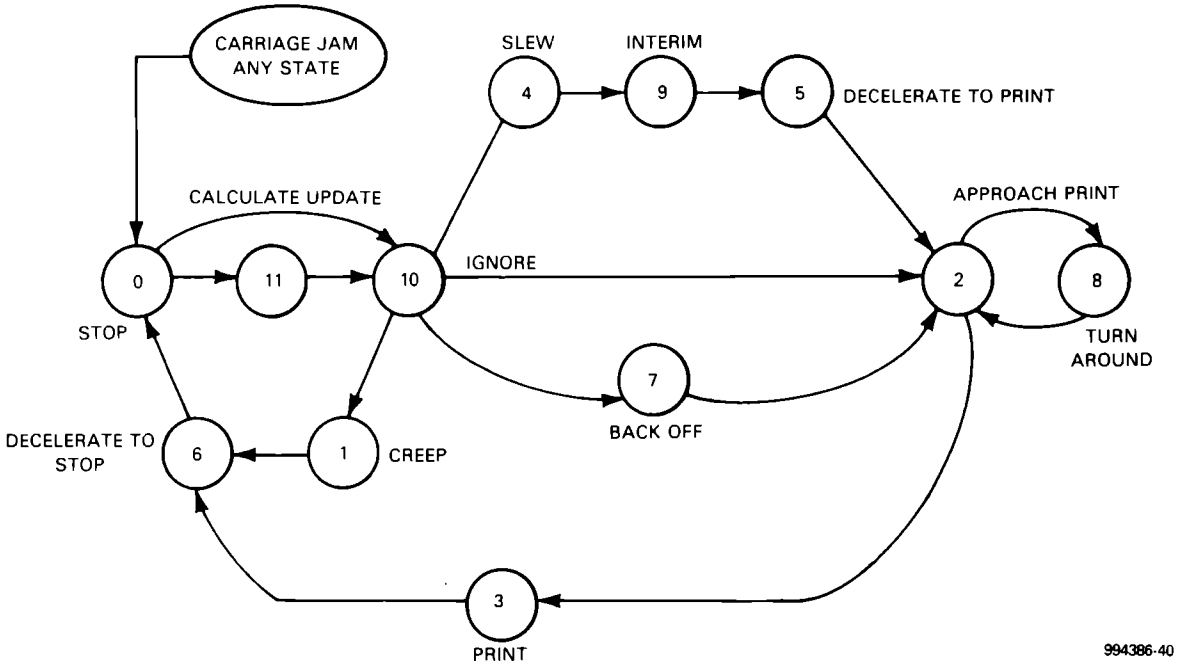


Figure 7-21. Printhead Carriage State Diagram

4. Timer 3—Trap 3. The Timer 3 interrupt software controls the stepper motor, all paper motion except vertical alignment, and long and short time delays. Four Timer 3 modes handle the following functions:

   Mode 0—Last 10-msec step of any paper movement
   Mode 1—All paper movement except the last step
   Mode 2—Time delays less than 16 msec
   Mode 3—Time delays greater than 16 msec

5. Serial Data Input—Trap 4. Serial data arriving in the receive buffer of the TMS 5501 is removed and stored in the FIFO.

6. Fail-Safe Timer or Timer 4—Trap 6. The fail-safe timer is used to shut off the carriage motor if an obstruction prevents sensor interrupts from occurring for longer than 24 msec during printing. Timer 4 also controls the error bell and blinking light during a carriage jam and, during normal operation, shuts off the ribbon drive if no printing occurs for one second.

7.3.3 Driver Board

This board, TI Part No. 994528, may be divided into three areas: printhead driver circuits, carriage motor circuits, and paper feed motor circuits (Figure 7-22). All drivers are constant-current switching regulators. Power for the carriage driver motor and paper feed motor is derived from the +30 Vdc supply. Power for the printhead solenoids is derived from the −75 Vdc supply. For the driver board, Part No. 994322, look at Appendix K.

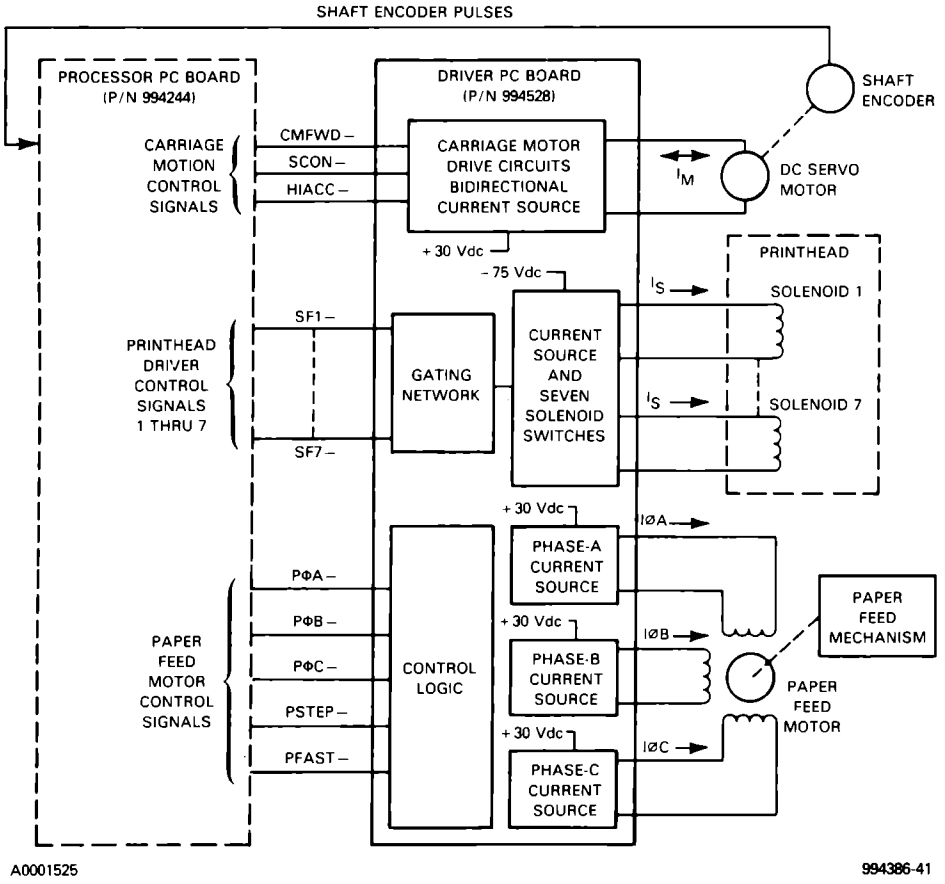


Figure 7-22. Driver PC Board Block Diagram

7.3.3.1 Printhead Driver Circuits. These circuits provide current pulses of the proper magnitude for excitation of the print wire solenoids. The sequence and duration of the pulses are defined by the microprocessor, which provides active low-level logic input signals $\overline{SF1}$ through $\overline{SF7}$ to the printhead driver circuitry (Figure 7-22). Driver stages A1 through A7 act as on/off switches and current sensors for each of the seven printhead solenoids. A1 through A7 contain switching transistors Q12 through Q72 (e.g., A1 contains Q12, A2 contains Q22, etc.) which are controlled by active low-level logic inputs ($\overline{SF1}$ through $\overline{SF7}$) from the microprocessor. The simplified schematic of the printhead driver in Figure 7-24 shows only one of the seven drive stages A1 through A7 (drive stage is enclosed by dotted lines). The seven drive stages are connected in parallel, with each logic signal $\overline{SF1}$ through $\overline{SF7}$ controlling its respective printhead solenoid switch Q12 through Q72.

Power is supplied to the printhead from the unregulated −75 Vdc bus by the transistor switch Q106. The +8 SW supply must be present to supply drive for Q106. Because the +8 SW sup-

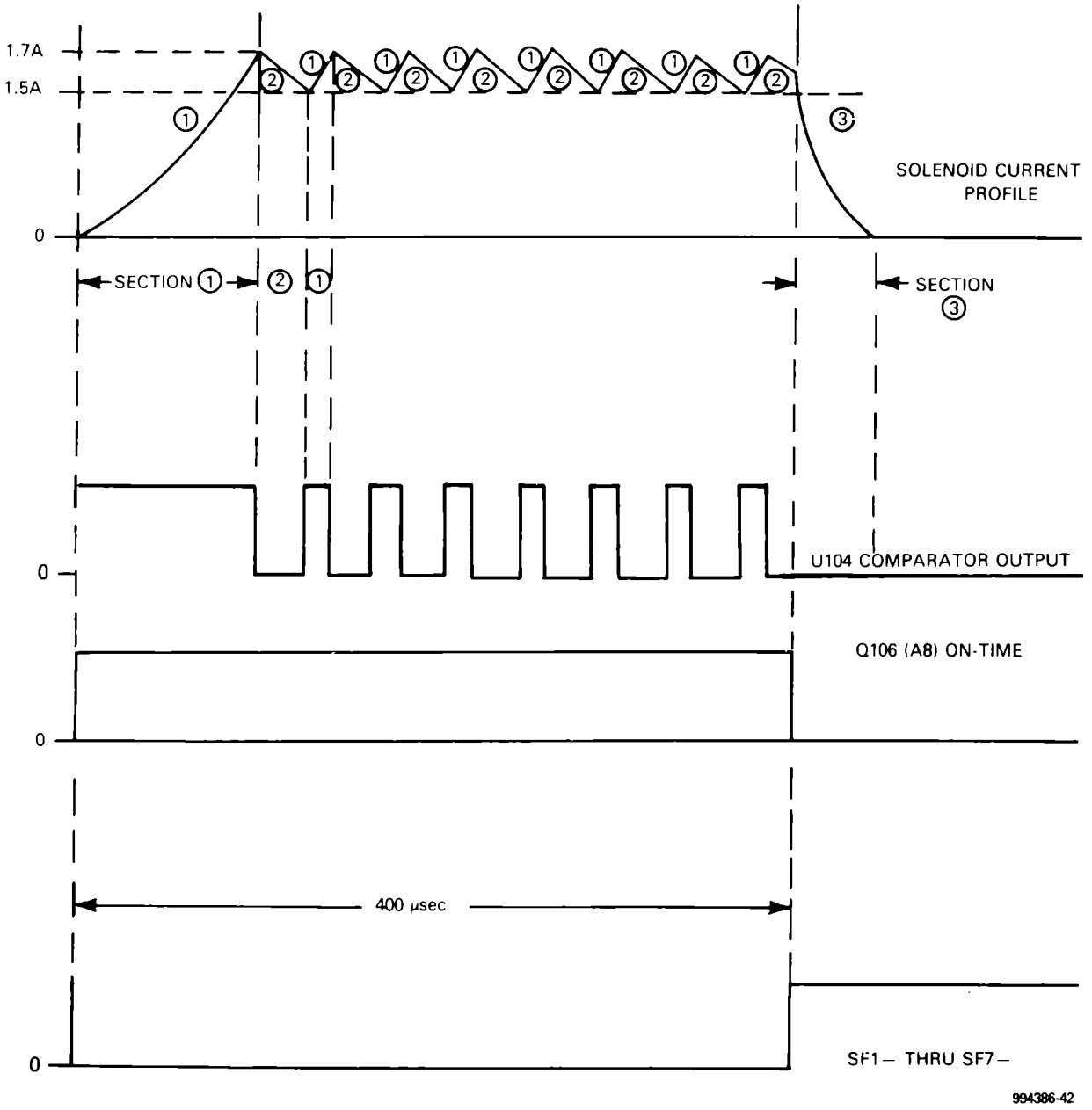


Figure 7-23. Printhead Solenoid Current Pulse Profile

ply is present only when PWRGOOD is true, firing of the printhead needles will be inhibited during power-up and power-down sequences or during times of marginal logic power conditions.

The switching action of the current regulator Q106 and the driver stages A1 through A7 combine to generate the solenoid current profile illustrated in Figure 7-23. When one or more of the input signals SF1 through SF7 is activated by the microprocessor, the respective transistors Q12 through Q72 and the current regulator transistor are switched on. Current begins to flow from −75 V common, returns through the selected drive stages and Q106 to the −75 V supply. The current through the selected printhead solenoids rises at a rate determined by the solenoid inductances (Section 1 of Figure 7-23). When the voltage across the sense resistors, R11 through R71, becomes more negative than VREF, the reference voltage to the comparator U104 turns Q106 off. The solenoid currents then begin to decay through the sense resistor drive stage switch Q12 through Q72 and CR101. The comparator allows the current to fall approximately 0.25 amperes before the comparator U104 turns Q106 on again (Section 2 of Figure 7-23). The current oscillates in this mode, Q106 switching on and then off, for the duration of the inputs (SF1 through SF7). Because of the parallel connection of the driver stages and the sense resistors, the switching regulator will track the solenoids which are rising the fastest and decaying the slowest.

When the input signals from the microprocessor (SF1 through SF7) become high, the driver stages and current regulator transistors switch off. Then current in the printhead solenoids is returned to the −75 V supply through CR14 through CR74 and CR101. The resulting current decay in the solenoids is shown in Section 3 of Figure 7-23.

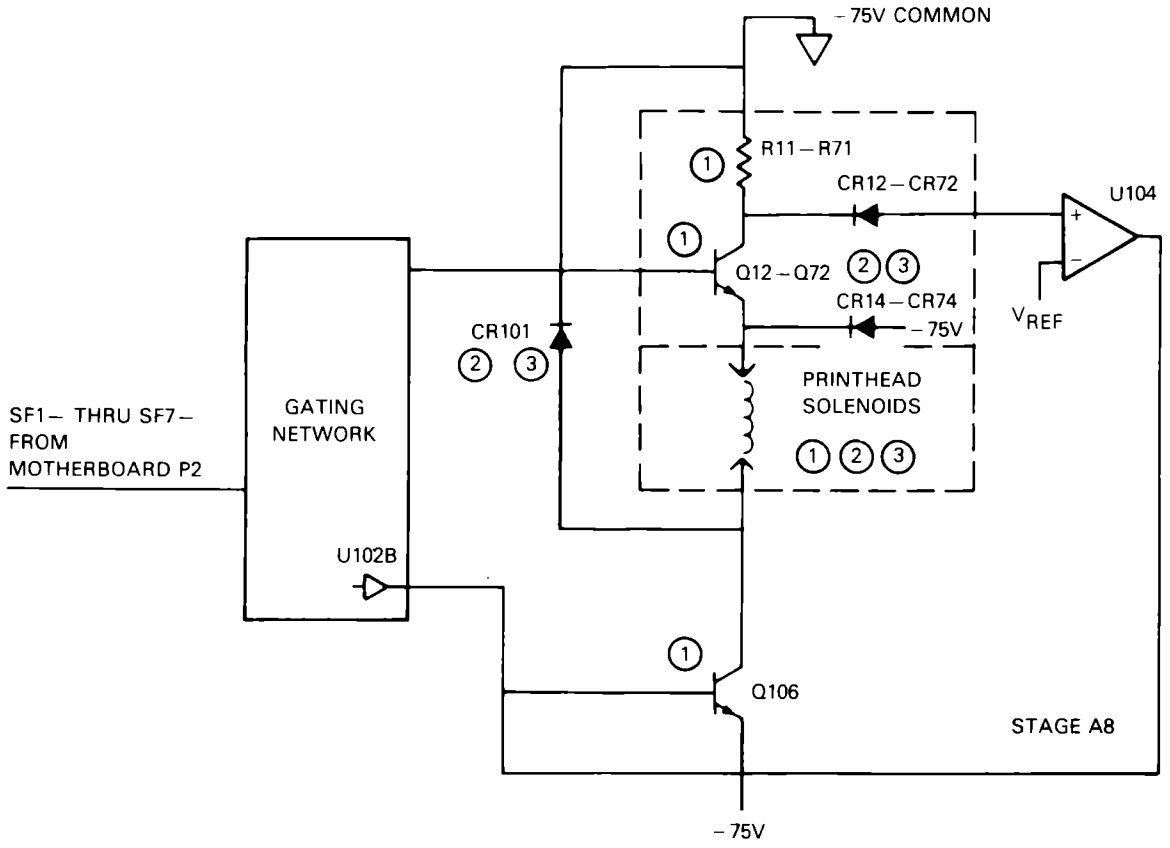


Figure 7-24. Printhead Power Driver Simplified Schematic

994386-43

7.3.3.2 Carriage Motor Driver Circuit. This circuit is a bidirectional, two-level, regulated current source. "Bidirectional" describes its ability to drive the carriage in either direction by reversing motor current direction. The high-level current setting is used during periods when high acceleration or deceleration rates are required, such as starting from rest, accelerating from print speed to slew speed, decelerating from slew to print speeds, or stopping from print speeds. The low current setting is used during the print speed or slew speed regulating mode to minimize velocity variations during these phases of operation. With constant current motor drive, carriage acceleration is constant.

Nominal acceleration values for the two levels of current are:

Level	Motor Current Amperes	Acceleration Meters/Sec²	Deceleration Meters/Sec²
Hi (ACC– = 1)	2.85 ± 5%	25.4	38.1
Lo (ACC– = 0)	1.43 ± 5%	12.7	25.4

These values allow the carriage to reach print speed (15 inches-per-second) in 15 msec, or slew speed in 35 msec.

The carriage motor drive control signals from the processor board (Figure 7-25) are:

CMFWD– A low on this line sets direction of current flow in the carriage motor to produce forward carriage motion (left to right)

SCON– A low on this line turns on the motor current

ACC– A low on this line sets the motor current to the high acceleration value (2.85A nominal).

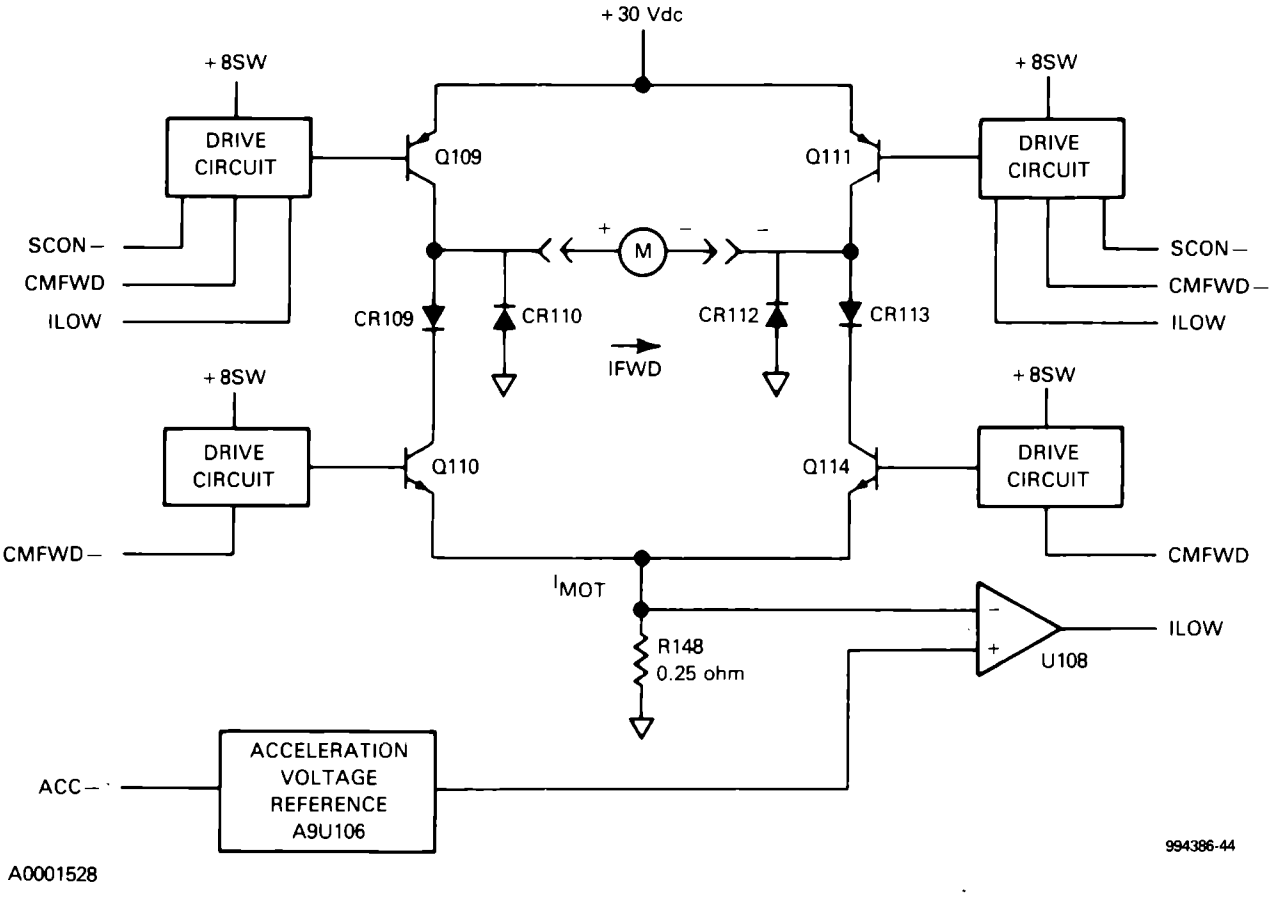


Figure 7-25. Printhead Carriage Driver Simplified Schematic

The basic circuit of the carriage motor driver is a switching mode current regulator which operates from the unregulated +30 Vdc bus. The main components are illustrated in simplified form in Figure 7-25. The four power transistors operate in pairs (Q109, Q114 and Q111, Q110) to establish current flow through the motor in a positive or negative direction. Motor current always flows through the sense resistor R148 in the same direction.

Figure 7-26 illustrates current flow for a forward command from the processor board. The CMFWD signal is through the driver circuits turning on Q114. Q114 remains on as long as the processor is commanding forward motion. CMFWD prevents Q110, Q111 from conducting (Figure 7-25). The operation of the carriage motor circuit can be analyzed using the conduction paths illustrated in Figure 7-26 for forward motion. Conduction in transistor Q109 is controlled by three signals: CMFWD, SCON−, and I_{LOW}.

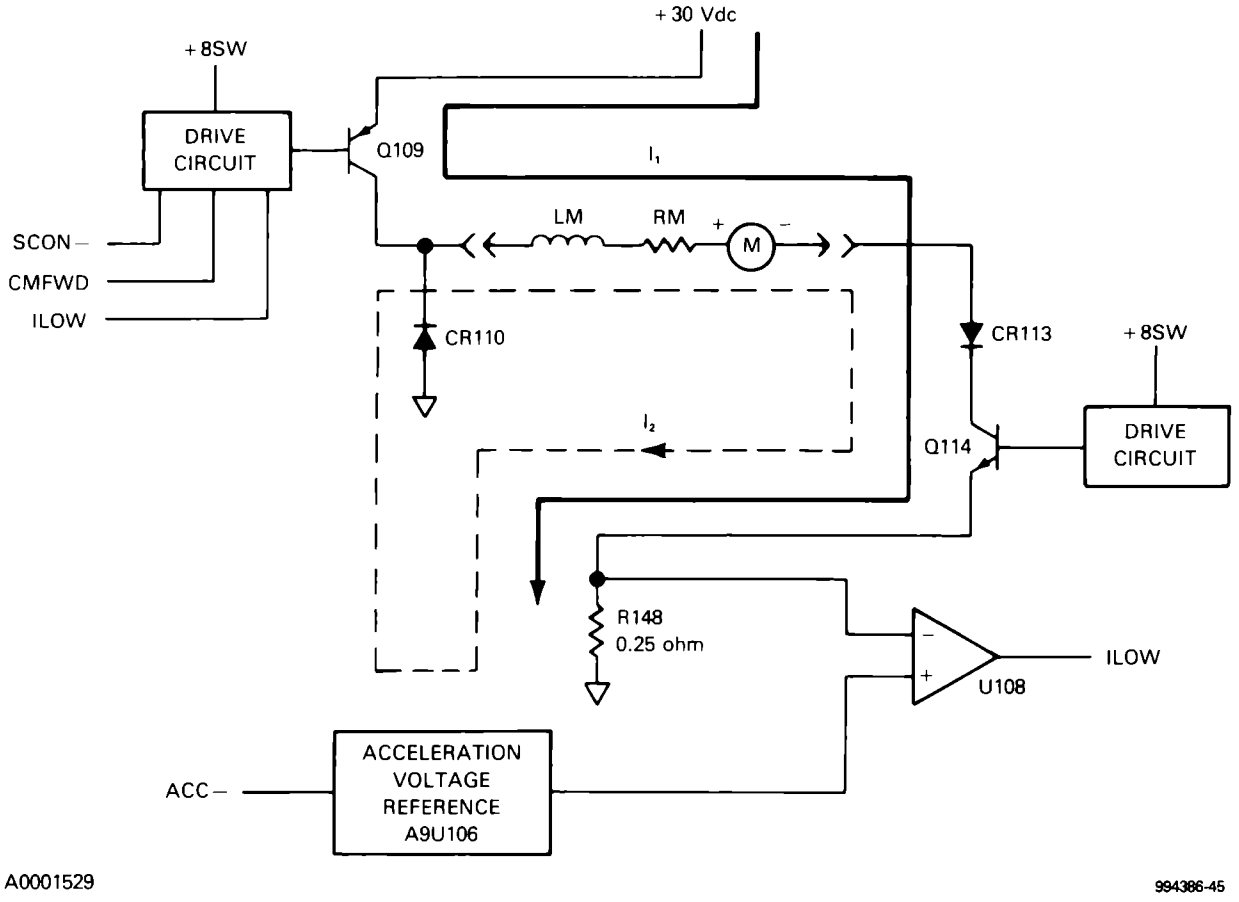


Figure 7-26. Printhead Carriage Driver Circuit Forward Command

CMFWD and SCON— are generated by the processor board and are assumed to be true for this part of the circuit analysis.

I_{LOW} is a logic level signal generated on the driver board by comparator U108, which compares a voltage drop across R148 to one of two dc reference voltages. The voltage drop across R148 is proportional to the motor current. The dc reference voltage is selected by an FET switch (A9U106) when the ACC command is sent by the processor board. The output of comparator U108 is at a logic one level if the voltage drop across R148 is less than the selected dc reference voltage. Thus, I_{LOW} is high when the motor current is below the reference selected, or low when the motor current is greater than the reference.

Assuming the processor has selected forward motion by setting CMFWD and SCON— true, I_{LOW} determines if Q109 is conducting. When Q109 is turned on, current I_1 (Figure 7-26) exponentially increases towards a target value set by the unregulated supply voltage, the back electromagnetic field generated by the motor, and the circuit resistance. The time constant of this exponential rise is set by the motor inductance and the circuit resistance. Figure 7-27 illustrates a typical motor current waveform from turn-on through the first few regulating cycles.

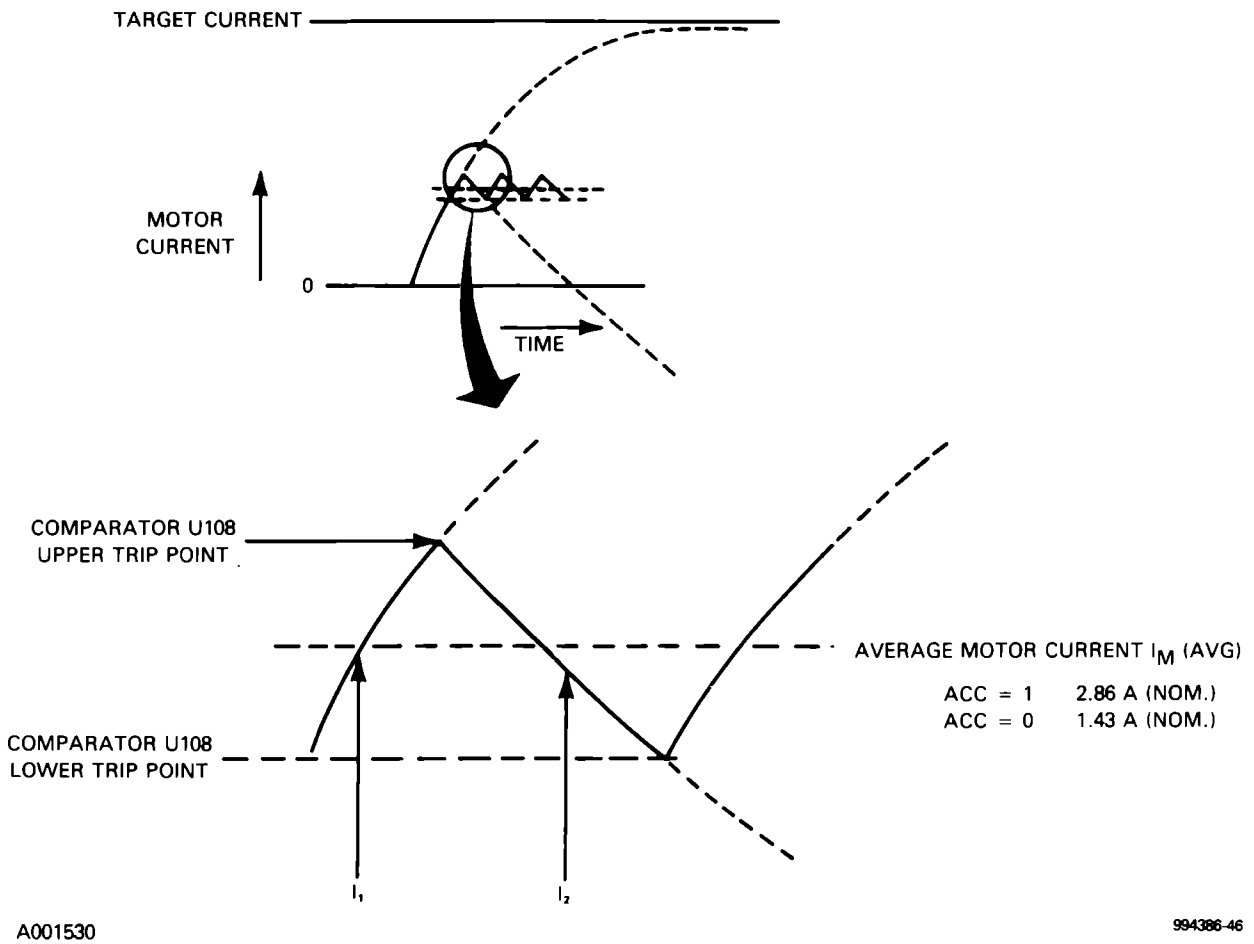


Figure 7-27. Printhead Carriage Motor Current Waveforms

When the motor current reaches the comparator upper trip point, I_{LOW} goes low, turning Q109 off. The current path shown as I_1, therefore, is interrupted. Motor current cannot change instantaneously, however, due to the motor inductance. The collapsing magnetic field in the motor tries to maintain the motor current. Figure 7-26 illustrates this current path (I_2).

Figure 7-27 illustrates the exponential decay of motor current I_2. The motor inductance and circuit resistance determine the time constant or decay rate for the motor current.

The comparator circuit has a designed-in hysteresis which causes the lower trip point to be approximately 150 mA lower than the upper trip point. When I_2 decays to this lower trip point, I_{LOW} goes high again (Figure 7-26). This action turns Q109 on again and current is again established along current path I_1. Q109 is turned on and off at a frequency determined by the current rise (I_1) and fall times (I_2) and the amount of comparator hysteresis.

The nominal frequency is 10 kHz, although this value can vary widely with variations in motors and the +30 Vdc unregulated supply voltage. As long as SCON— and CMFWD remain true, this switching action continues and produces a constant average current in the motor windings. This average motor current is between the upper and lower comparator trip points as shown in Figure 7-27. Average motor current is also determined by the dc reference voltage applied to the comparator positive input terminal. When ACC— is true, the average motor current is 2.86A (nominal). When ACC— is false, the average motor current is 1.43A (nominal).

Bidirectional printhead drive capability is achieved by reversing the current flow in the motor. The processor changes the circuit configuration by changing CMFWD form true to false (Figure 7-25). In the reverse direction, Q109 and Q114 are turned off and Q111 and Q110 are turned on. Regulation in the reverse direction is similar to the forward current cycle except that the current flows through Q110, Q111, CR109, R148, and CR112.

The Logic Driver diagram (drawing number 994527 in Section 10) is a detailed schematic of the carriage motor power circuits. The basic circuit components are Q109 through Q114, CR110, CR112, and U108. Transistors Q107, Q108, and logic gates U107A and U105A form the drive circuit and logic functions for Q109. Transistors Q112, Q113, and logic gates U105B and U107B form the drive circuit and logic functions for Q111.

Q110 and Q114 are high-gain Darlington power transistors requiring minimal base current through R138 and R146, respectively. Diodes CR109 and CR113 prevent inverted mode operation of Q110 and Q114 during the motor current decay phase (I_2, Figure 7-27).

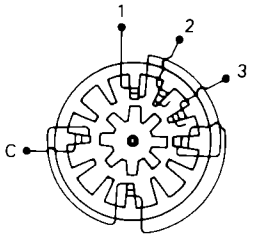
CR107 is a 1-percent, 5.1V zener reference diode which sets the 2.86A current level for high acceleration. This same 5.1V reference source is divided down by R131 and R133 to set the 1.43A reference for U108. U106 is a quad FET switch which selects the required reference. The reference voltage set by CR107 is also used by the paper feed motor drive circuit.

U108 is an inverting comparator with the hysteresis level set by R154. Resistor R155 and CR114 bias the output stage of U108 to 0.6V below ground. This provides additional noise margins when coupling to TTL circuits grounded on the Motherboard.

The +8 SW supply voltage controls the base drive to Q110 and Q114 directly and to Q109 and Q111 indirectly. Thus, the +8 SW supply forms a positive motor drive inhibit function independent of logic supplies, which prevents application of power to the carriage motor during power-up sequences or marginal power conditions since the +8 SW is only turned on when power-good is true. (See paragraph 7.3.4.7 for a power-good circuit description.)

7.3.3.3 Paper Feed Motor Drive Circuits. Commands from the microprocessor enable the stepper motor driver circuits which provide current for the three-phase variable reluctance (VR) stepper motor. Logic signals from the microprocessor control the sequence, direction, and magnitude of current through each of the windings to start, brake, or reverse paper motion (forms). Paper direction is controlled by pulsing the motor's A, B, and C windings in the proper order (A, B, C; A, B, C...etc. for forward; or C, B, A; C, B, A...etc. for reverse).

The VR stator consists of various wire-wound poles (Figure 7-28). The rotor consists of a cylindrical, toothed member. The number of teeth determines the step angle required (15° for the 810). When current flows through the motor windings, torque is developed to rotate the rotor to the position of minimum path reluctance.



A0001531 15° VR Stepper (3-phase), complete winding shown for one phase only. 994386-47

Figure 7-28. Variable Reluctance, Paper Feed Stepper Motor

This position is statically stable, i.e., external torque is required to move the rotor from its present position. This position is not an "absolute" position since there are many stable positions of the motor.

When a different set of windings is energized, the minimum reluctance occurs at a different set of poles and rotor teeth, moving the rotor to a new position.

This action produces rotational speed and torque coupled to the paper drive tractors through a 7.5-to-1 gear set. When the phase rotation sequence stops, the rotor position becomes fixed. The rotor *detent torque* is due to the holding current which locks the tractors and paper into position for printing.

When the energizing sequence is stopped, the rotor continues to move because of motor and load inertias. The motor overshoots until sufficient reverse torque is developed to pull the rotor back to the detent position. Special timing is used in the stepper motor drive sequence to minimize overshoot.

Figure 7-29 illustrates the major component parts of the switching regulator drive current for all three phases. These motor drive circuits form a switching mode and constant current regulator which operates from the unregulated +30 Vdc

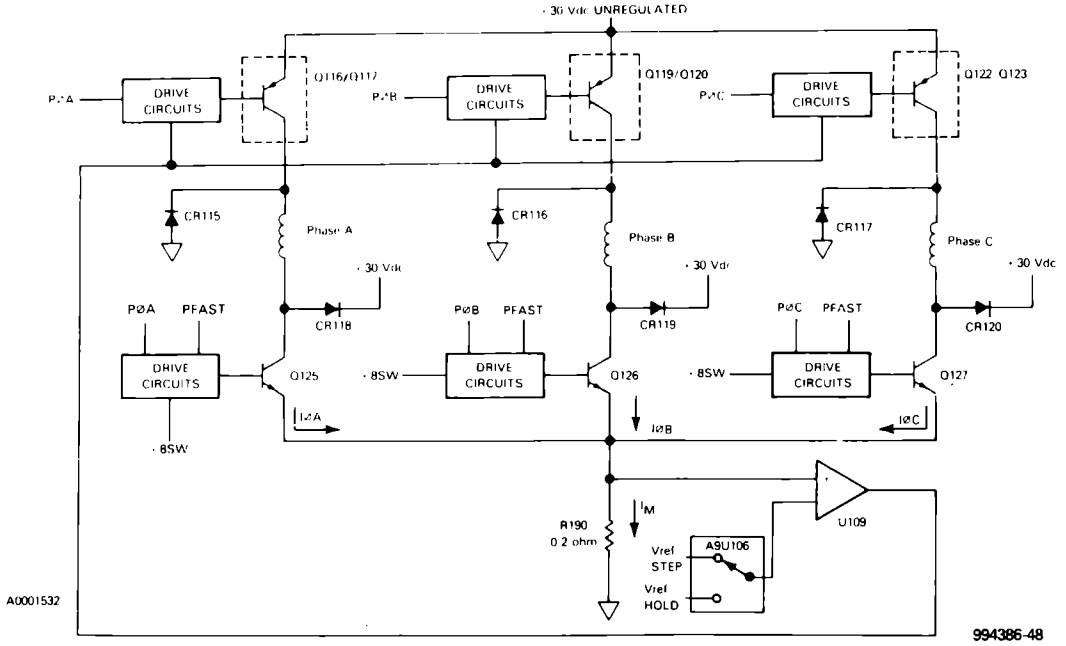


Figure 7-29. Stepper Motor Drive Circuit, Simplified Diagram

bus. The switching action (which regulates the current in a selected phase) can be analyzed using the simplified single phase schematic illustrated in Figure 7-30.

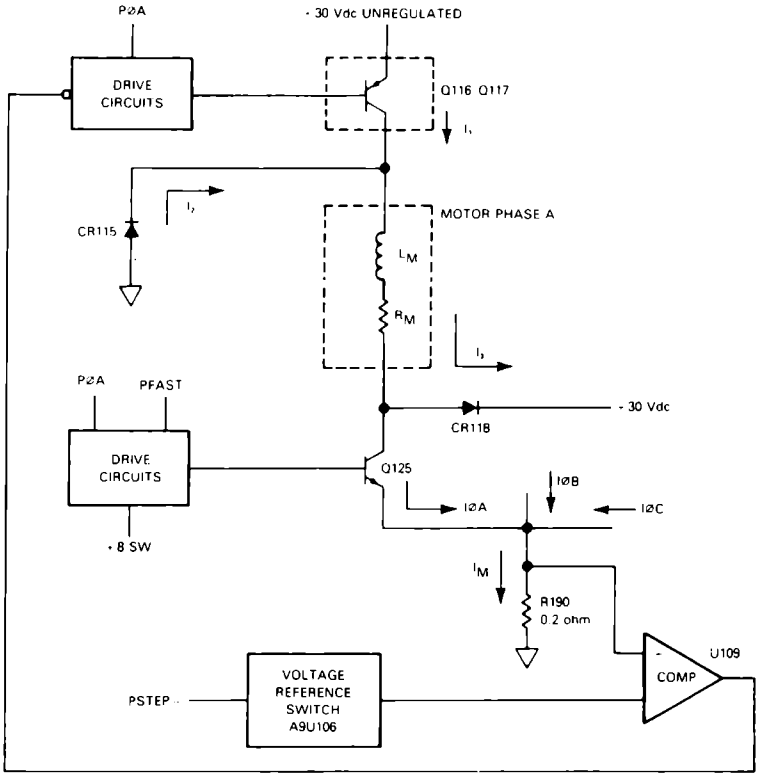


Figure 7-30. Stepper Motor Drive Circuit, Phase A 994386-49

The PNP transistor labeled Q116/Q117 is a quasi-PNP circuit formed from an NPN output stage and a PNP driver. Q116/Q117 is turned on by a combination of signal PØA from the processor board and the output of comparator U109.

The power circuits are controlled by the processor board through the following logic signals:

PØA—
PØB—
PØC— An active low on one of these signal lines determines which of the three phases will be energized. One phase is energized at all times (the signals are exclusive).

PSTEP— An active low on this line sets the motor phase current to 3.0A nominal. A high level sets the current to 1.0A.

PFAST— An active low on this line changes the time constant of the current decay circuits from slow to fast.

1. Hold mode operation. The hold mode energizes phase A (PØA) of the stepper motor with a low-level signal. Phase A is selected when the printer is switched on; other phases may be selected by pressing the form align switch on the control panel. One ampere of constant current is used to provide a detent or holding torque.

In this mode, the processor board selects the mode voltage reference and applies it to the inverting terminal of U109 (Figure 7-30). The comparator U109 output is at a logic low for motor current (I_M) which is less than the reference current.

The PFAST— command from the processor board changes the time constant of the motor current decay circuit. In the regulating mode, this command is false. Starting with zero motor current and PØA true, transistor switches Q116/Q117 and Q125 are turned on. Motor current I_1 starts to rise at a rate set by the supply voltage and the circuit time constant

determined by the motor inductance and resistance. At this instant, I_1, IØA, and I_M (Figure 7-30) represent the motor phase current.

The motor current continues to increase towards a target value set by the supply voltage and circuit resistance. Figure 7-31

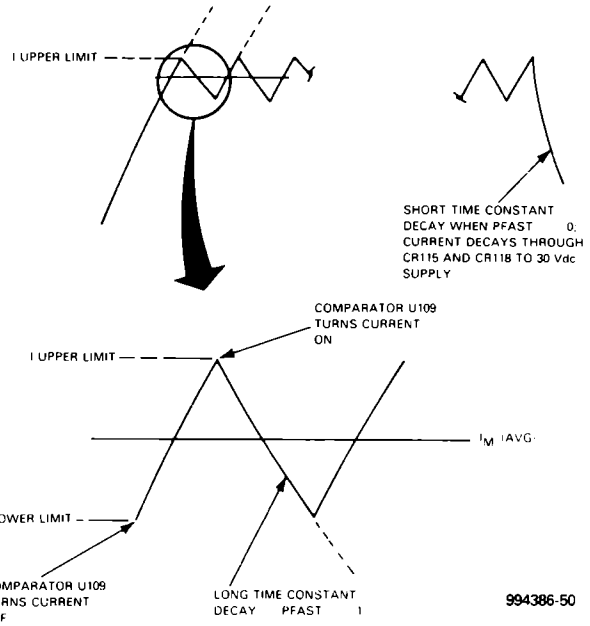


Figure 7-31. Stepper Motor Circuit Waveforms

illustrates the switching waveforms. When the current reaches the upper comparator limit, the voltage drop across R190 equals the hold current reference voltage and comparator U109 switches to a high state. This, in turn, switches off transistor Q116/Q117.

Since the motor is inductive, motor current cannot change instantly (Figure 7-30). The path for the decay current is through Q125 (IØA), R190 (I_M), and CR115 (I_2). The time constant for this decay path is determined by the motor and circuit resistances, and is relatively long. The current continues to decay until the lower current limit is reached. The lower limit is set by the hold current reference voltage and the comparator U109 hysteresis. At the lower limit, Q116/Q117 are again turned on and the switching cycle is repeated. The holding current is the average of the switched current waveform.

2. Stepping Mode Operation. The regulation action of the stepper motor driver circuit is similar to the analysis present for the hold current mode. There are, however, exceptions.

Magnitude: The average current level is maintained at a 3.0A (nominal) level by the PSTEP— command.

End-of-step time delay: When switching current from one phase to another during the stepping mode, a decrease in the time constant is required for the current decay in the phase being turned off. This is accomplished by turning off Q125 with the PFAST— signal from the processor. The decay current then follows through diode CR118 and CR115 as shown by I_3 and I_2 in Figure 7-30. The energy stored in the magnetic field of the motor windings is returned to the +30 volt supply, and the current decays rapidly as illustrated in Figure 7-31.

3. Motor Braking Mode. Referring again to Figure 7-30, note that the three phase currents IØA, IØB, and IØC are summed to form the total motor current I_M. Therefore, when viewed as a complete driver circuit, the total regulated current is 3A in the stepping mode. This summing effect is important during the overlap time between the decay current in the preceding phase and the buildup of current in the phase being turned on.

   Figure 7-32 illustrates the current distribution in the stepper motor when making a transition to the last or detent phase. Normal stepping time, or the time each phase is energized in the stepping mode, is 2 msec. At the end of each step the time constant is changed to fast (PFAST− = 0), which causes a rapid decay of phase current. At t_{12} (Figure 7-32) the normal sequence is changed to leave the decay time constant in the slow mode (PFAST− = 1). The phase signals are advanced as in a normal step. The slowly decaying current (Note 1, Figure 7-32) retards the normally fast current buildup of the next phase (Note 2, Figure 7-32). This is necessary since the sum of the phase currents must be equal to the programmed motor current.

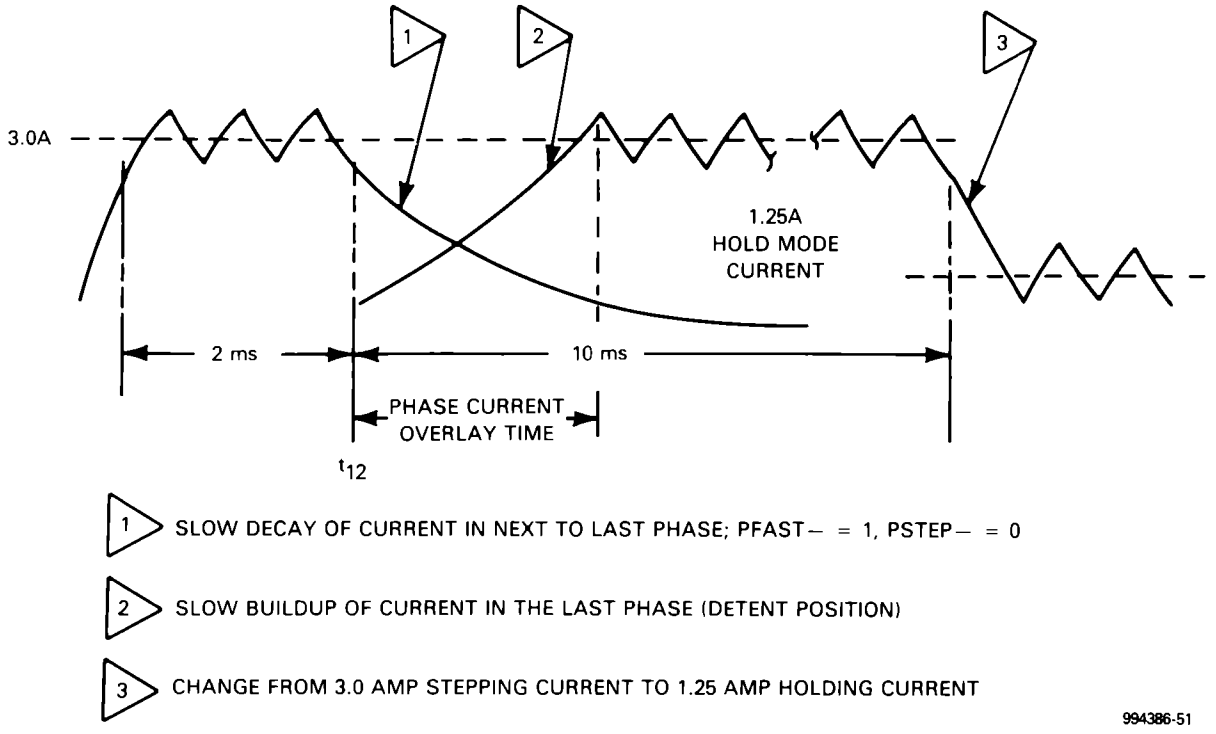


Figure 7-32. Paper Feed Stepper Motor Currents

The mechanical position of the rotor at time t_{12} is leading the energized winding. The slow decay of current, therefore, becomes a retarding force. In addition, slow buildup of current in the detent windings provides only a relatively weak accelerating force on the rotor. The net effect is to slow the rotor just before detenting to the final position. This action minimizes the overshoot of the rotor and brings the paper advance mechanism to a smooth stop.

4. Line Feed Cycle. Figure 7-33 illustrates the current waveforms in the phase A, B, and C windings of the motor for a complete 12-step line feed. The diagram assumes the motor is in the hold mode with phase C energized at the start of the sequence.

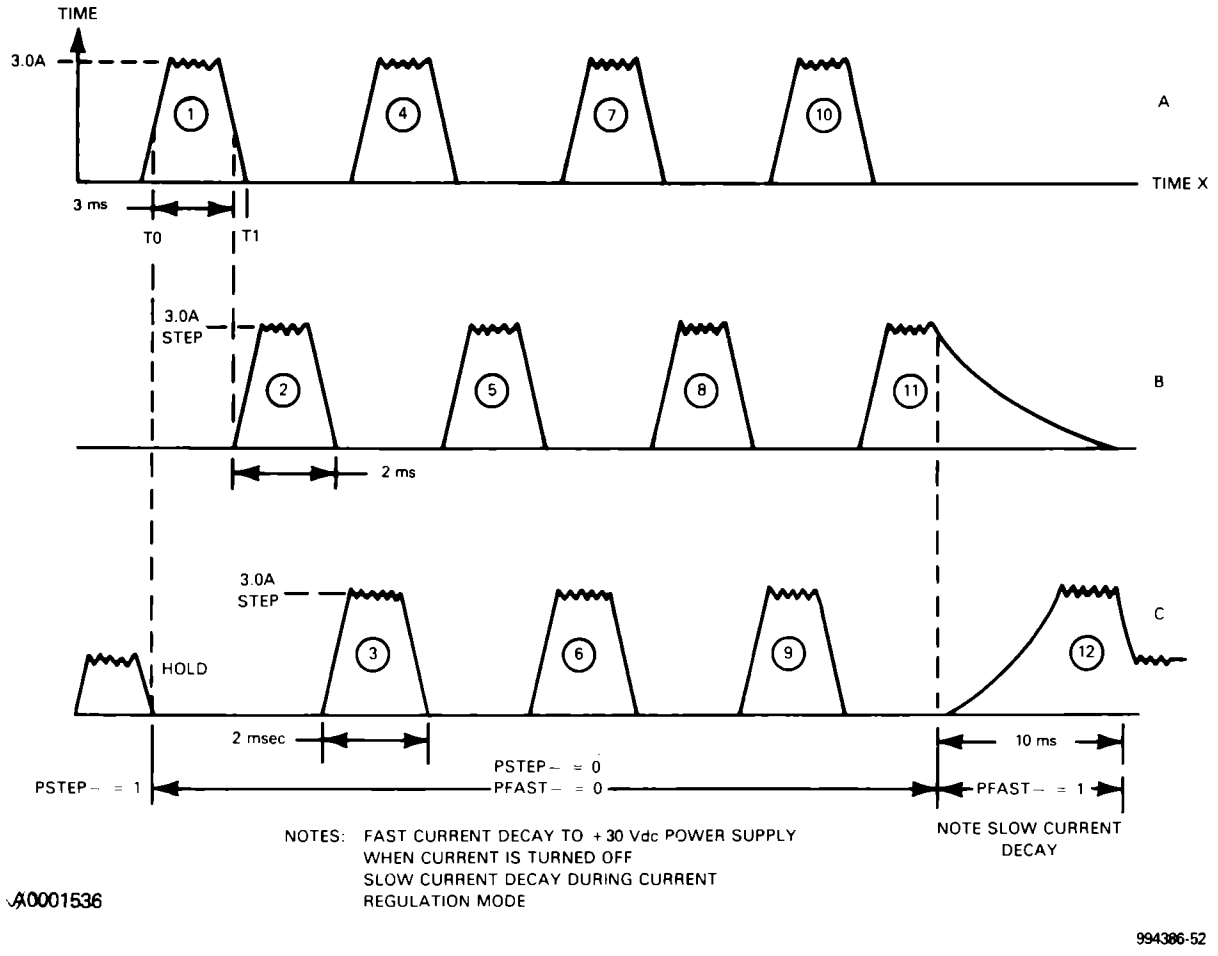


Figure 7-33. Stepper Motor Line Feed Cycle

7.3.4 Power Supply

The power supply, TI Part No. 994534, consists of the ac power module and the power supply board (which plugs into the Motherboard). The power supply provides the necessary voltage and current requirements for all printer operations. It also generates power-good and reset signals for initializing the microprocessor system when power is turned on. Figure 7-34 provides a detailed block diagram of the power supply. (The sheet numbers listed on Figure 7-34 refer to sheets of Schematic 994533 located in Section 7. A different power supply, TI Part No. 994392, appears in some units and is covered in Appendix K.)

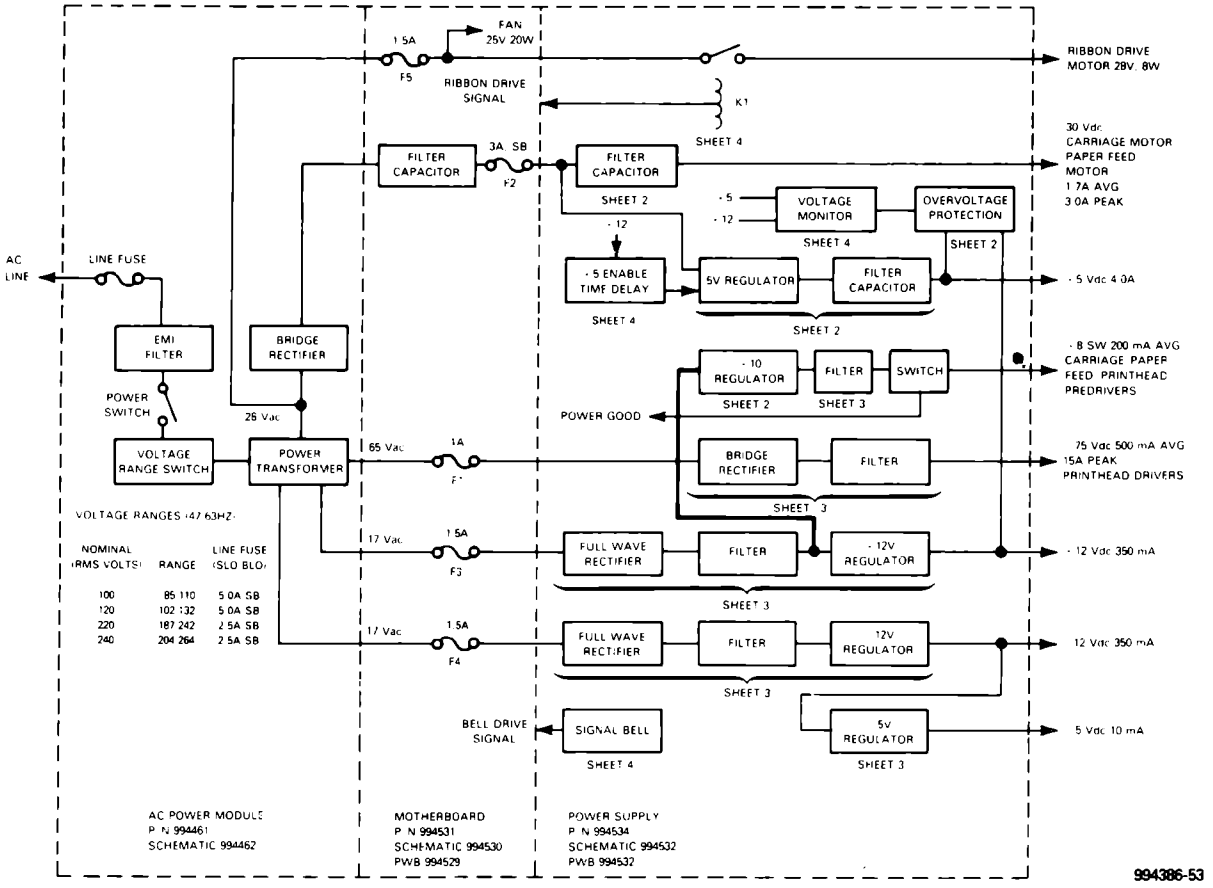


Figure 7-34. Power Supply Functional Block Diagram

7.3.4.1 AC Power Module. As shown in Figure 7-34, the ac power module (TI Part No. 994461) consists of an EMI filter, an on/off switch, line fuse, power transformer, a bridge rectifier, and a power input selection mechanism which allows selection of four primary line voltages: 100, 120, 220, or 240 Vac. The power supply module produces 75 Vac, 40 Vac (center-tapped to produce two 20-Vac lines), 30 Vdc unfiltered, and 28 Vac to operate the inked ribbon drive and the cooling fan.

Line voltage selection (described in Section 2,) is accomplished by changing the orientation of a small printed circuit board at the rear of the printer which rearranges the power transformer primary taps. The primary taps arrangements are illustrated in Figure 7-35. Refer to diagram number 994462 in Section 7 for a detailed schematic.

The EMI filter prevents printer switching regulator noise from being conducted into the ac power line. The ac line (primary side of the power transformer) is fused with either a 2.5A or 5.0A fuse depending upon line voltage selection. A 5.0A fuse is required for 100 or 120 Vac selection (Figure 7-34), and a 2.5A fuse is required for 220 or 240 Vac selection. The secondary side of the power transformer is fused with five fuses located on the Motherboard. Refer to diagram 994533, sheet 1, in Section 7 for its location.

7.3.4.2 +30 Vdc Supply. The +30 Vdc supply consists of a transformer, bridge rectifier, and filter capacitor configuration as illustrated in Figure 7-36.

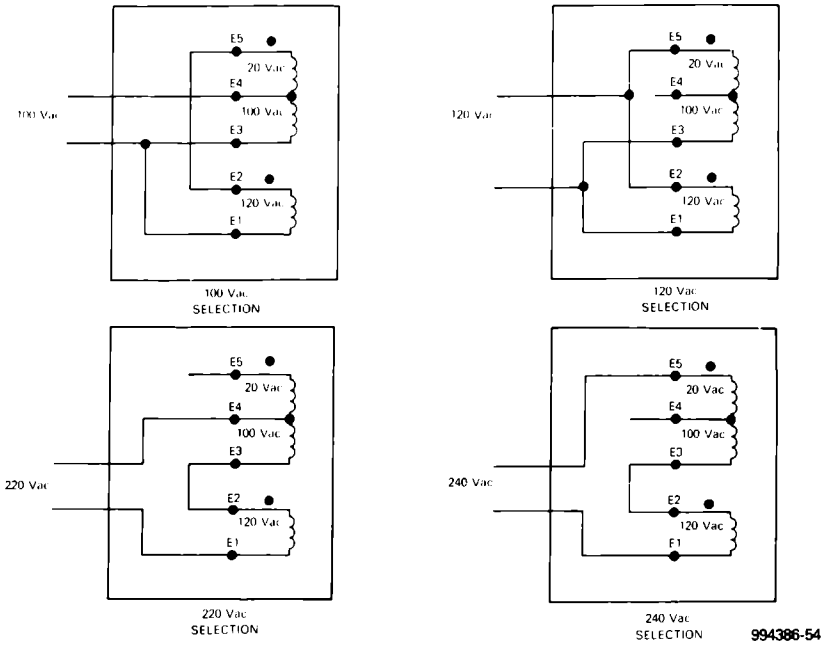


Figure 7-35. Power Transformer Primary Tap Arrangements

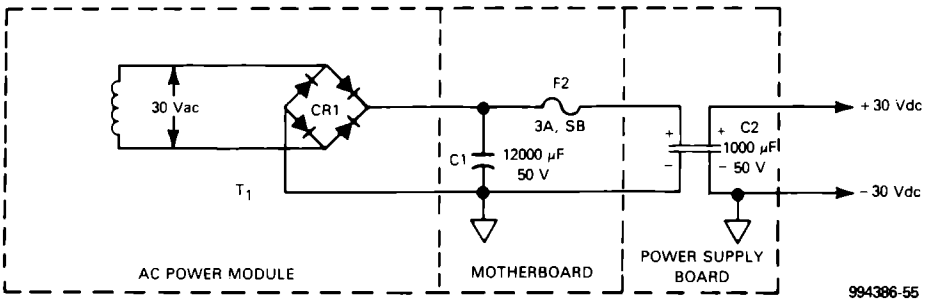


Figure 7-36. 30 Vdc Supply

The transformer and bridge rectifier are contained in the ac module. Filter capacitor C1 is located on the Motherboard and filter capacitor C2 is located on the power supply board. C1 is a low frequency electrolytic capacitor which filters the raw dc voltage from the ac module. C2 is a high frequency electrolytic capacitor used to decouple the high frequency load imposed by the numerous switching regulators in the printer.

The +30 V line supplies power for the carriage motor, paper feed motor, and +5 Vdc regulator (Figure 7-34).

7.3.4.3 +5 Vdc Regulator. The +5 Vdc regulator, located on the power supply board (Figure 7-34), furnishes power for all processor, driver board, and option board circuits. The +5 V regulator can be defined as a constant voltage switching regulator. The basic configuration of the circuit is illustrated in Figure 7-37a. The +30 Vdc supply provides input power for the +5 Vdc regulator.

The +5 Vdc regulator output is maintained at +5 ±0.10 Vdc with a load current from 0.5 to 4.0A. The output is regulated by the power switch Q4 duty cycle and the control circuitry (which monitors the ac and dc voltage cross R10 and the 5 Vdc output voltage). L1, C7, C8, and C9 are the energy storage elements of the regulator. CR4 serves as a commutating diode during the off time of Q4. The enable circuit provides a means of enabling or disabling the entire regulator, i.e., when +5 ENA is high, the regulator is turned on.

Refer to drawing number 994533, sheet 2, in Section 10 for diagrams pertaining to the following discussion of the +5 Vdc regulator operation.

Assembly number 0994534, revision V and later, have a 5.6 V zener clamp on the +5 Vdc line, as shown in Figure 7-37b. Fuse F1 will blow if the +5 Vdc load exceeds 5 A, or if +5 Vdc exceeds 5.6 V.

Transistors Q3 and Q4 form a power switch which is turned on or off by the circuit which controls transistor Q2. Q2 acts as a voltage isolating element to prevent the +30 Vdc on the base of Q3 from increasing the driving point (pin 2 of AR1) more than 0.6 V above the AR1 supply voltage

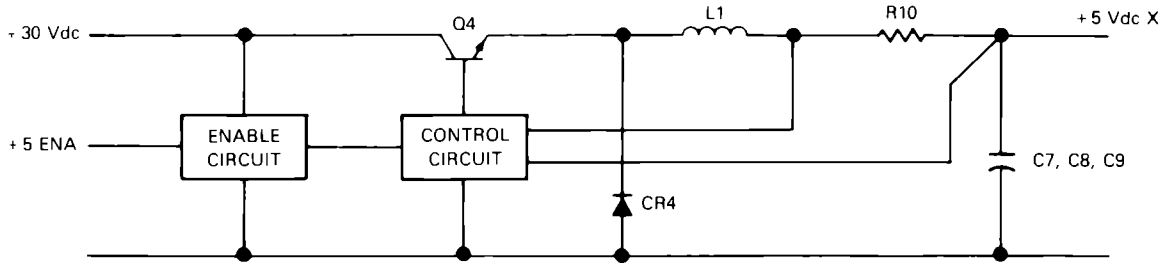


Figure 7-37a. 5 Vdc Regulator

994386-56

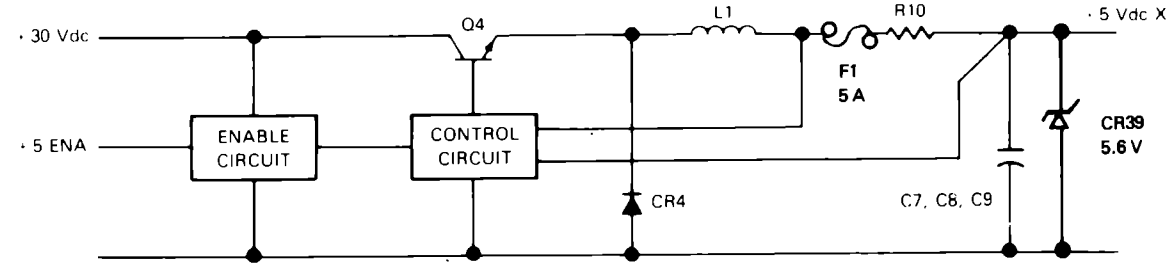


Figure 7-37b. 5 Vdc Regulator

994386-57

(derived from CR39). Transistor Q1 enables the 24 mA constant current source which supplies current to CR39 to AR1. A voltage proportional to the ripple current in R10 is fed back to AR1 through C4 and C6. This voltage defines the filter capacitor ripple current and, thereby, the ripple voltage at the output. The voltage at pin 2 of R13 is compared to an internal reference in AR1 to produce the desired output. Adjustment of R13 will vary the output dc level from 4.2 Vdc to 5.5 Vdc. If the regulator output is overloaded Q6 senses an overvoltage across R10 and increases the off time of Q4 to current limit the regulator at 5 amps. This lowers the frequency of operation from 25 kHz to 8 kHz and produces an audible indication that the regulator is overloaded or shorted.

7.3.4.4 +8 SW Line. Refer to Figure 7-34. The +8 SW line is required to enable the power circuitry on the driver board after the +12V and +5V regulators in the power supply exceed their respective minimum values for proper machine operation (refer to power-good/reset circuit description, paragraph 7.3.4.7). This prevents carriage and paper motion and/or printing to occur during the power-up and power-down sequence of the machine. Basic implementation of the circuit is illustrated in Figure 7-38. The +8 Vdc regulator input is derived from the 12 Vdc unregulated line. The regulated output is then communicated to the load through power switch 1 which is turned on or off by the power-good signal.

Refer to drawing number 994533, sheet 3, in Section 10 to help understand the +8 SW circuit.

Through the power switch comprised of Q8 (Darlington) and its driver transistor Q7, the +8 SW is connected to the load. Q7 is turned on when the "power-good" line goes high, providing a collector-emitter drop across Q8 which lowers the output to approximately 7.5 Vdc. CR41 and CR42 ensure that Q7 is off when "power-good" is low.

7.3.4.5 +12 Vdc and −5 Vdc Regulators. The ±12 Vdc regulators are two three-terminal regulators. The −5 Vdc output is regulated by zener diode CR16 from the −12 Vdc bus. Figure 7-39 illustrates ±12 Vdc and −5 Vdc regulator configuration. The input to the ±12 Vdc regulators is from a conventional center-tapped transformer, bridge rectifier, and capacitor configuration.

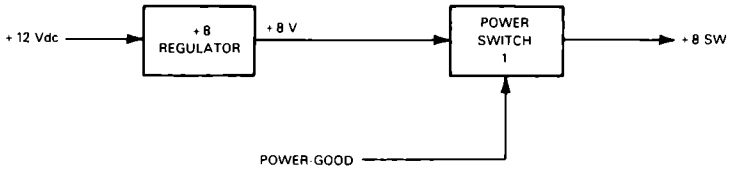


Figure 7-38. +8 SW Line

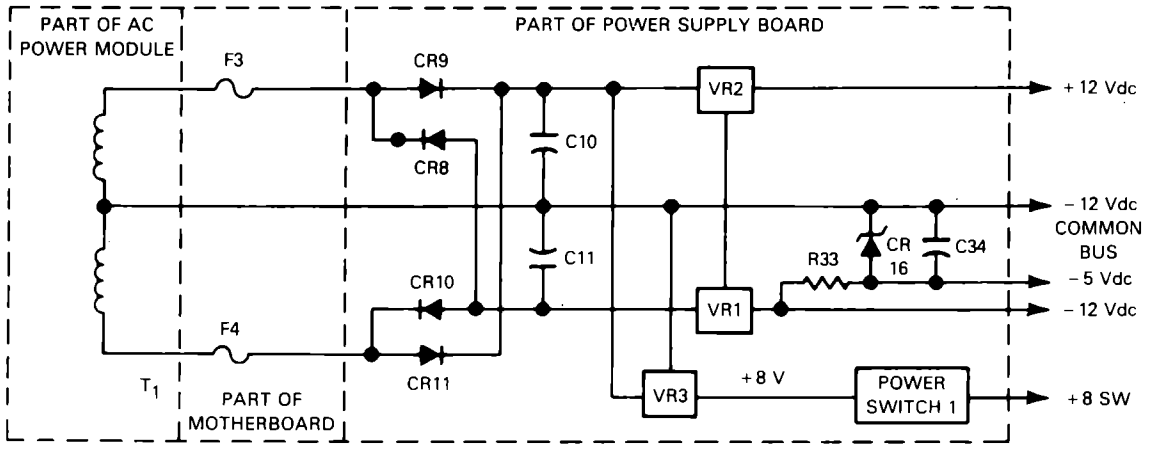


Figure 7-39. ±12 Vdc and −5 Vdc Regulators

The ± 12 Vdc output supplies the processor board and various comparators on the driver board. The −5 Vdc line is used as a substrate bias for the TMS 8080A microprocessor.

7.3.4.6 −75 Vdc Supply. The −75 Vdc source is derived from a conventional transformer, bridge rectifier, capacitor configuration as illustrated in Figure 7-40.

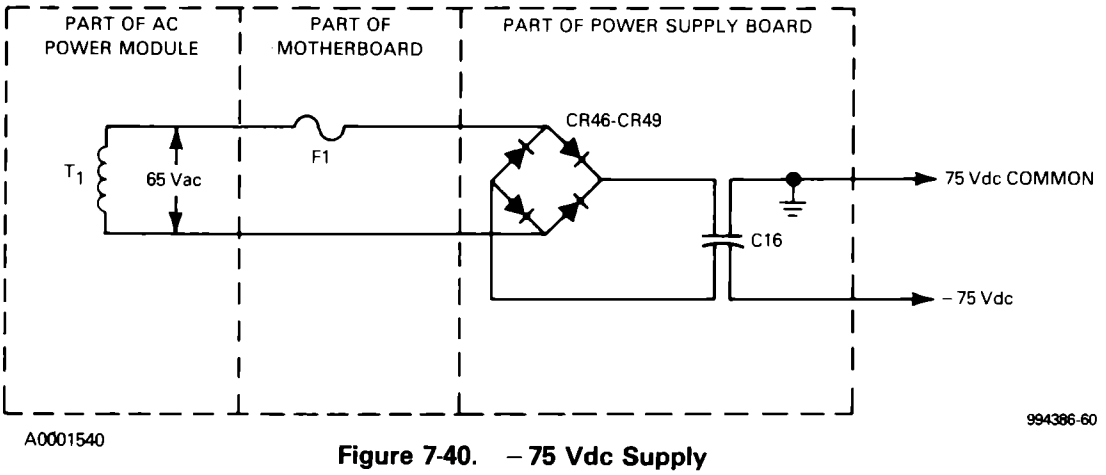


Figure 7-40. −75 Vdc Supply

The −75 Vdc supply is used only for supplying power to the printhead driver circuits. This high potential is necessary to produce fast rising current pulses in the printhead solenoids.

7.3.4.7 Power-Good/Reset. The purpose of the power-good/reset circuit is to provide signals to the processor board which indicate that the +5 Vdc and +12 Vdc supplies are above the minimum required levels for proper circuit operation. The power-good signal also controls the +8 SW power to the driver board. Figure 7-41 illustrates the power-good and reset signals provided during power-up and power-down. The low to high tran-

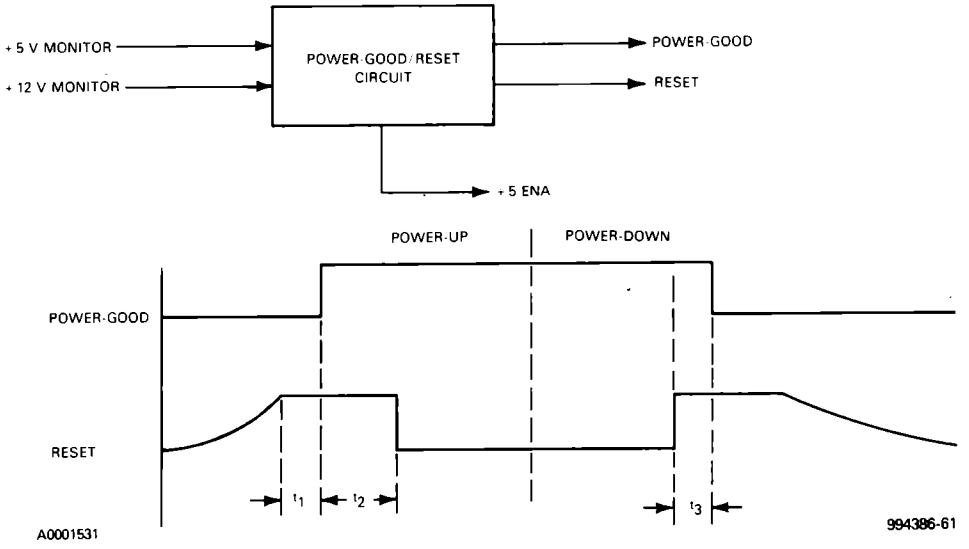


Figure 7-41. Power-Good/Reset Signal Profiles

sition of the power-good line indicates that the +5 Vdc and +12 Vdc lines exceed their respective minimum values for proper printer operation. These signals are used to reset the TMS 8080A microprocessor, as an enable for the +8 SW circuit (which remotely enables the power circuits on the driver board), and to clear the control latches on the processor board. A functional block diagram of the power-good/reset circuit is illustrated in Figure 7-42.

comparators goes low because either the +5 Vdc or the +12 Vdc line falls below its reference values, C23 discharges through R79, generating a power-down sequence. For a detailed circuit diagram of the power-good/reset circuit, refer to drawing number 994533, sheet 4, in Section 10.

The storage for the power-good/reset circuit is provided by C18. CR26 prevents C18 from being discharged by grounding the +12 Vdc monitor

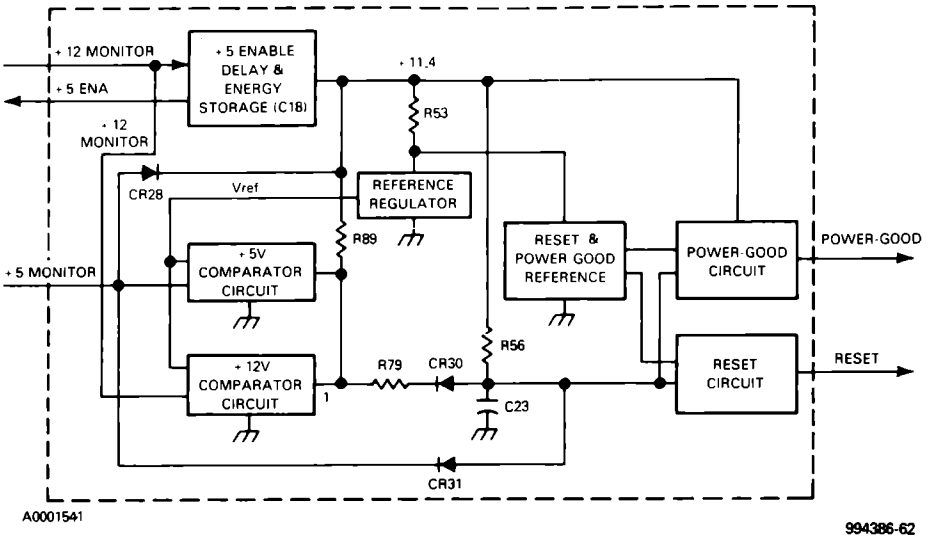


Figure 7-42. Power-Good/Reset Circuit Block Diagram

The 5 Vdc enable (ENA) provides a timed delay which allows the +12 Vdc regulator to be at least in coarse regulation before the +5 Vdc line is allowed to come up. This ensures that the power-good/reset circuit itself has adequate power for its own operation. The storage element in the block (C18) provides enough energy for this circuit to remain in operation during power-down or circuit malfunction for an orderly power-down sequence. The +5 Vdc and +12 Vdc comparator circuits compare the +12 Vdc monitor and the +5 Vdc monitor lines to a voltage generated by the reference regulator block. The outputs of these comparator circuits are wire-ANDed so that when the +5 Vdc and +12 Vdc regulators are both within limits, and both detection circuit outputs are high, C23 begins charging through R56. The voltage ramp developed across C23 is compared to a low level reference in the power-good circuit comparator and a higher level reference in the reset circuit comparator. If either of the detector line. Q14 or Q15 acts as an inverted Schmitt trigger. Q15 remains saturated during power-up while C19 is charging. This keeps the base of Q15 below the base of Q14 for approximately 200 msec, which provides enough time for the +12 Vdc regulator to come into regulation under normal conditions. If the +12 Vdc supply does not come up, the +5 ENA signal remains low, and the +5 Vdc regulator is not enabled. If the +11.4 Vdc line is grounded, C19 is discharged through CR27 and the +5 ENA line immediately goes low, disabling the +5 Vdc regulator.

CR29 and R53 provide the constant reference voltage for all the comparator circuits of the printer. The output of the power-good comparator (AR2B) is buffered by Q17 and Q18 to provide the necessary current sink capability. The output of the reset comparator goes directly to the microprocessor. CR31 provides immediate discharge of C23 in the event of a +5 Vdc short.

7.3.5 Current Loop Option Board

The current loop option board (TI Part No. 2230497-0001) enables the Model 810 printer to receive data from a teletypewriter (TTY) data source. This capability requires installation of the TTY Current Loop Interface Kit (TI Part No. 0994402) if the printer is not purchased with this option installed. The current loop option board includes a receiver circuit and a transmitter circuit. The 2230497-0001 board replaces the 0994305-0001 board.

7.3.5.1 Receiver Circuit. The current loop (TTY) receiver (refer to drawing number 2230499 in Section 10) consists of the necessary circuitry to sense current from an external source, and to convert the current levels to the appropriate EIA-level logic values required by the serial input of the processor board. The voltage drop across receiver inputs TTYRCVD and TTYRCVD/R is 3 Vdc (maximum) at 20 mA loop current into TTYRCVD. The MARK/SPACE threshold decision current is nominally 10 $\pm$6 mA. The receiver circuit utilizes an optically coupled isolator to isolate the current loop from the printer circuitry.

A current level at the receiver circuit input above the MARK/SPACE threshold will forward-bias U5 energizing the phototransistor. With the phototransistor energized, a logic ZERO is applied to Pin 5 of U3 and the RCVD output of U8 is negative (less than $-$3 volts).

With a current level at the receiver input below the MARK/SPACE threshold, the emitter and phototransistor of U5 are off and a logic ONE is applied to Pin 5 of U3. With the EIA interface disconnected, circuit BB is open and a logic ONE also appears at Pin 4 of U3, hence, circuit RCVD will be positive (greater than + 3 volts).

Circuits CDET and DSR are held positive by the action of U8.

7.3.5.2 Transmitter Circuit. The current loop (TTY) transmitter (refer to drawing number 2230499 in Section 10) consists of the circuitry necessary to switch the current in the transmit loop (supplied from an external source). The input to the transmitter is the EIA-level status signal, REVCH, from the processor board. When positive, this signal indicates that the printer is ONLINE and ready to receive data. The voltage drop across the transmitter output terminals is less than 1.5 Vdc at 20 mA loop current. The maximum spacing leakage current is 0.5 mA at 45 Vdc.

A positive voltage level (greater than + 3 volts) at Pin 10 of U9 energizes Q4 on; with Q4 on, the emitter and phototransistor of U4 are energized. With base drive supplied to Q3, the output transistor remains on, allowing current flow in the transmit loop.

A negative voltage level (less than $-$3 volts dc) at Pin 10 of U9 switches off Q4. With Q4 off, the emitter and phototransistor of U4 are off. With no base current drive, output transistor Q3 is off and the transmitter is open, i.e., no current.

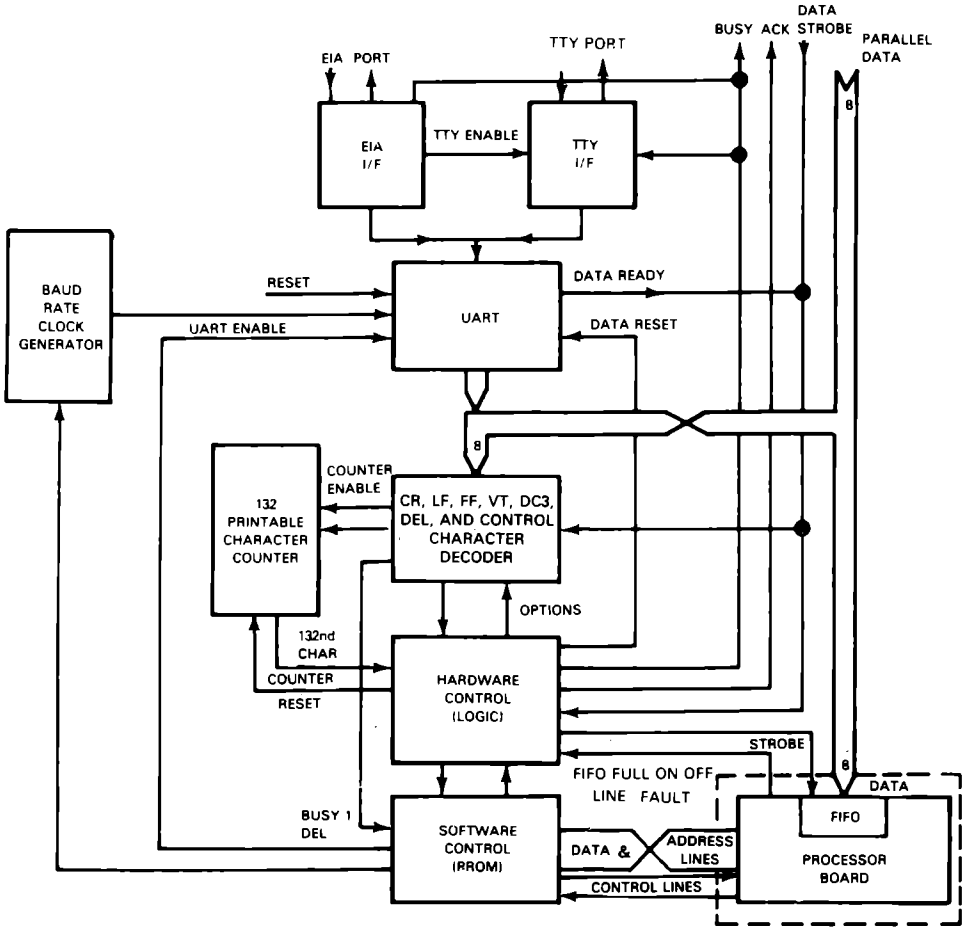
7.3.5.3 Auxiliary Parallel Interface (Obsolete). This PC board (TI Part No. 994305-0002) provides two auxiliary interface signals for the parallel interface (refer to drawing number 994303 in Section 10). The processor board 2-MHz clock signal (CLK01) is divided by U12 to produce a 125-kHz clock signal (OSCXT) at connector pin P2-66. An isolated contact closure is provided between signals LINE COUNT and LINE COUNT RET. This contact closes momentarily for each line feed.

7.3.6 Line Buffer Option Board

The optional line buffer board monitors the input data from the EIA (LBE), TTY (LBT), or PARALLEL (LBP) interface ports, and buffers one printable line of incoming data while the electronic control subsystem processes the data. The line buffer board generates BUSY and ACKNOWLEDGE signals. If a BUSY signal is caused by a received character, the BUSY signal is synchronized to occur in the middle of the last stop bit for serial data (see Figure 6-3, LBE and LBT Busy Timing) or the trailing edge of the DATA STROBE signal for parallel data (see Figure 6-4, LBP Busy Timing). Figure 7-43 is the Line Buffer Board Block Diagram.

7.3.6.1 Serial Communications Interface.

Asynchronous serial data is received by the UART (U15) from the sending device via the EIA or TTY interface ports. The serial data is received in accordance with ANSI Standard X3.16-1966 for character structure and parity sense, and ANSI Standard X3.15-1967 for bit sequence. The EIA interface converts the EIA input voltage levels to TTL output voltage levels (U10). (See drawing number 994501, sheet 3 in Section 10.) The serial data signal is gated with the DATA SET READY (DSR) and CARRIER DETECT (CDET) signals (U28). The BUSY and ONLINE signals are converted to EIA output voltage levels (U11) which are transmitted to the sending device via DATA TERMINAL READY (DTR-ONLINE) and reverse channel (BUSY) signals. The TTY interface converts the input current levels of the serial data to TTL voltage levels (U8). The BUSY signal is converted to impedance levels by the TTY transmitter circuit (U7), thus permitting a controlled current flow according to the BUSY levels.



994386-63

Figure 7-43. Line Buffer Board Block Diagram

The UART converts the serial data into parallel data which is buffered by U6 and U30 to the parallel data bus. The DATA READY (DR) signal goes to a high level when the UART receives a character. The hardware control logic generates a DTSTRB signal which is sent to the FIFO when the DR signal goes to a high level.

7.3.6.2 Baud Rate Clock Generator. The baud rate clock generator (U9, U16, U17, and U18) is controlled by the software control PROM (U21) via the address lines A, B, C, D, and E (see Table 7-4). The baud rate clock sets the baud rate for the UART receiver. The baud rate clock interval time is 1/16th the bit time of the received character.

Table 7-4. Baud Rate Selection Table

TMS 5501 (Standard)

Baud Rate	Address Lines A	B	C	D	E
9600	0	0	0	0	0
4800	0	0	1	0	0
2400	0	1	0	0	0
1200	0	1	1	0	0
300	1	0	1	0	0
150	1	1	0	0	0
110	1	1	1	1	1

TMS 5504 [Baud Rate Option (BRO)]

Baud Rate	Address Lines A	B	C	D	E
9600	0	0	0	0	0
2400	0	1	0	0	0
1200	0	1	1	0	0
600	1	0	0	0	0
300	1	0	1	0	0
200	1	1	0	1	0
110	1	1	1	1	1

7.3.6.3 Control Character Decoder. This decoder decodes the following control characters: Carriage Return (CR), Line Feed (LF), Vertical Tab (VT), Form Feed (FF), software off-line command (DC3) and Delete (DEL) from the parallel data bus, and sends a signal (U14, U22A; U23B, U32) to the hardware control logic.

7.3.6.4 132-Printable Character Counter. This counter (U41 or U42) counts the number of printable characters received for one line of data. When the 132nd printable character is counted, a carry signal (U44—see drawing number 994501, sheet 4, in Section 10) is sent to the hardware control logic. The counter is cleared by any line termination character.

7.3.6.5 Hardware Control Logic. The hardware control logic consists of a BUSY signal generator and the ACKNOWLEDGE signal timing logic. The signal that results from the control character decoder signal being ORed with the carry signal from the 132 printable character counter (U24C and U34C) sets the internal BUSY signal (BUSY 1) U41A. (See drawing number 994501, sheet 4, Section 10.)

The line buffer boards BUSY signal is the result of the BUSY1 signal ORed with the processor board's BUSY signal (U42A).

The DTSTRB signal from the parallel port, or the DR signal from the UART, sets flip-flop U36A for acknowledge request. (See drawing number 994501, sheet 3, in Section 10.) The acknowledge request signal is propagated by clocks which are synchronized with the FIFO parallel data store clock. The acknowledge timing logic generates an ACKNOWLEDGE signal (ACK) and a data ready reset (DRR) signal after the FIFO stores the parallel data.

7.3.6.6 Software Control (PROM). The line buffer interface software control resides in the programmable read only memory (PROM) U21. The address decoder (U4 and U20) (see drawing number 994501, sheet 2, in Section 10) disables the 4K ROM on the processor board (via the TEST MODE signal) and enables PROM U21 on the line buffer board whenever the 8080 processor addresses locations 38-3F HEX (refer to Figure 7-44). At location 38-3F HEX, the software in PROM U21 sets the program counter of the 8080 processor to 70XX HEX, where XX is set according to the patch code table (refer to Figure 7-45). When a program is completed, the return routine in PROM U21 returns to the original patch hook call routine in the 4K ROM software.

The software control residing in the line buffer PROM U21 complements the hardware control functions and modifies the firmware of the 810 printer. These functions are:

1. Clear the BUSY1 signal whenever the FIFO is empty.
2. Clear the print buffer and stop printing whenever the delete (DEL) character is received.
3. Set the baud rate clock generator specified by the pencil switches on the auxiliary control panel.
4. Set the line width of 132 characters.
5. Insert a CARRIAGE RETURN (CR) following the 132nd printable character.

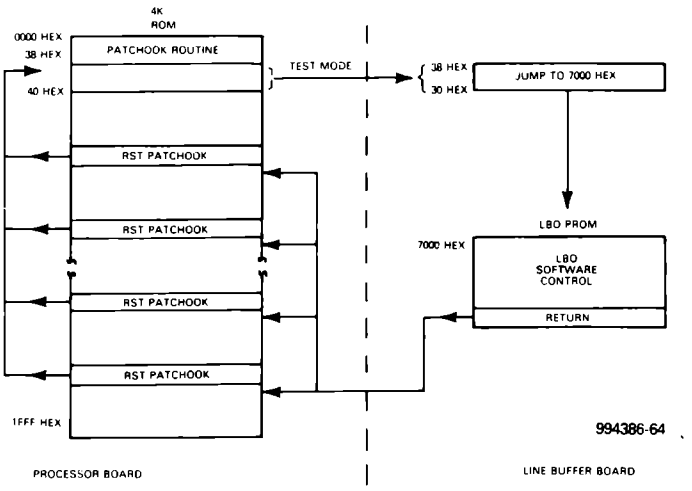


Figure 7-44. Line Buffer Option Modification of 810 Firmware

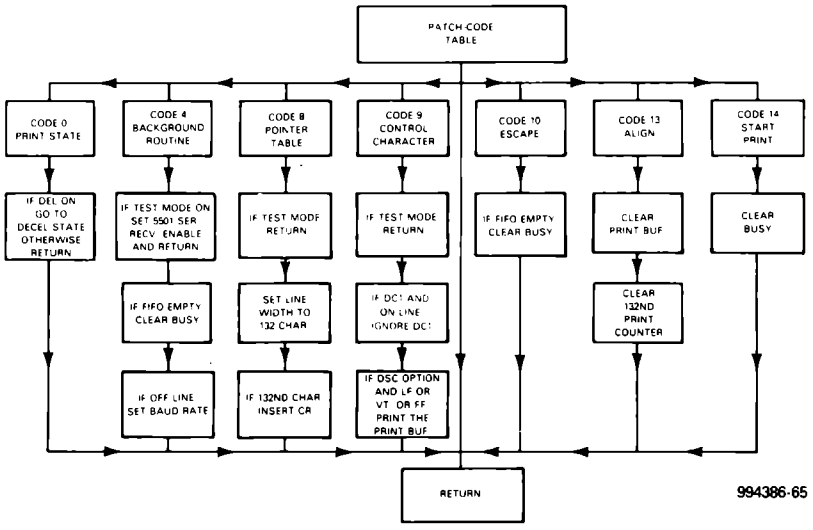


Figure 7-45. Line Buffer Option Software Block Diagram

Section 8

Maintenance

8.1 INTRODUCTION

Preventive and routine maintenance procedures may be performed by the operator. More complex maintenance or repair should be performed by qualified technicians. In addition to the information found in this section, Appendix L presents the removal procedures for older models of the carriage drive motor, the control panel assembly, and the auxiliary control panel assembly.

8.2 PREVENTIVE MAINTENANCE

To ensure satisfactory operation of the printer in normal service, the following maintenance schedule must be observed.

Procedure	Period
Vacuuming	Every month
Cleaning Ribbon Guides	Every month
Optional Battery Replacement	Every 15 months

NOTE

Failure to follow the scheduled procedures, listed under Preventive Maintenance, may void the warranty.

8.3 LUBRICATION AND CLEANING

CAUTION

Do not use chlorinated solvents such as carbon tetrachloride as a cleaning agent.

Printers with printhead carriage mechanisms manufactured earlier than Revision T require monthly lubrication. Use the Model 810 Service Kit (TI Part No. 994472) which contains an approved cleaning agent and lubricant.

IMPORTANT NOTE

Printers with printhead carriage mechanisms designated Revision T and later do not require oiling of the carriage guide rods or the paper advance gear eyelet; doing so defeats the self-lubrication properties of the bearings. These printers can be identified by an instruction label on the platen.

8.3.1 Oiling Printer Carriage Guide Rods **

Refer to Figure 8-1 for component locations.

1. Clean the printhead carriage rods (both upper and lower) with a cloth soaked in denatured alcohol.

2. Apply a few drops of lubricant* to the printhead carriage rods. Manually move the carriage back and forth to oil the printhead carriage bearings.

8.3.2 Oiling Paper Advance Gear Eyelet

Refer to Figure 8-2 for component locations.

1. Locate the paper advance bearing installation hole on the outboard side of the right sideplate (the hole is partially obscured by the paper advance motor).

2. Using a suitable applicator, apply no more than one drop of lubricant* through the hole onto the eyelet.

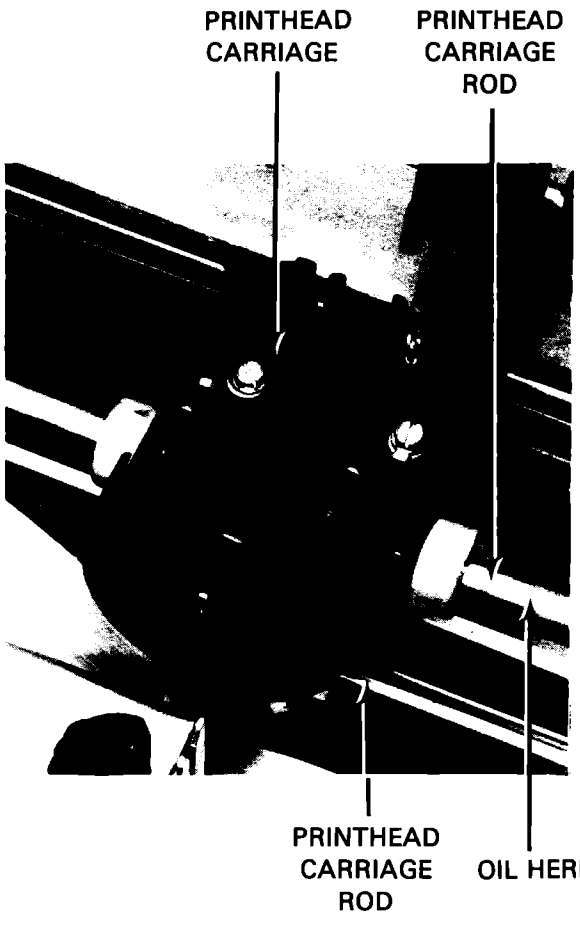


Figure 8-1. Carriage Lubrication Points

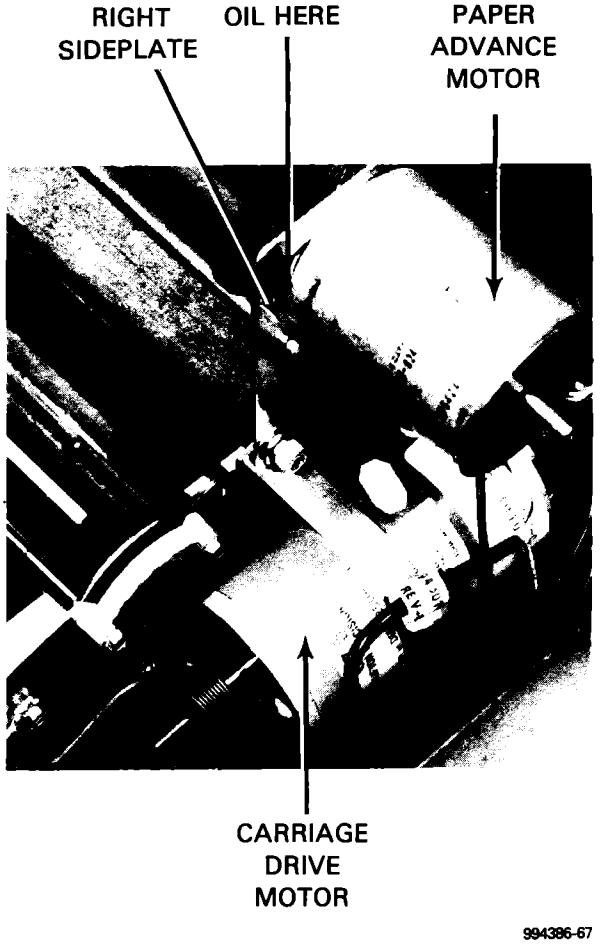


Figure 8-2. Paper Advance Lubrication Points

* Use TI Part No. 0199594-0001 or equivalent listed below:
1. Terristic 43 Oil (Exxon)
2. Regal Oil A—R & O (Texaco)

** See Important Note in Section 8.3

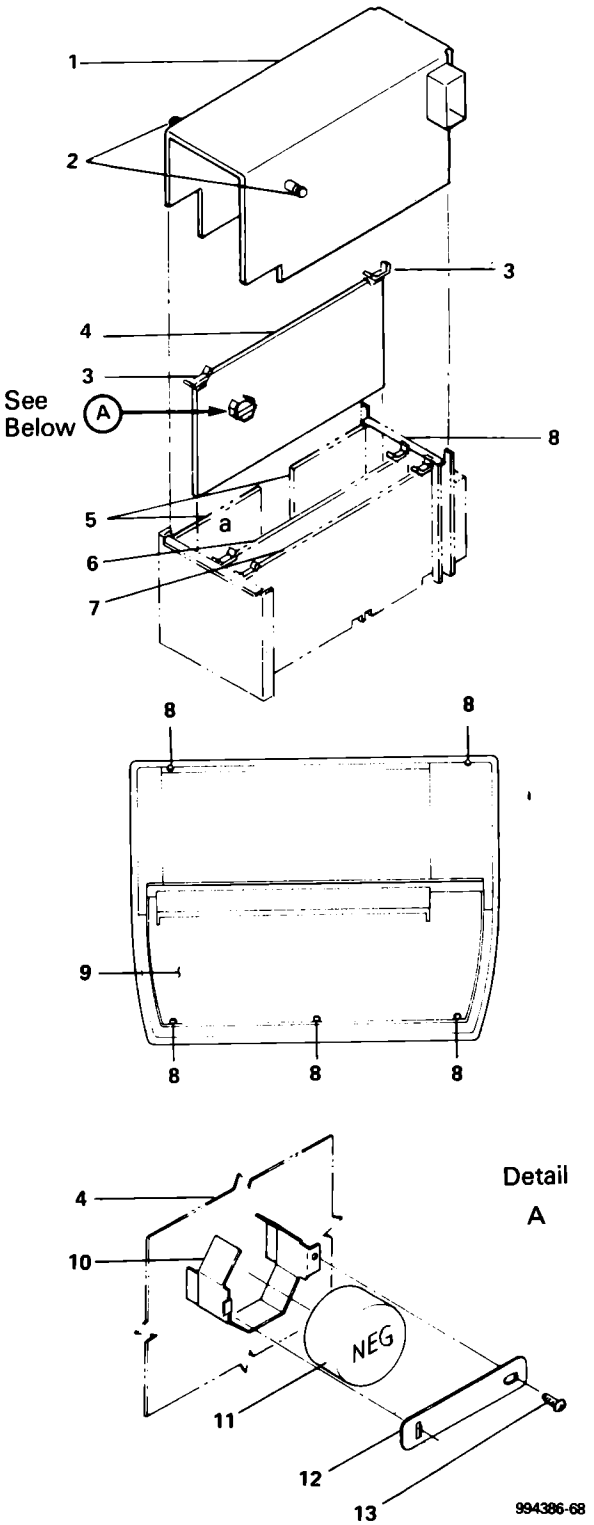
8.4 BATTERY REPLACEMENT

The VFC and VCO printers use a Mallory PX14 or equivalent battery (TI Part No. 996371-0001) which is locally available at most photographic supply stores. Qualified service personnel should refer to Figure 8-3 and proceed as follows to replace the battery.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the five screws which secure the printer cover (three screws are located under the access door; two screws are located at the left and right rear corners of the printer cover).
2. Lift off the printer cover.
3. Loosen the three screws on the electronics cover and lift the cover up and off.
4. Remove the processor PC board (the third board from the front of the printer with the green ejector).
5. On the processor PC board, remove the screw from the battery strap and remove the battery strap. Save the screw and battery strap.
6. Install a new battery with the positive (+) side down (touching the printed circuit board) in the battery retainer.
7. Replace the battery strap on the battery retainer; replace the screw in the battery strap and tighten the screw.
8. Record the date of installation.
9. Replace the processor PC board, electronics cover, and the printer cover. Tighten all cover screws.



1. Electronics Cover
2. Cover Screws
3. Ejector Tabs
4. Processor Board (Green Ejector Tabs)
5. Option Boards
   a. Interface PC Board
   b. TTY Board
6. Driver Board
7. Power Supply Board (Orange Ejector Tabs)
8. Screw
9. Access Door
10. Battery Retainer
11. Battery
12. Battery Strap
13. Retainer Screw

Figure 8-3. Battery Replacement

8.5 ROUTINE MAINTENANCE AND ADJUSTMENTS

The following maintenance and adjustment procedures may be performed by the operator.

8.5.1 Ribbon Guide Adjustment

To align the ribbon path in the center of the right ribbon shift arm, perform the following procedures.

1. Remove the printer cover as discussed previously in battery replacement.
2. Slightly loosen the screw which secures the adjustable ribbon guide to the right front of the sideplate (see Figure 2-5).
3. Adjust the ribbon guide as necessary to align the ribbon in the center of the slot in the right ribbon shift arm.
4. Tighten the ribbon guide screw.
5. Replace the printer cover.

8.5.2 Fuse Replacement

To replace the power line fuse, refer to Figure 8-4 and proceed as follows.

1. At the left rear of the printer (disconnect the power cord, if installed), slide the clear plastic cover up to gain access to the fuse compartment.
2. Remove the line fuse by pulling out and upward on the FUSE PULL lever.
3. Push the FUSE PULL lever down.
4. Select the appropriate fuse from the following table:

AC Line Voltage	Fuse Type	TI Part No.
100/120V	5.0 ampere, 250V	416434-0503
220/240V	2.5 ampere, 250V	416434-0004

5. Place the fuse in the fuse holder.
6. Slide the clear plastic cover down.
7. Check that the ON/OFF switch is in the OFF position.
8. Connect the power cord to the receptacle and to the power source.

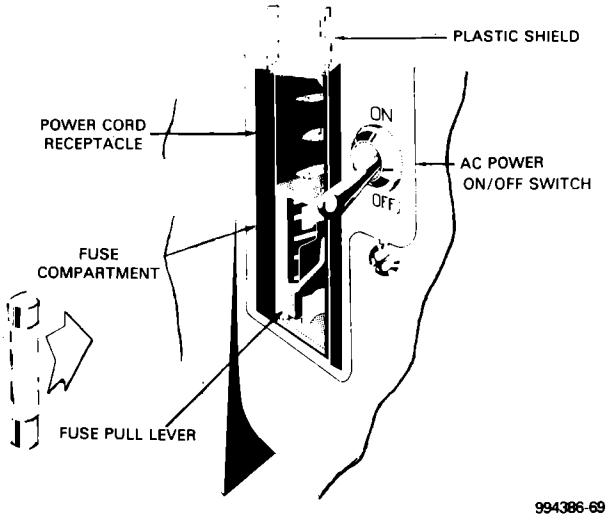


Figure 8-4. Power Fuse at Rear of Printer

8.5.3 Printhead Replacement

To remove the printhead, refer to Figure 8-5 and proceed as follows.

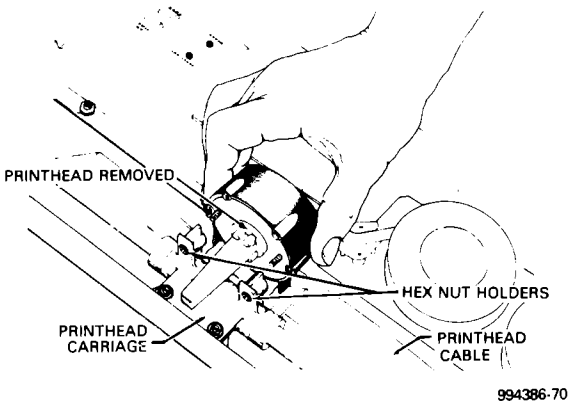


Figure 8-5. Printhead Removal

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Raise the access door.
2. Manually slide the printhead to the center of the printing area.
3. Using a 3/16-inch wrench, remove the two long hex nuts which secure the printhead to the printhead carriage.
4. Remove the printhead from the carriage by rotating the printhead back and downward out of the carriage mounting holes.
5. Remove the printhead cable from the printhead cable connector by supporting the connector with one hand while pulling the printhead up with the other hand.
6. To replace the printhead, reverse the removal steps. Tighten the two long hex nuts fingertight, then turn the wrench 25 to 90° counterclockwise.

8.6 TROUBLESHOOTING

Table 8-1 helps identify malfunctioning printer components. For aid in correcting minor operating problems, refer to Table 7-1 in the *Model 810 Printer Operating Instructions* (TI Manual No. 994353-9701). For more severe problems that may require the services of a skilled technician or TI service personnel, consult Table 8-1, Failure Analysis Chart, in this Section. To use it, select one of the 18 possible failures listed, read across to the lowest number in the chart, then upward to the area of failure. The suggestions to help correct the problems appear on the right side of the table.

Table 8-1. Failure Analysis Chart

FAILURE CATEGORY / PROBABLE AREA OF FAILURE	AC MODULE (994461)	POWER SUPPLY BOARD (994394)*	DRIVER BOARD (994322)**	PROCESSOR BOARD (994244)	MOTHERBOARD (994330)***	MOTOR ENCODER ASSY (994238)	CONTROL PANEL (994293)	AUX CONTROL PANEL (994258)	PRINTHEAD (994293)	RIBBON DRIVE ASSY (994215)	PAPER FEED MOTOR (994183)	PAPER FEED TRACTORS (994183)	FAN ASSEMBLY (996275)	AC POWER FUSES (416434)	MOTHERBOARD FUSES (416434)	PRINTHEAD TO PLATEN ADJUST MECHANICAL ASSEMBLY (994291)	CORRECTIVE ACTION
1. Failure to align carriage																	
Power on LED ON	4	3	2	1		5											Recycle power switch several times
Power on LED OFF		1															Remove all PCB's except P/S. To check for shorted +5 or +12
2. Failure to print																	
a. Self-test mode																	
(1) Carriage moves normally		4	3	5				6						2			Check −75 V fuse MB F1
(2) Carriage does not move			2	3		4								1			
b. Print quality—any mode																	
(1) Light print		3						4	2						1		Ribbon worn out
(2) Missing dots		4	3	2				5							1		
(3) Missing Characters		3	2	1													Maintains column position on printed characters. Check pencil switches.
c. Fails to print (self-test OK) or move carriage—ONLINE				1			2	3									See Section 3 of this manual. Check cables, software compatibility
3. a. Carriage drifts left or right			2	1	4	3								4			Check capstan, wire rope, carriage for damage after a slam
b. Carriage slams left or right			2	1	4	3								4			
4. Blows line fuse—MB fuses OK	1	2			3												Check for proper fuse size. Line voltage setting. Remove all cards and ac power cable from motherboard and recheck
5. Blows +30 V fuse MB F2 (3ASB)		1	2		3	4			5								Disconnect motors or PCB's and recheck test filter cap—or MB
6. Blows +28 Vac fuse MB F5 (1.5A)		3			4				2			1					Disconnect fan/ribbon drive, recheck
7. Blows 20 Vac fuse MB F3 (1.5A)		1			2												
8. Blows 20 Vac fuse MB F4 (1.5A)		1			2												
9. Blows −75 Vac fuse MB F1		2	1					3									
10. Fan stopped	3											2		1			Check for frozen fan motor
11. Ribbon drive inoperative		2		4					3					1			Processor controlled ribbon runs during printing only
12. Power will not come up (No panel indicator)	4	3					5						1	2			Recycle power several times to check for inadvertent crowbar operation. Measure +12V and +5V on P/S board; +12V will inhibit +5 supply
13. Carriage moves and stops—error light blinks		5	3	4	6	2									1		Clean and lubricate carriage rods. See subsection 8.3 of this manual. Check for obstruction to carriage movement.
14. No response to manual control panel inputs. Power indicator ON				2		1	1										Check cable connections
15. Vertical Format programs not retained on power down				1			2	2									Check battery and CMOS RAM (U25)
16. Form feeds—intermittent or random			2			1											
17. Vertical character registration out of tolerance									2	2					1		Check gearmesh; change paper drive plastic gear if worn
18. Paper feeds out of tractors											1					2	Adjust lateral tractor tension (right tractor); check paper box alignment with chute

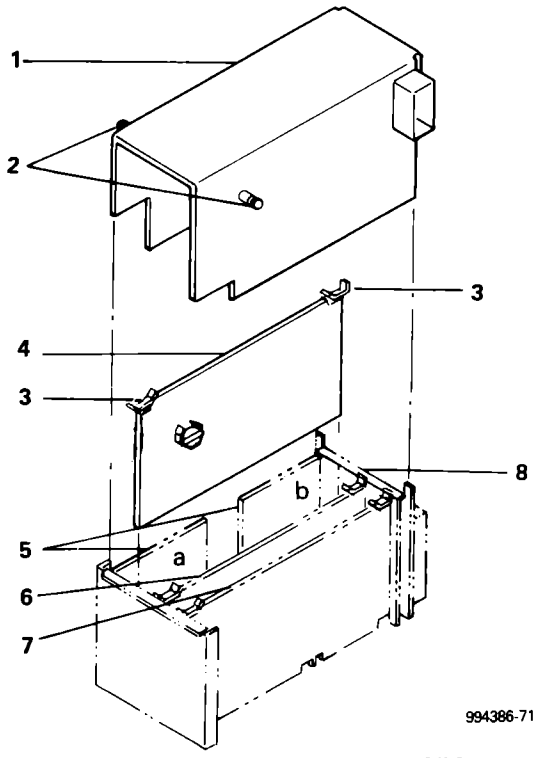
*Power Supply Board (TI Part No. 994394 or TI Part No. 994534)
**Driver Board (TI Part No. 994322 or TI Part No. 994528)
***Motherboard (TI Part No. 994330 or TI Part No. 994531)

8.7 REMOVAL AND REPLACEMENT

The following subparagraphs present removal and replacement procedures for replaceable parts. See paragraph 8.4 for the instructions on battery replacement and refer to Section 10 for identification of these parts by Texas Instruments part number. Appendix L covers the removal procedures for older models of the carriage motor, the control and indicator assembly, and the auxiliary control panel.

8.7.1 Printed Circuit Board(s)

To remove the printed circuit board(s), qualified service personnel should refer to figures 8-6 and 8-7 and proceed as follows.



LEGEND

1. Electronics Cover
2. Cover Screws
3. Ejector Tabs
4. Processor Board (Green Ejector Tabs)
5. Option Boards
   a. Interface PC Board
   b. TTY Board
6. Driver Board (Red Ejector Tabs)
7. Power Supply Board (Orange Ejector Tabs)
8. Screw

Figure 8-6. Printed Circuit Board Removal

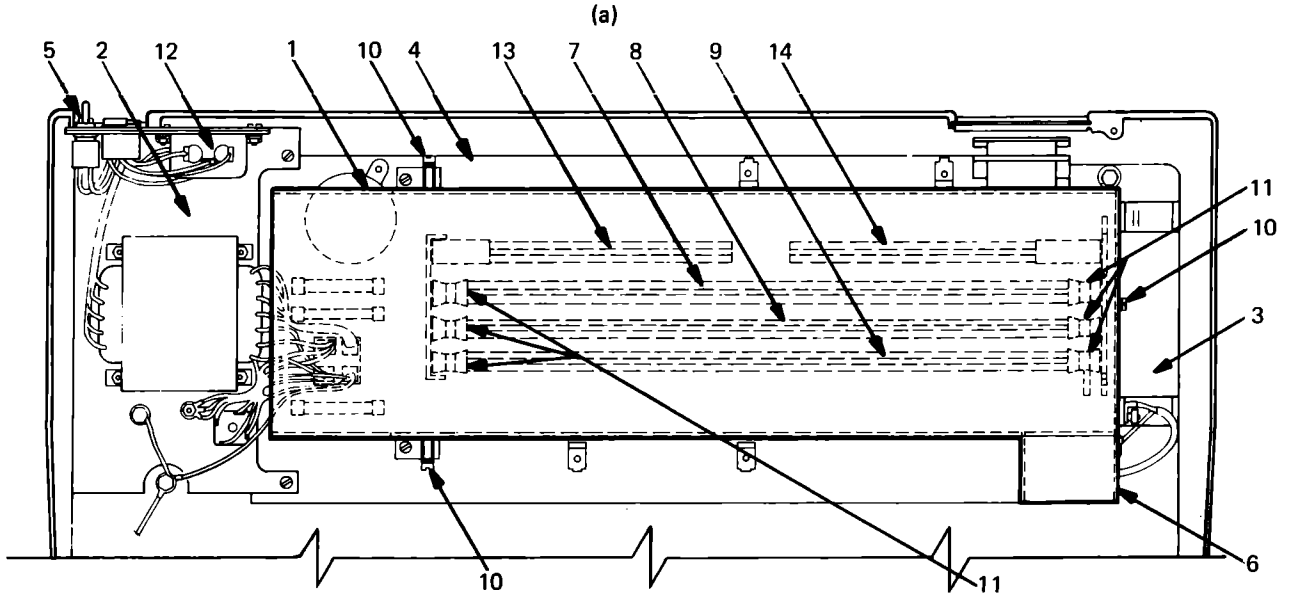
WARNING

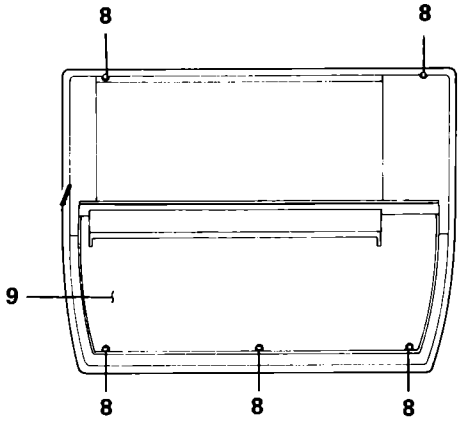
Disconnect the power cord to prevent possible electrical shock.

1. Remove the five screws securing the printer cover (three screws are located under the access door; two screws are located at the left and right rear corners of the printer cover).
2. Lift off the printer cover.
3. Loosen the three screws on the electronics cover and lift the cover up and off.
4. Remove the printed circuit board(s) by placing your thumbs underneath the innermost section of the ejector tabs and pushing on them.
5. To replace the printed circuit boards and covers, reverse the removal steps. Remember to match the ejector tab colors with the same colored dot(s) on top of the right card guide.

NOTE

When replacing the processor board, refer to Table 8-2 at the end of Section 8 for the location of the optional PROMs, etc. which must be transferred to the replacement assembly.





LEGEND

1. Electronics Cover
2. Power Supply Module
3. Fan Assembly
4. Motherboard
5. Single Screw (below ON/OFF switch)
6. Air Plenum
7. Processor PC Board (green ejector)
8. Driver PC Board (red ejector)
9. Power Supply PC Board (orange ejector)
10. Securing Screws
11. Ejector Tabs
12. Filter
13. Optical Interface PC Board
14. TTY Board (yellow)
15. Rear External Attaching Screws
16. Access Door
17. Internal Attaching Screws

994386-72

Figure 8-7. Electronics Cover Removal

8.7.2 AC Power Module Removal and Replacement

To remove the power supply module (TI Part No. 994461-0001), refer to Figure 8-8 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the printer cover and the electronics cover (see paragraph 8.7.1).
2. Loosen the single screw below the power ON/OFF switch at the rear of the printer. (Figure 8-4)
3. Loosen the four captive screws securing the power supply base to the printer base.
4. Disconnect the grounding strap at the front of the power transformer.
5. Disconnect the transformer cable connector J1 from the Motherboard.
6. Remove the power supply module.
7. To replace the power supply module, reverse the removal steps and note the following.
   a. The power supply base should remain level as the screws are tightened down.
   b. The single screws should slide smoothly into the slot in the rear.

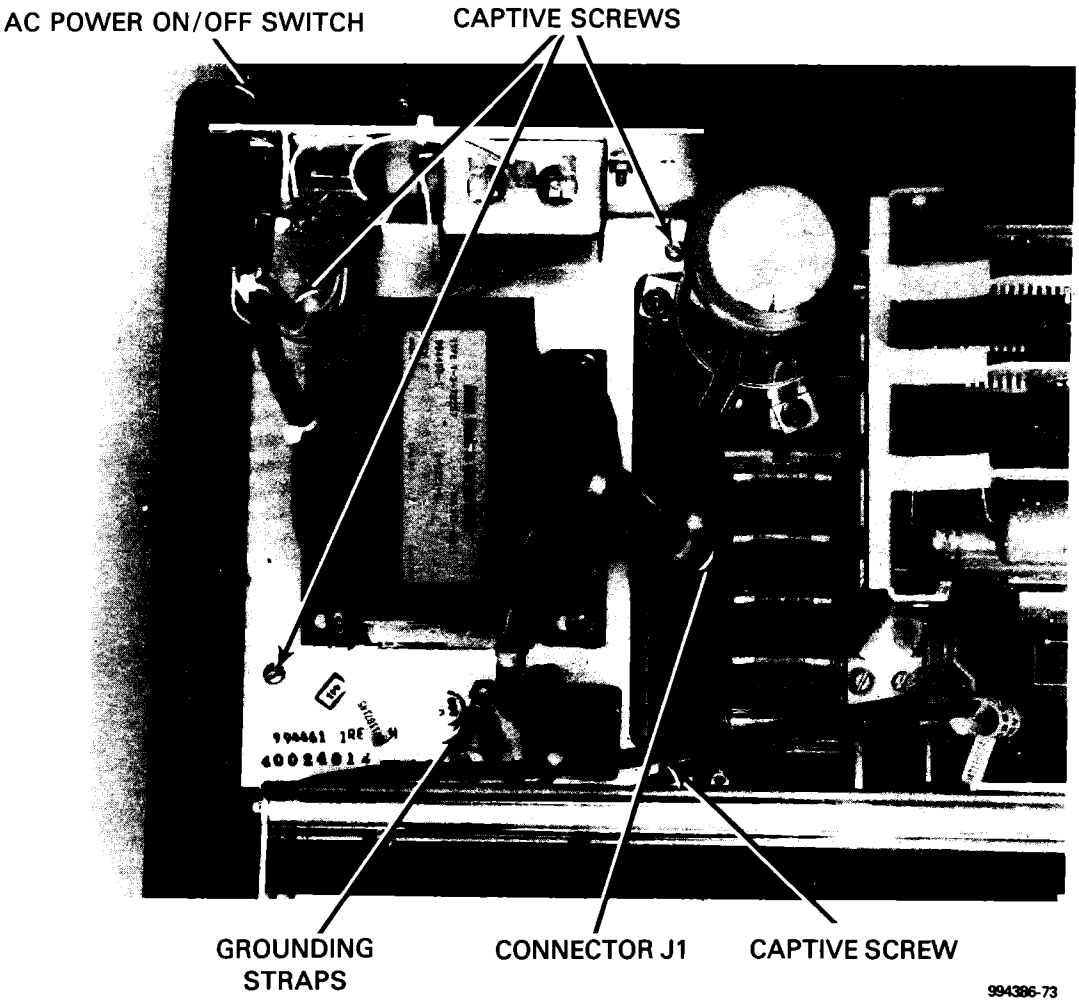


Figure 8-8. AC Power Module

8.7.3 Motherboard

To remove the Motherboard (TI Part No. 994531-0001), refer to Figure 8-9 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the printer and electronic covers and printed circuit boards (see paragraph 8.7.1).
2. Remove the power supply module (see paragraph 8.7.2).
3. Disconnect all connectors to the Motherboard.
4. Remove the six clips (seven if the center guide is present). Using needle nose pliers to help remove the clips expedites their removal.
5. Remove the left side card guide by removing the four screws at its base (two on each side).
6. Remove the Motherboard from the base.
7. To replace the Motherboard, reverse the removal steps.

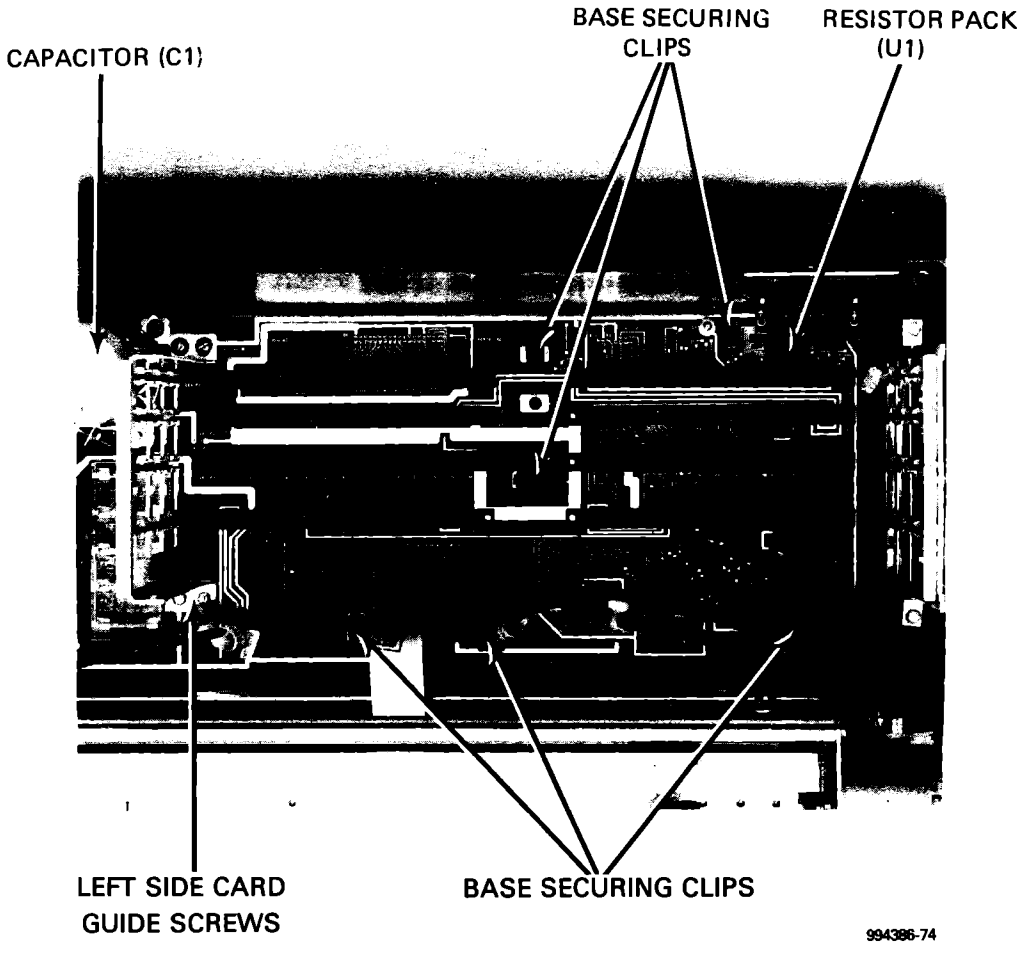


Figure 8-9. Motherboard

8.7.4 Fan Assembly

To remove the fan assembly (TI Part No. 996275), refer to Figure 8-10 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the printer and electronic covers and printed circuit boards (see paragraph 8.7.1).

2. Remove the two screws securing the fan bracket and card guide to the base.

3. Disconnect connector J9 on the Motherboard.

4. Remove the fan assembly by pulling straight up.

5. Remove the fan from the bracket and card guide by removing the four screws that fasten the card guide to the bracket and the four screws that fasten the fan to the fan bracket. If the fan is being replaced, remove the fan guard from the defective fan and attach the guard to the new fan.

6. To replace the fan, reverse the removal steps.

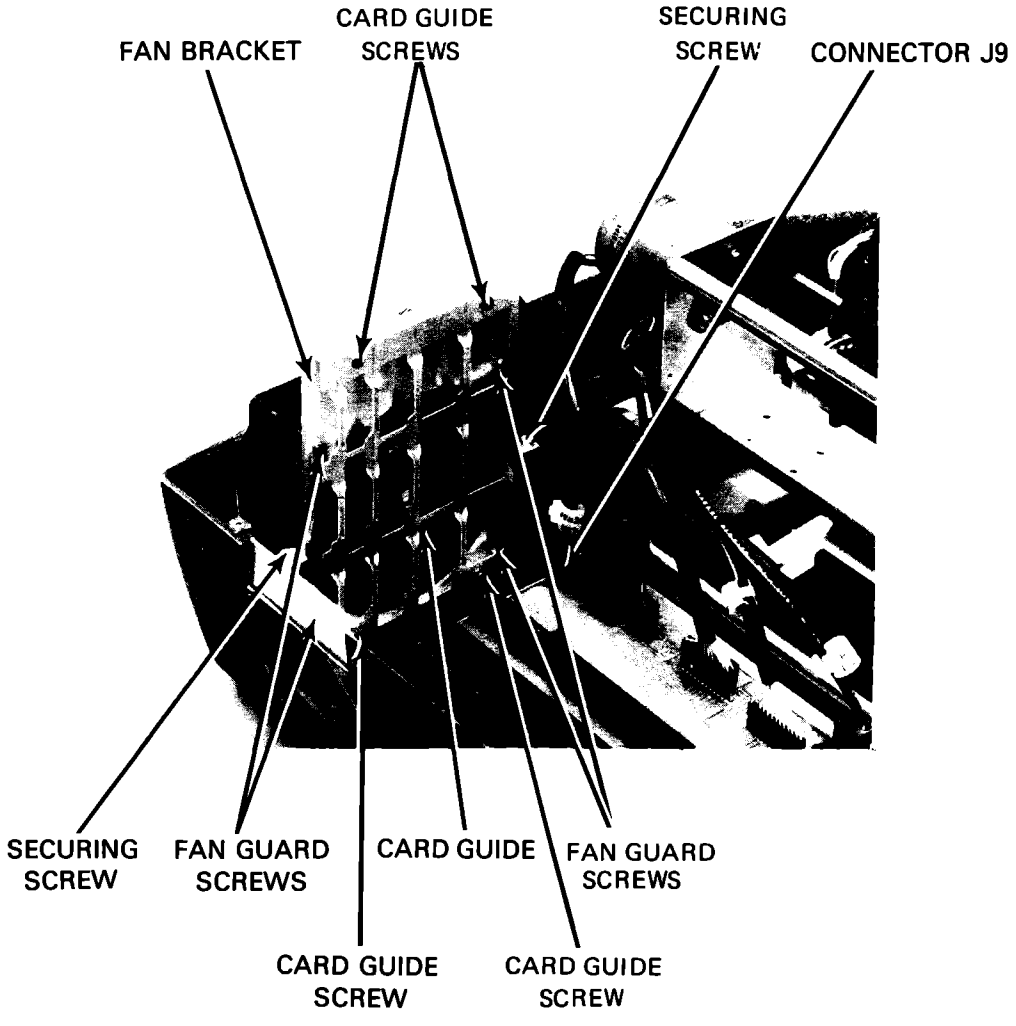


Figure 8-10. Fan, Card Guide, and Bracket

8.7.5 Paper Drive Motor Assembly

To remove the paper drive motor assembly (TI Part No. 994183), refer to figures 8-11 and 8-12 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the printer cover (see paragraph 8.7.1).
2. Disconnect connector J12 from the Motherboard.
3. Position the right paper tractor at the center of the platen.

CAUTION

To avoid possible damage to the paper advance gear, do not attempt to remove the paper drive motor screw without first sliding the paper advance gear to the left.

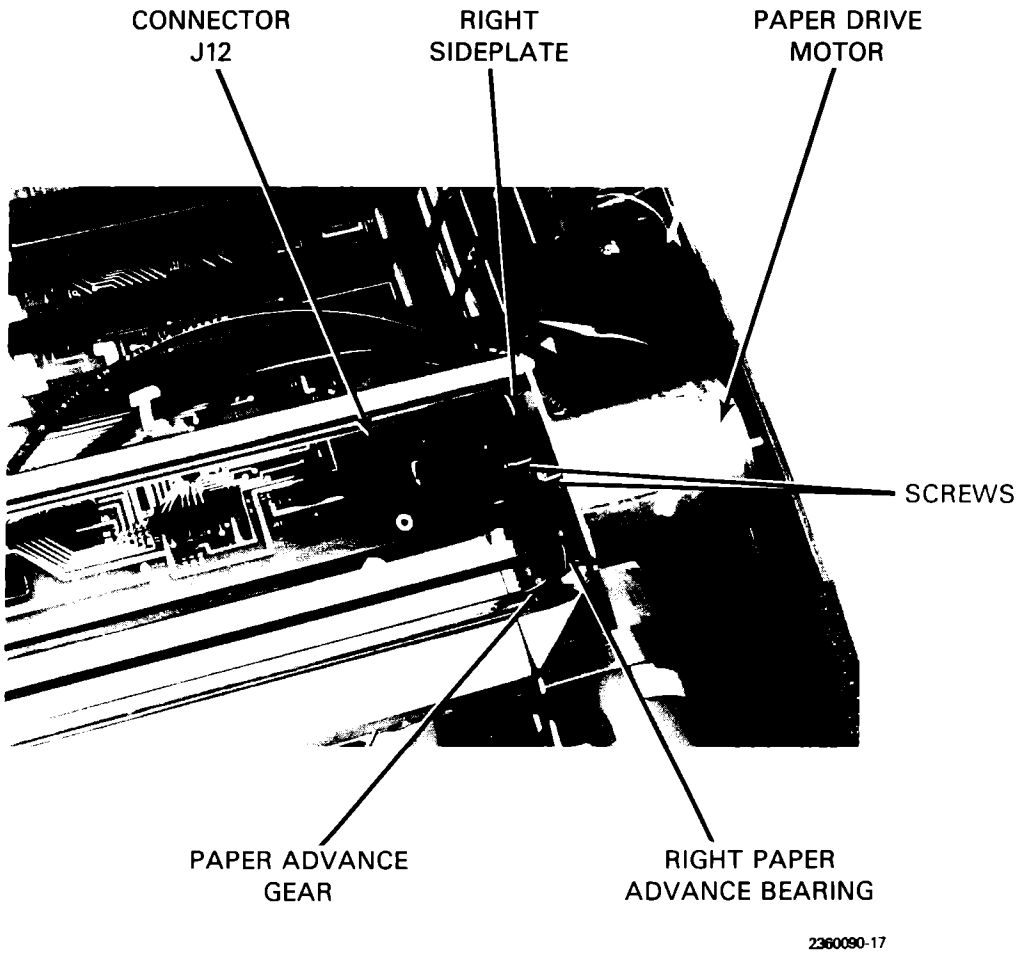


Figure 8-11. Paper Drive Motor with Gear, Connector, and Shaft

4. Remove the two sets of screws with washers and nuts securing the **left** paper advance bearing to the **left** sideplate.

5. Remove the left paper advance and bearing being careful to retain the spring inside.

6. Disengage the paper advance gear from the motor shaft by moving the tractor drive shaft to the left a few inches.

7. Remove the three screws securing the paper drive motor assembly to the right paper advance bearing and the right sideplate.

8. Remove the paper drive motor assembly.

9. To replace the assembly, reverse the removal steps.

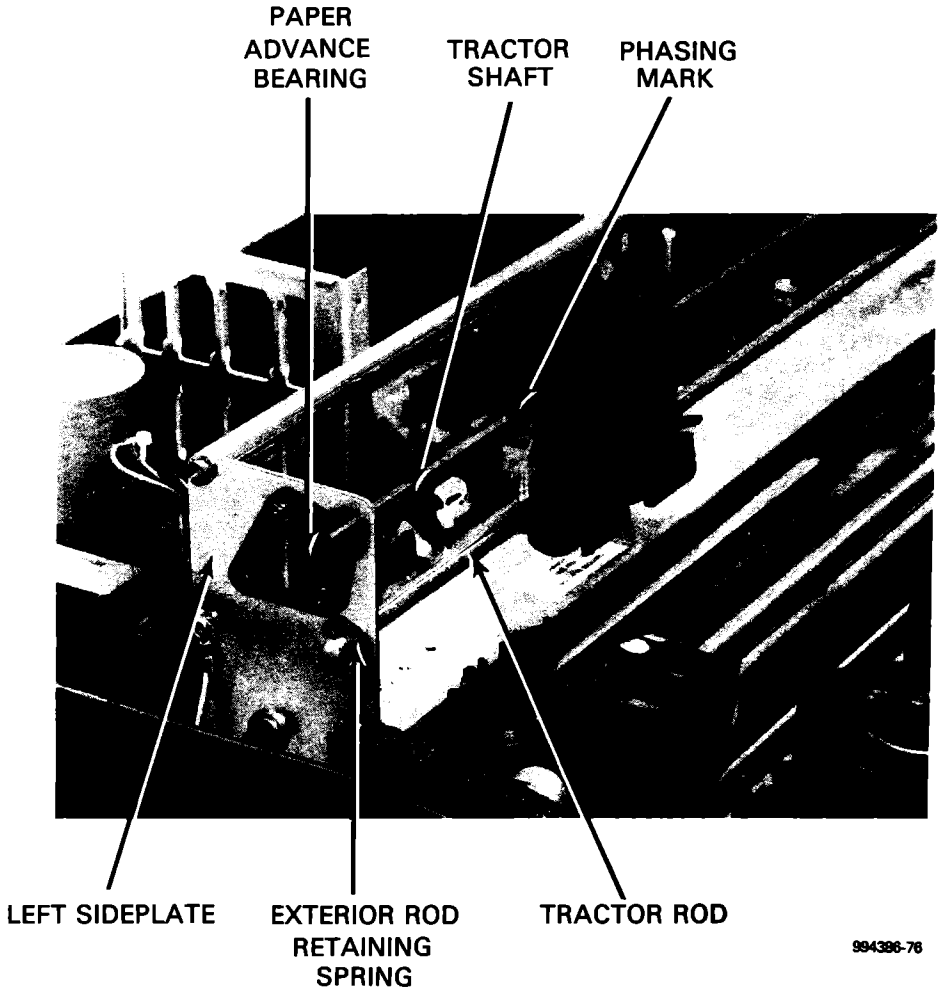


Figure 8-12. Left Paper Advance Bearing

8.7.6 Paper Tractor

To remove the paper tractors (TI Part Nos. 996158-0001, 0002), refer to figures 8-13 and 8-14 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the printer cover (see paragraph 8.7.1).
2. Note the position of the paper tractors for final realignment.
3. Pull forward on the clamps to loosen the clamps on both paper tractors and slide the tractors to the right side of the tractor drive shaft (approximately three inches from the right end).
4. Remove the two sets of nuts, washers, and screws securing the paper advance bearing to the left sideplate (Figure 8-12).
5. Remove the left paper advance hub, being careful to retain the spring inside.
6. Slide the tractor drive shaft to the left so that the right end of the shaft is removed from the tractors and the paper drive gears (Figure 8-13).

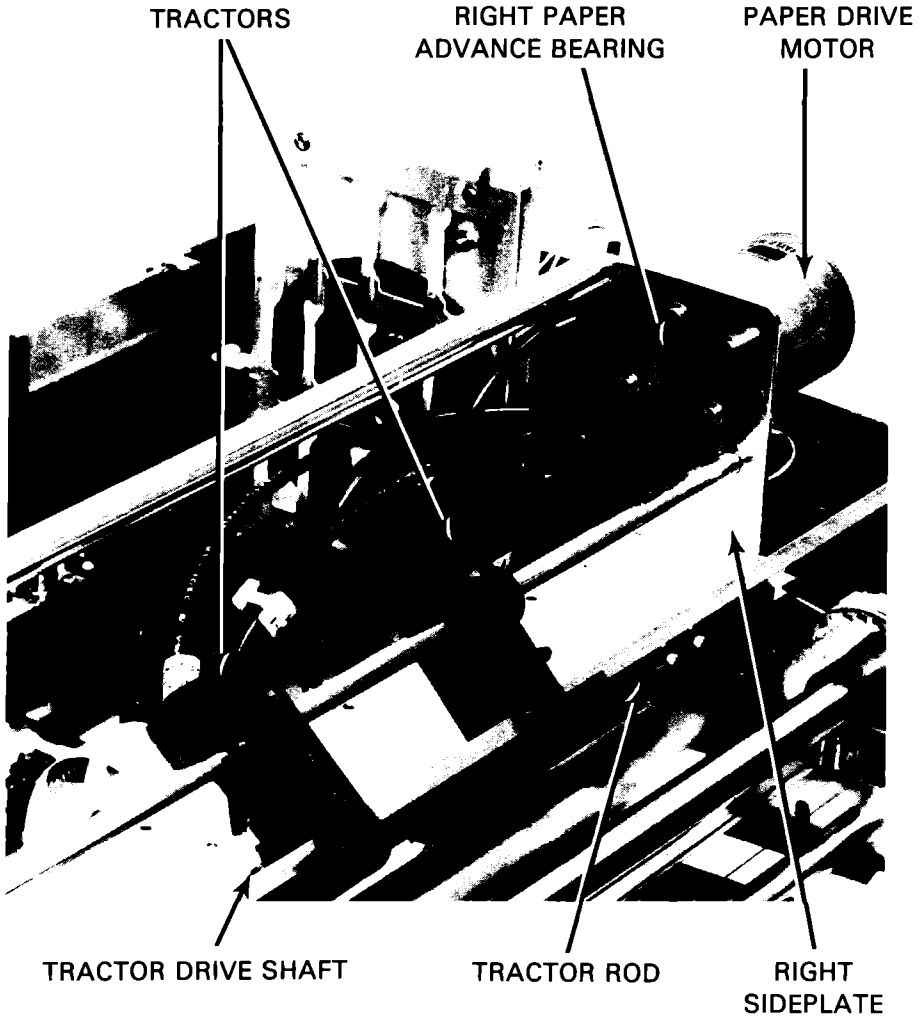


Figure 8-13. Paper Tractors Removal, Right Side View

7. Remove the exterior and interior rod retaining clips from the tractor rod (round shaft) at the left sideplate (Figure 8-14).

8. Slide the tractor rod to the left so that the right end of the rod is removed from the tractors.

9. To replace the paper tractors, reverse the removal steps and note the following.

   a. Replace the small spring in the left paper advance hub.

   b. Align the paper tractors to their original positions.

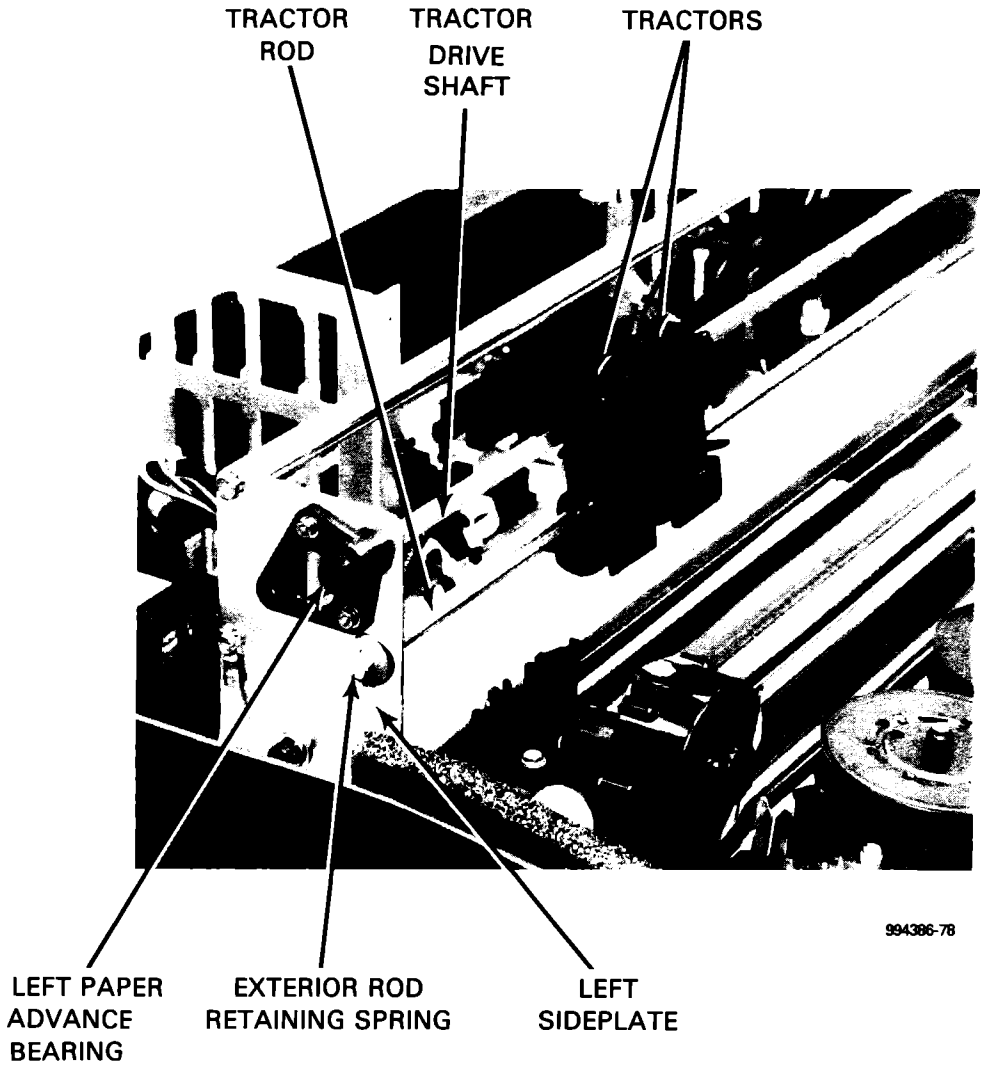


Figure 8-14. Paper Tractors Removal, Left Side View

8.7.7 Ribbon Drive Assembly

To remove the ribbon drive assembly (TI Part No. 994215), refer to figures 8-15 and 8-16 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Raise the access door.
2. Remove both ribbon reels by pulling them up.

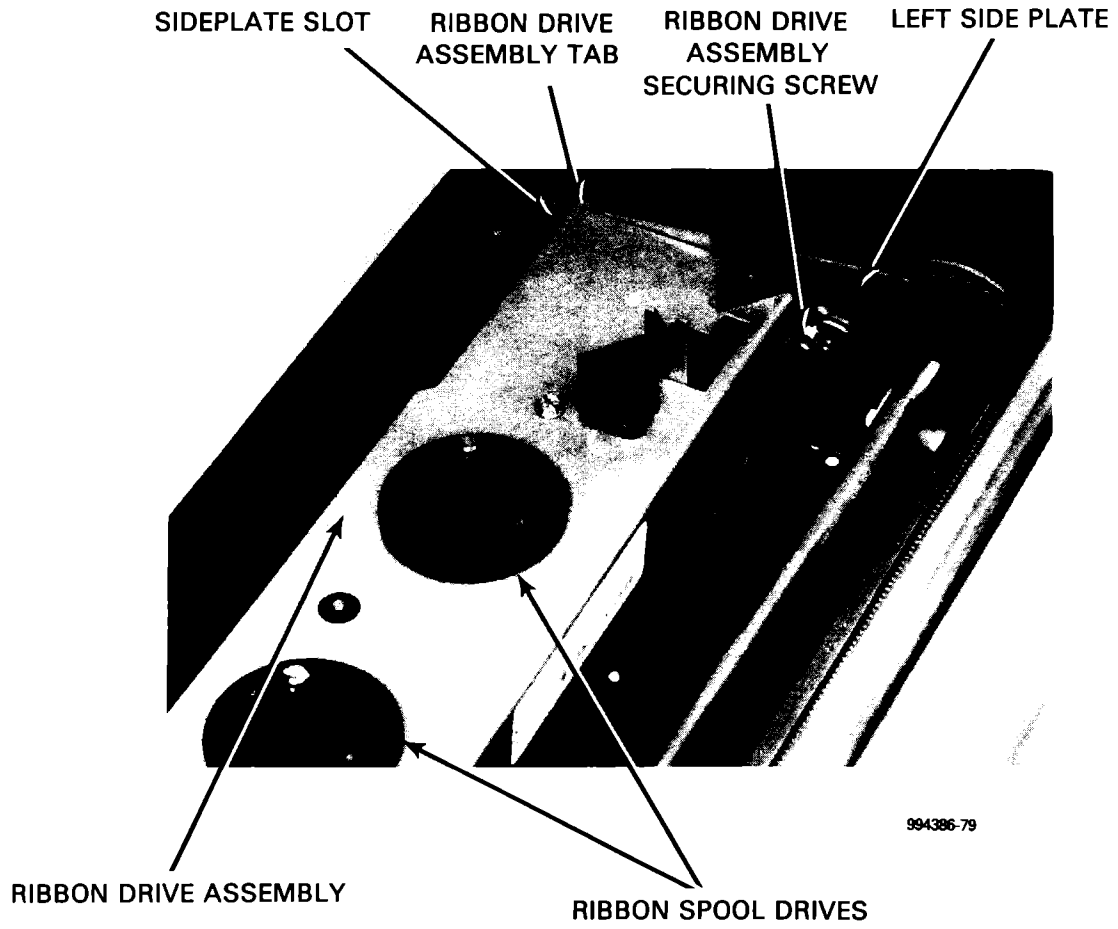


Figure 8-15. Ribbon Drive Assembly

3. Loosen the screw securing the ribbon drive assembly to the left sideplate. It is not necessary to remove the screw.

4. Slide the ribbon drive to the right to disengage the tab from the sideplate slotted hole.

5. Rotate the ribbon assembly back to disengage the securing screw from the slot. When the ribbon assembly is disengaged from the screw, the entire ribbon assembly can be moved to the right to position the plastic yokes over the indents on the lower spacer rod underneath the ribbon drive assembly.

6. Disconnect the four wires on the left front of the ribbon assembly. Also disconnect the grounding strap on the right of the ribbon assembly.

7. Remove the ribbon drive assembly by gently pulling it upward.

8. To replace the ribbon drive assembly, reverse the removal steps.

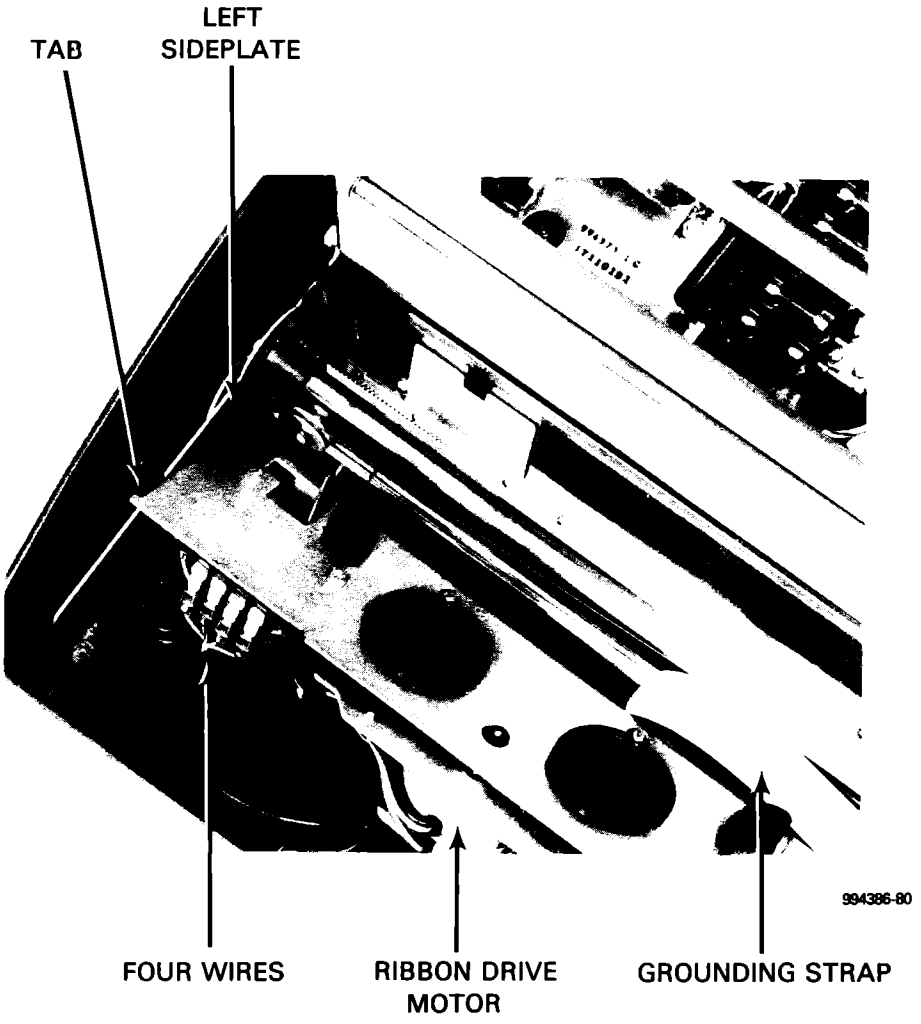


Figure 8-16. Ribbon Drive Assembly Removal

8.7.8 Main/Auxiliary Control Panel

To remove the main/auxiliary control panel assembly (TI Part No. 994555), refer to Figure 8-17 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the covers (see paragraph 8.7.1).
2. Disconnect connector J16 from the Motherboard.
3. Remove the four screws securing the control panel assembly to the base.
4. Remove the two ground straps.
5. Remove the control panel assembly.
6. To replace the main/auxiliary control panel assembly, reverse the removal steps.

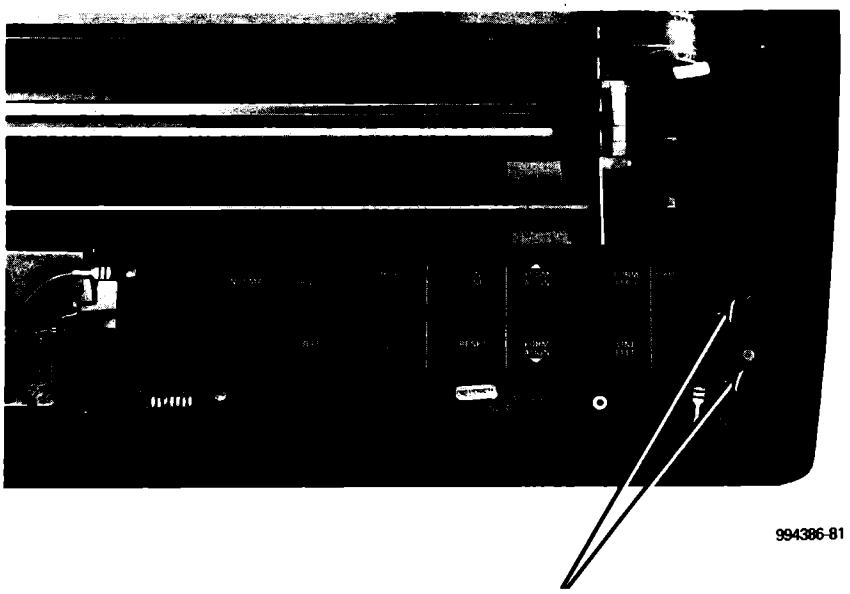


Figure 8-17. Main/Auxiliary Control Panel

8.7.9 Carriage Drive Motor Assembly

To remove the carriage drive motor assembly (TI Part No. 994546), refer to figures 8-18 and 8-19 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the cover (see paragraph 8.7.1).
2. Disconnect the two motor power leads from the motor noting the wire color location to ensure correct replacement.
3. Disconnect the blue encoder sensor cable from the Motherboard (connects to J8).

Figure 8-18. Carriage Drive Motor

4. Push the idler pulley support girder to the right allowing the detent in the bottom of the girder to latch on the right sideplate.*

5. Remove the wire rope from the capstan by disengaging the end of the wire rope from either end of the capstan and unwrapping the wire rope.

6. Loosen the motor strap retaining screw by turning it two or three times. Use a long screwdriver (6-8 inches).

7. Press down on top of the motor strap to disengage the motor strap from the right sideplate.

8. Remove the screw securing the carriage drive motor assembly to the cradle and remove the carriage drive motor assembly.

9. Remove the screw securing the ground wire to the motor.

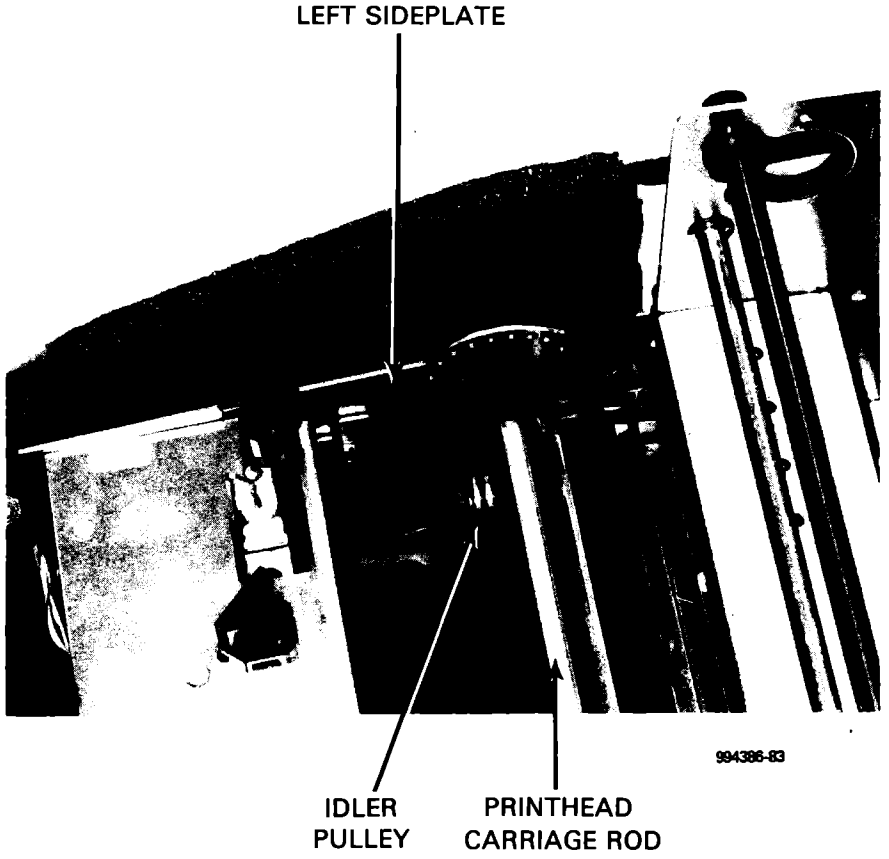


Figure 8-19. Idler Pulley

* This girder, to which the idler pulley is attached, is located beneath the printhead carriage rod and extends from the left sideplate to the right sideplate. Because it is held in place by a long spiral spring (this spring can be seen by looking down behind the printhead carriage), it requires a definite effort to move it the required ¼ inch to the right.

10. To replace the carriage drive motor assembly, reverse the removal steps noting these instructions for rewinding the wire rope.

    a. Move the carriage to the left stop.

    b. Bring the wire rope from the left side of the carriage around the idler pulley and back through the lower slot in the right sideplate.

    c. Bring the wire rope from the right side of the carriage through the upper slot in the right sideplate, and (with the innermost capstan slot in the up position) place the end of the wire rope in the slot.

    d. Wrap the wire rope counterclockwise (or allow the wire rope to follow the capstan groove while turning the capstan clockwise) 6½ turns. The outermost capstan slot should be in the up position.

    e. Bring the lower portion of the wire rope counterclockwise around the capstan 1½ turns (the rope ends in the outermost capstan slot).

    f. Carefully release the idler pulley support from the detent.

    g. Manually move the carriage from stop to stop to remove the wire rope slack in the capstan.

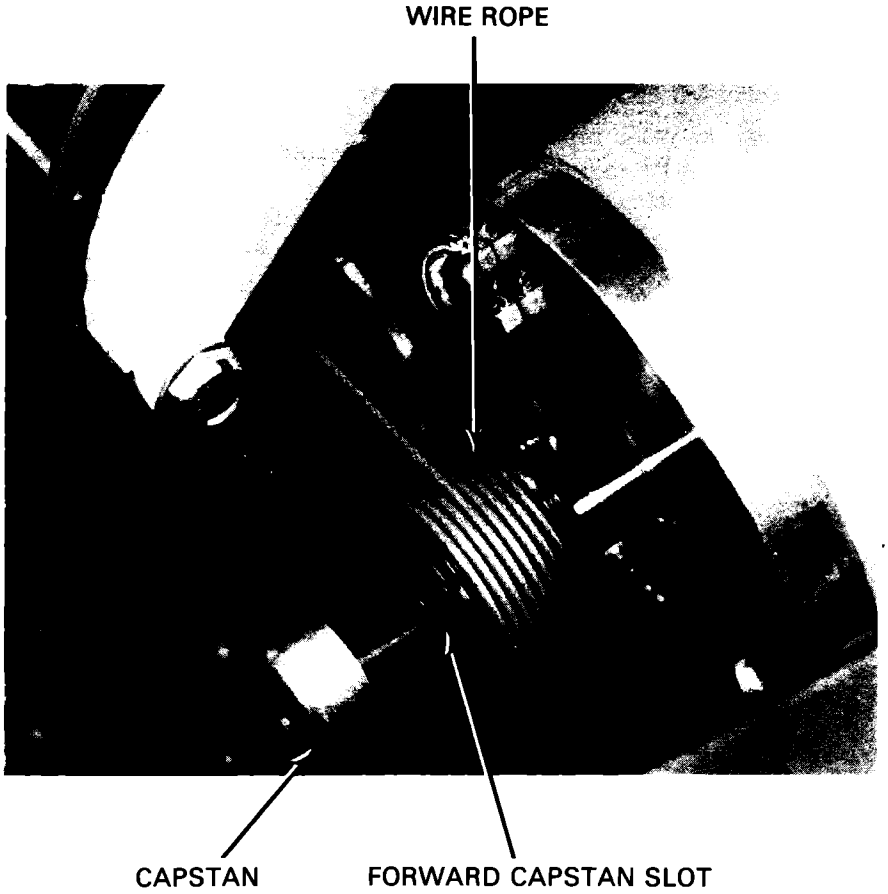


Figure 8-20. Wire Rope Detail 994386-84

8.7.10 Wire Rope

To remove the wire rope, refer to Figure 8-20 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the cover (see paragraph 8.7.1).
2. Move the carriage to the left sideplate.
3. Push the idler support girder to the right, allowing the detent in the bottom to latch on the right sideplate.
4. Remove the printhead (see paragraph 8.5.3). Loosen the two screws securing the wire rope to the printhead carriage so that the wire rope can be slipped out.
5. Remove the wire rope from the capstan by disengaging the end of the wire rope from either end of the capstan and unwrapping the wire rope.
6. To replace the wire rope, move the carriage to the left stop.
7. Bring the wire rope from the left side of the carriage around the idler pulley and back through the lower slot in the right sideplate.
8. Bring the wire rope from the right side of the carriage through the upper slot in the right sideplate, and (with the innermost capstan slot in the up position) place the end of the wire rope in the slot.
9. Wrap the wire rope counterclockwise 6½ turns. The outermost capstan slot should now be in the up position.
10. Wrap the lower portion of the wire rope counterclockwise around the capstan 1½ turns and place the end in the outermost capstan slot.
11. Carefully release the idler pulley support from the detent.
12. Turn the capstan to the extreme counterclockwise position (the rear capstan slot is up) to set the wire rope.
13. Turn the capstan once clockwise.
14. Holding the capstan and the wire rope stationary, move the carriage to the extreme left side of the printer and tighten the two screws securing the wire rope clamp to the carriage.

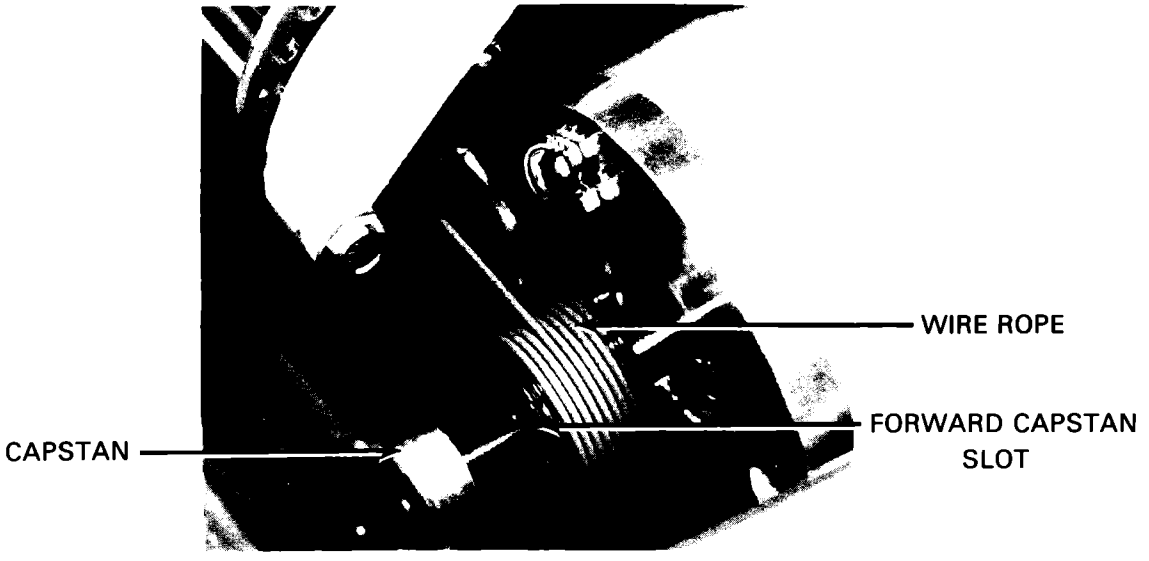


Figure 8-20a. Wire Rope Detail 994386-85

8.7.11 Carriage and Paper Drive Assembly

To remove the carriage and paper drive (TI Part No. 994183), refer to figures 8-21 and 22 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the cover (see paragraph 8.7.1).
2. Remove the printhead (see paragraph 8.5.3).
3. Remove the ribbon drive (see paragraph 8.7.7).

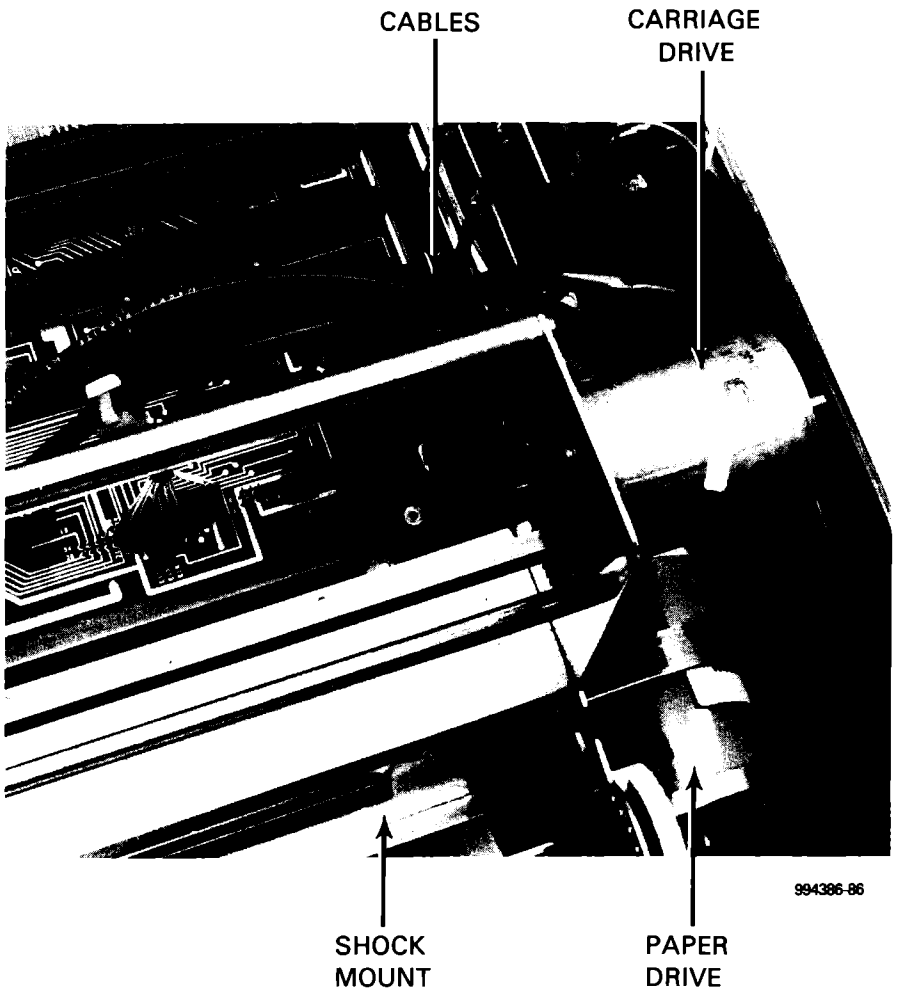


Figure 8-21. Carriage and Paper Drive Assembly

4. Unplug the carriage drive motor cable from the motor, the encoder sensor cable from the Motherboard, the paper advance motor cable from the Motherboard, and the paper-out cable (Figure 8-22) from the switch.

5. Remove the clip and the flex cable from the wire rope clamp and remove the left sideplate ground jumper connection from the power module ground stud.

6. Remove the four nuts (two on the studs through the lower front spacer and two on the studs through the lower rear spacer) and lock the washers that fasten the drive assembly to the shock mounts.

7. Carefully lift the drive out of the case by pulling up on the upper spacer (and lower the front spacer, if required). Do not pull on the tractor drive shaft (¼-inch square rod). Care should be used to prevent snagging the cables during removal.

8. To replace the carriage and paper drive assembly, reverse the removal steps.

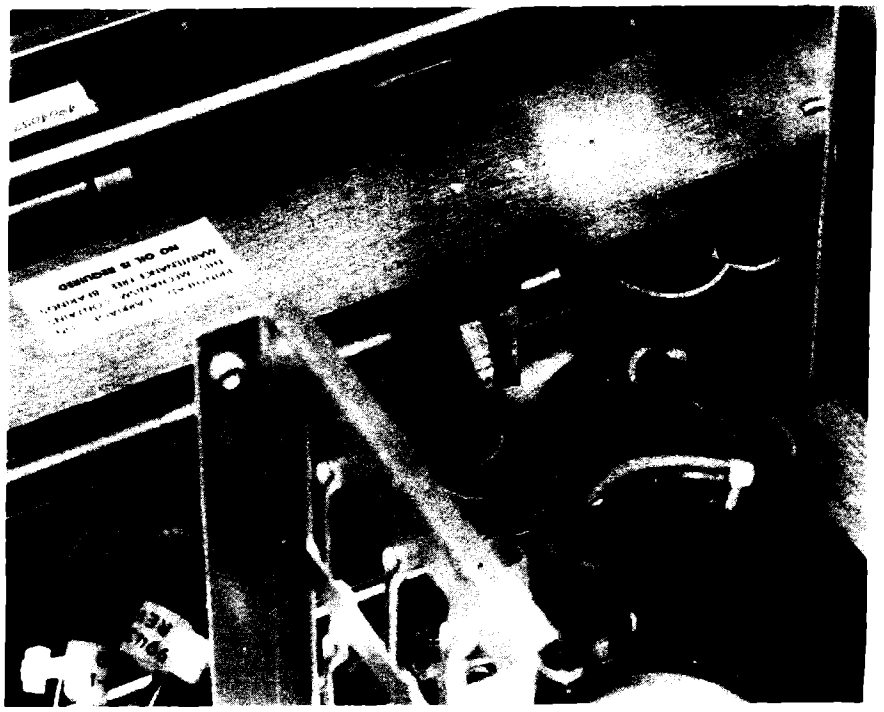


Figure 8-22. Paper-Out Switch

994386-87

8.7.12 Secondary Fuses

To remove a secondary fuse, refer to Figure 8-23 and proceed as follows.

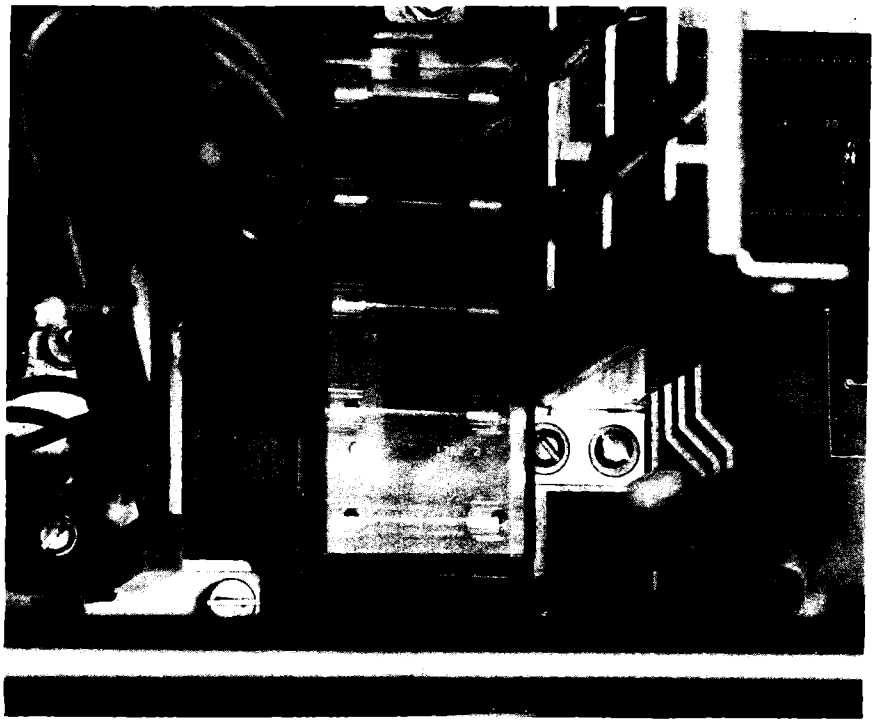
WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the printer cover and electronics cover (see paragraph 8.7.1).
2. Locate the secondary fuses between the printed circuit boards and the ac power supply.
3. Disconnect connector J1 from the power supply to the Motherboard.
4. Remove the fuse cover by pressing in at the ends and pulling upward.
5. Replace fuses as required.

Fuse	Rating	TI Part No.
F1	1A, 250 V	416434-0103
F2	3A, 125 V	411787-0012
F3	1A, 250 V	416434-0103
F4	1A, 250 V	416434-0103
F5	1.5A, 250 V	416434-0150

6. Replace the fuse cover, connector J1, the electronics cover, and the printer cover.



994386-88

Figure 8-23. Secondary Fuse Area

8.8 +5 VDC REGULATOR ADJUSTMENTS

The following adjustment procedure for the printer should be performed by qualified service personnel.

To adjust the +5 Vdc regulator output to its required level, perform the following procedure.

1. Remove the covers (see paragraph 8.7.1).
2. Adjust R13 (the upper right area of the power supply board) to obtain an output at E10 of +5 Vdc +10 mV.
3. Replace the covers.

8.9 TESTING

To test the printer with power ON (see paragraph 3.4.3), proceed as follows.

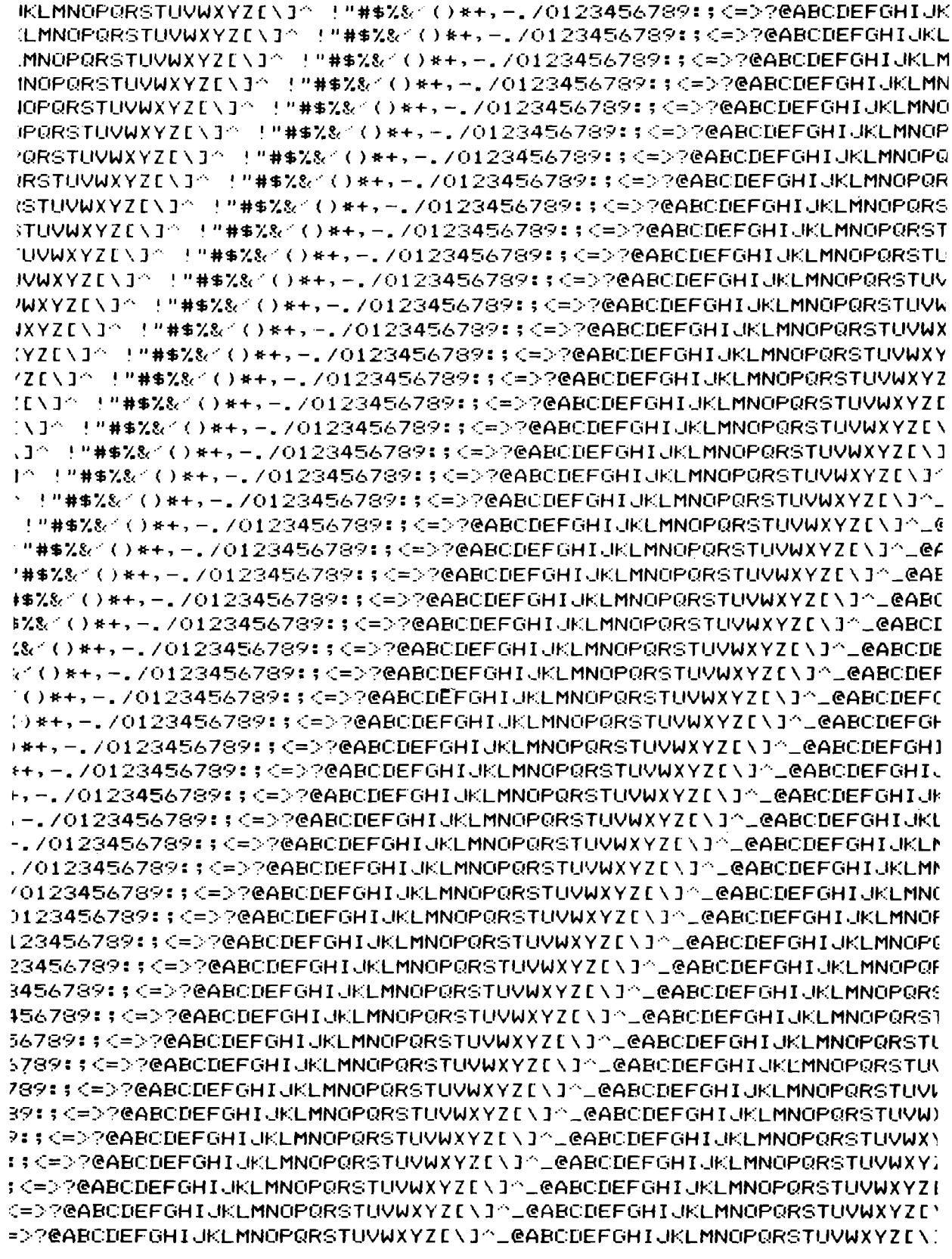
CAUTION

To prevent damage to the printhead, do not print without a ribbon or on paper too narrow for the printed line width. If the full 132-column line is used, the paper must be at least 278 mm (14-7/8 inches) wide for the standard 10 characters per inch spacing and at least 216 mm (8-½ inches) wide for the optional FCO and VCO printers only (16.5 characters-per-inch compressed print spacing).

1. Open the access door.
2. Ensure that pencil switches are not set for parallel operation.
3. Press the control panel TEST/VFC switch.
4. Press the control panel ONLINE switch and observe that the rotating character pole starts (see Figure 8-24).
5. Check that the entire 64-character (or optional 95-character) set is printed for each line.
6. After several lines have been printed and checked, press the control panel NORMAL switch and observe that the barber-pole stops.

NOTE

This procedure tests approximately 90 percent of the printer components.



994386-89

Figure 8-24. Test Barberpole Printout

Table 8-2. Option PROM TI Part Number and Location

Option \ Processor	0001 Processor (0994244) Required Option Device(s)			0002 Processor (0994244) Required Option Device(s)		
	Part Number	Device	Socket	Part Number	Device	Socket
U.S. Full ASCII	0994434-0010	PROM	XU67	0994434-0019	PROM	XU67
U.S. LTD.ASCII, VFC[1]	0994273-0001 0996203-0001	PROM RAM	XU55 XU25	0994434-0100 0996203-0001 0996279-0005	PROM RAM ROM	XU67 XU25 XU42
U.S. Full ASCII with VFC[1]	0994434-0010 0994273-0001 0996203-0001	PROM PROM RAM	XU67 XU55 XU25	0994434-0119 0996203-0001 0996279-0005	PROM RAM ROM	XU67 XU25 XU42
Expanded Character	Expanded Character Option is not applicable to Processor 0994244-0001			0994434-0008	PROM	XU67
Expanded Character with VFC[1]	Expanded Character Option is not applicable to Processor 0994244-0001			0994434-0108 0996203-0001 0996279-0005	PROM RAM ROM	XU67 XU25 XU42

NOTES:
(1) VFC options require battery 0996371-0001 (Mallory PX14 or equiv.) installed in processor battery retainer. Install battery with positive (+) pole toward board.

TI Part No. 994521-9701

Appendixes

- A — Dot Matrix Character Generation
- B — ASCII Control and Character Codes
- C — Model 810 Printer Versions, Options, and Accessories
- D — TMS 8080A Microprocessor
- E — TMS 5501 I/O Controller
- F — Installation of Option Kits
- G — TMS 6011 Data Sheets
- H — Cable Pin Assignments
- I — U.S. ASCII/Katakana Dual Character Set
- J — Strappable Options for Processor and Line Buffer Boards
- K — Theory of Operation for Drive Board (TI Part No. 994322) and Power Supply (TI Part No. 994394)
- L — First-Generation Front Panels and Carriage Motor Assembly

Appendix A

Dot Matrix Character Generation

Dot matrices of available character sets for the Model 810 printer are included in this appendix. Ordering information is contained in Appendix C.

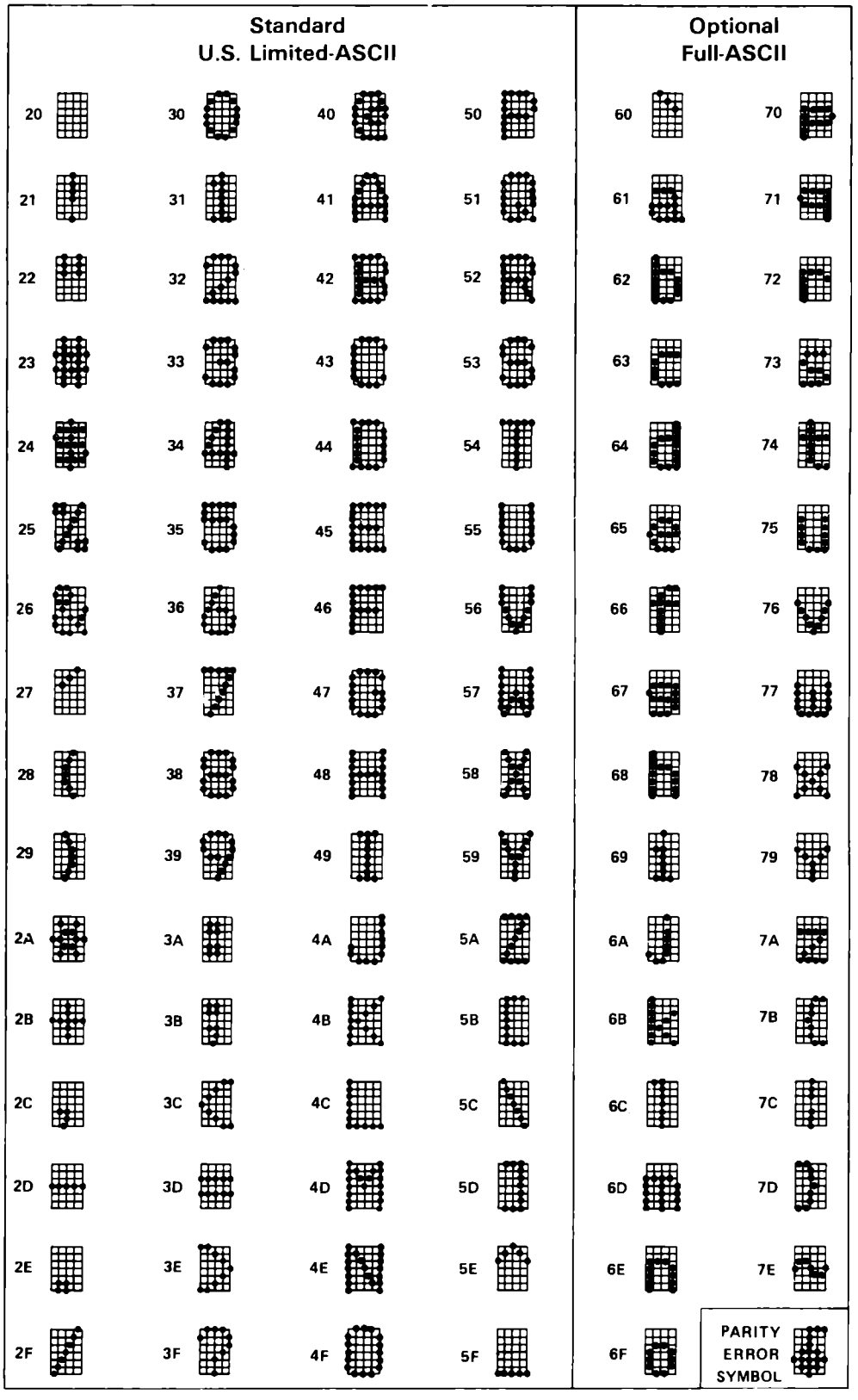


Figure A-1. U.S. Character Set (Standard and FUL) 99438c 91

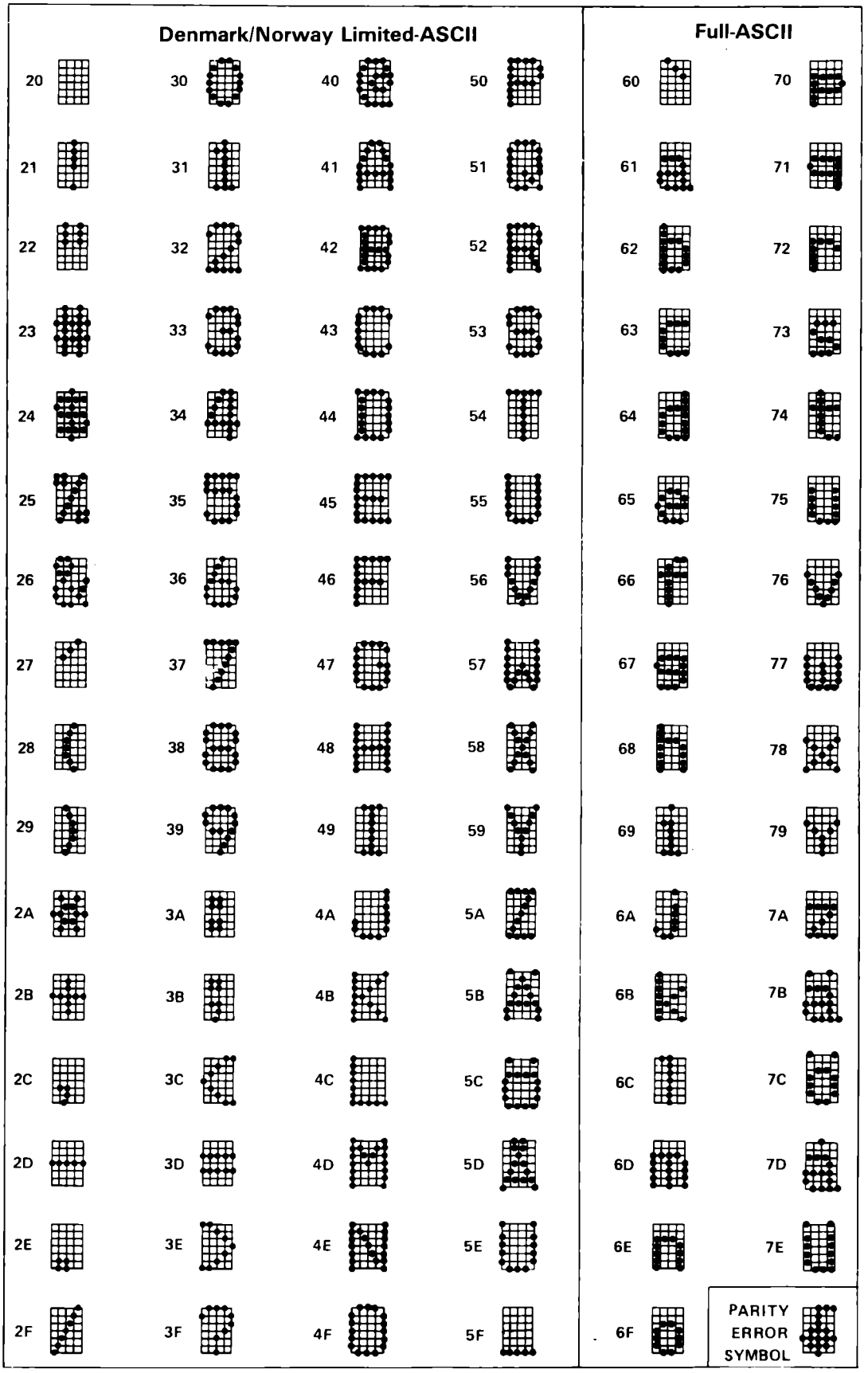


Figure A-2. Denmark/Norway Character Set (DNL and DNF) 994386-92

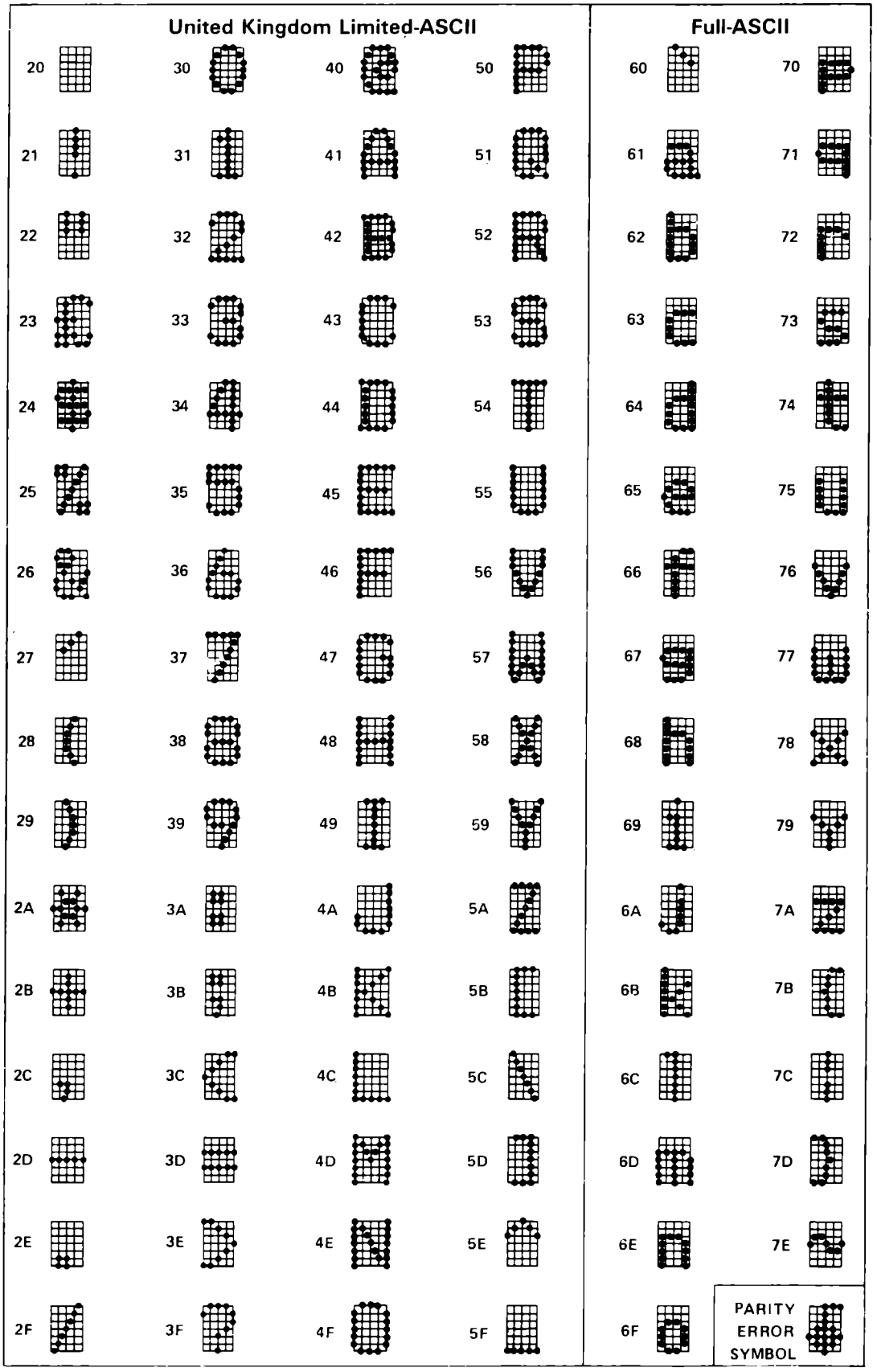


Figure A-3. United Kingdom Character Set (UKL and UKF) 994386-93

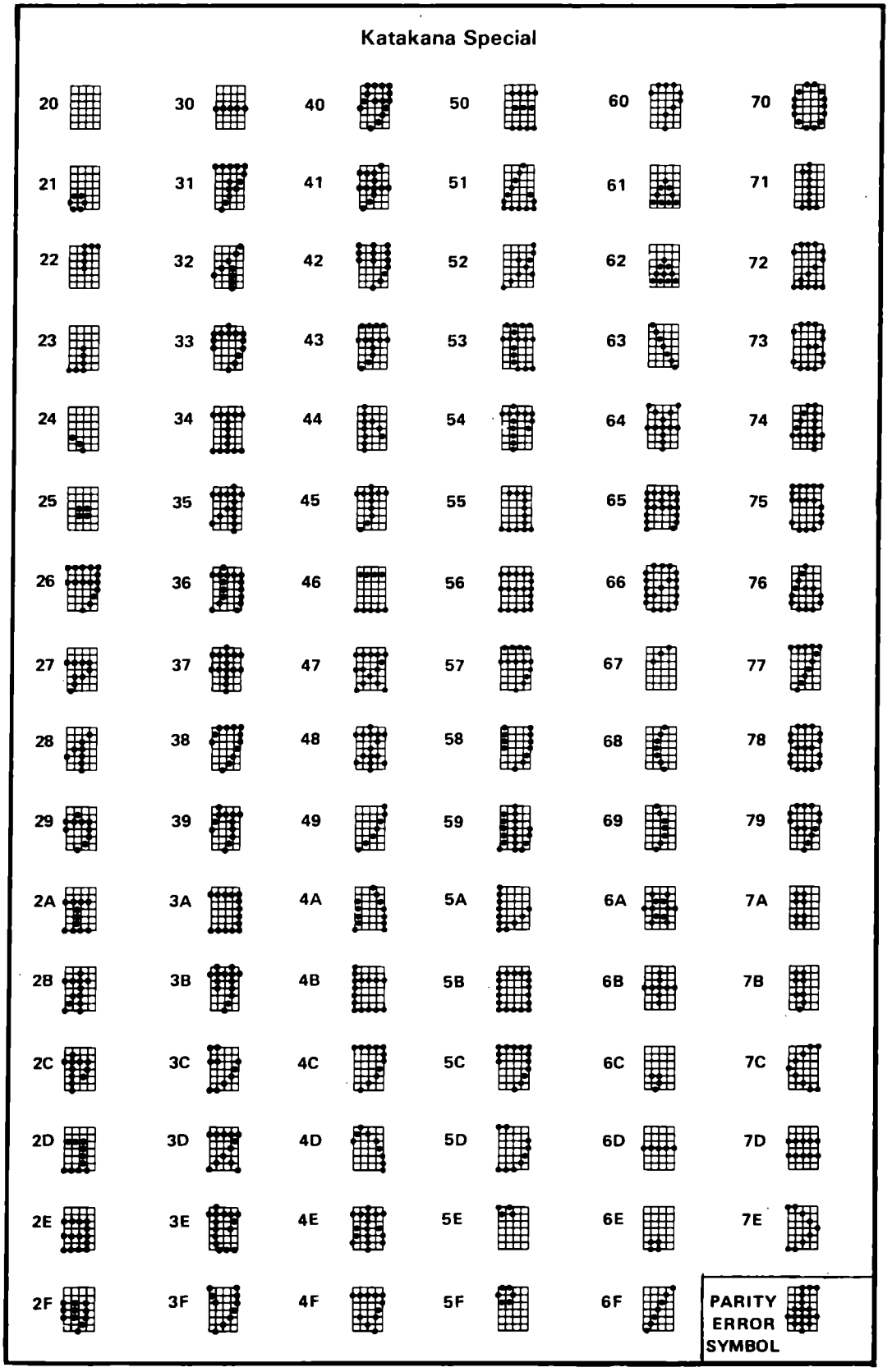


Figure A-4. Katakana Special Character Set (KTS)

994386-94

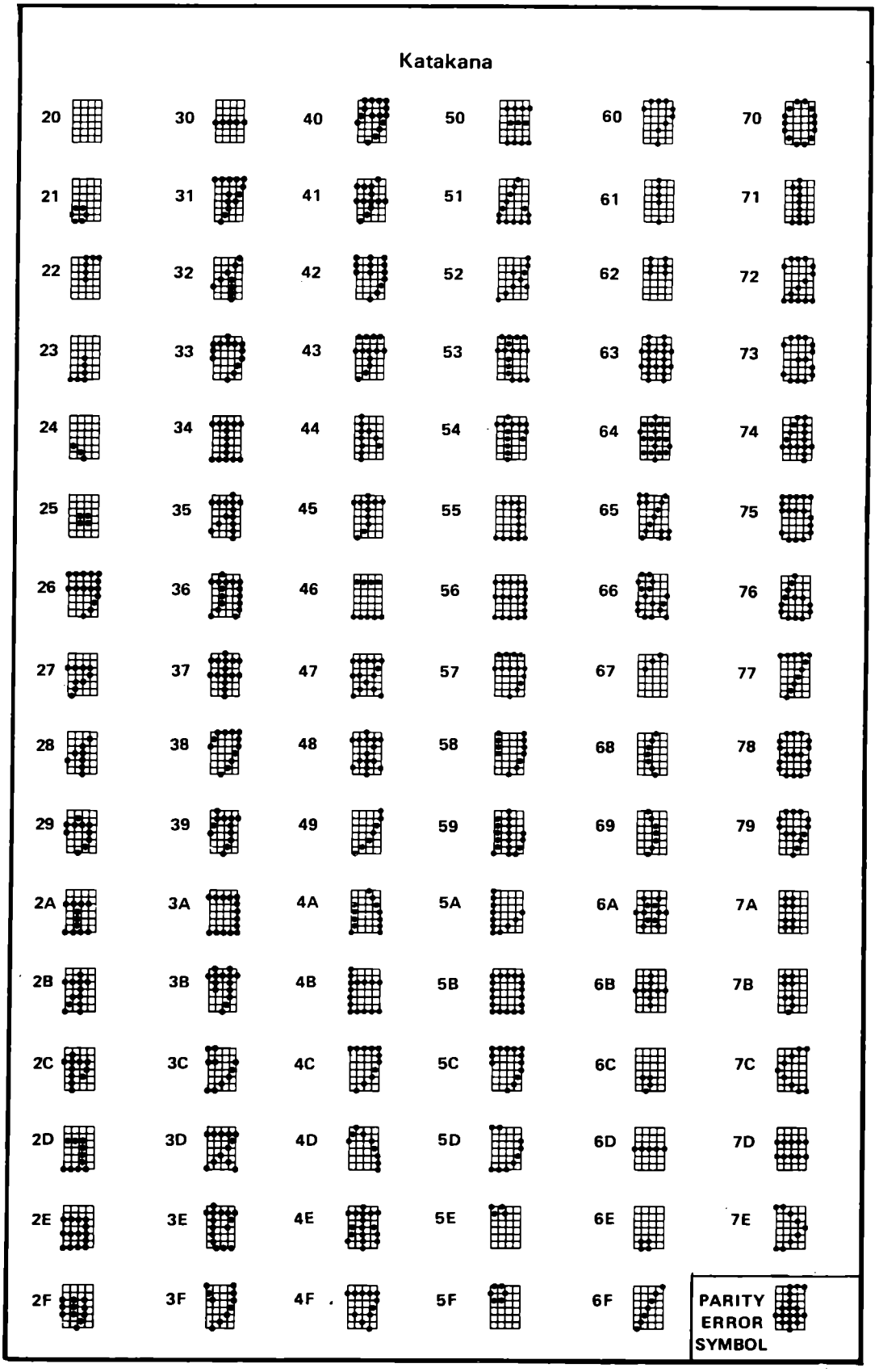


Figure A-5. Katakana Character Set (KAT)

994386-95

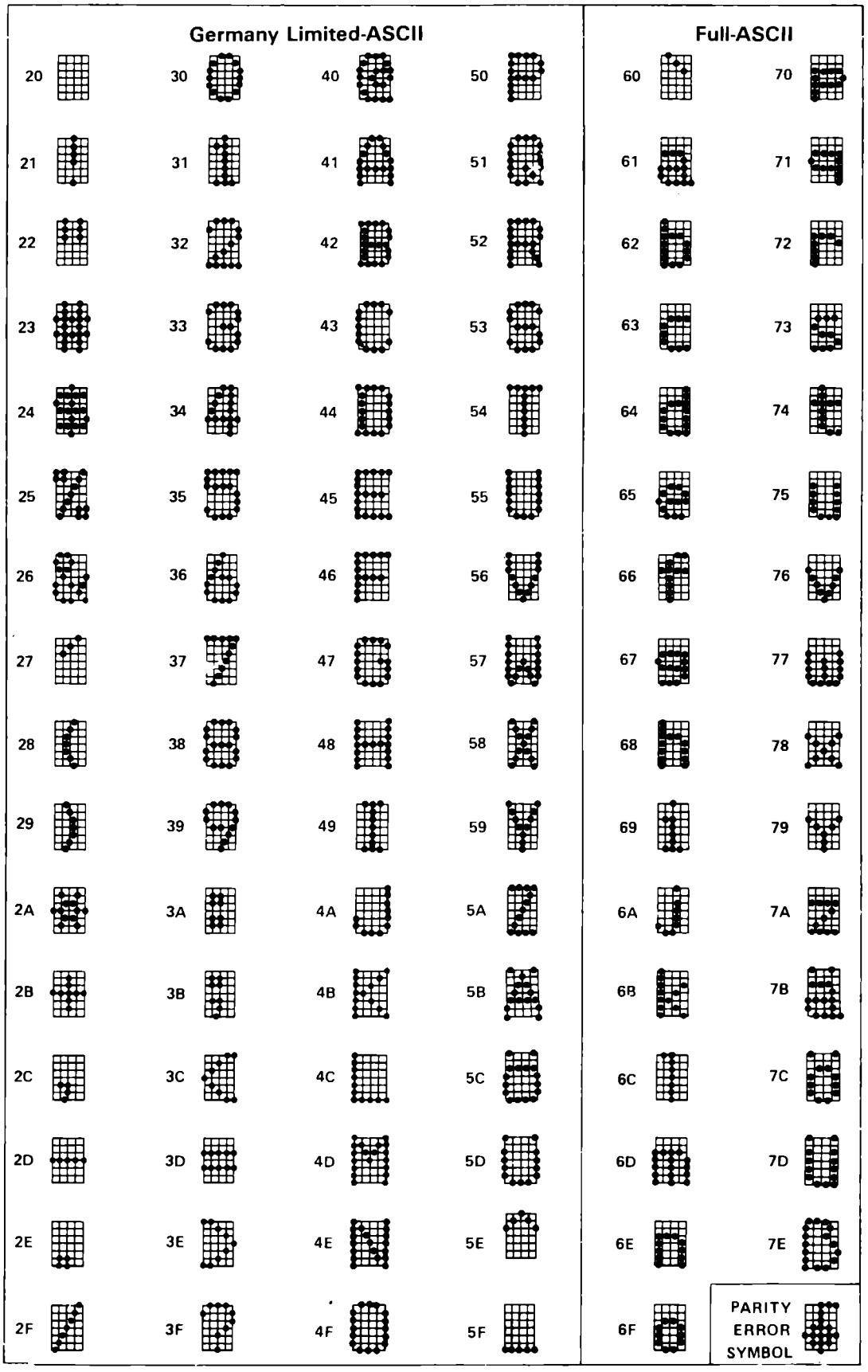


Figure A-6. Germany Limited Character Set (GRL and GRF)

994386-96

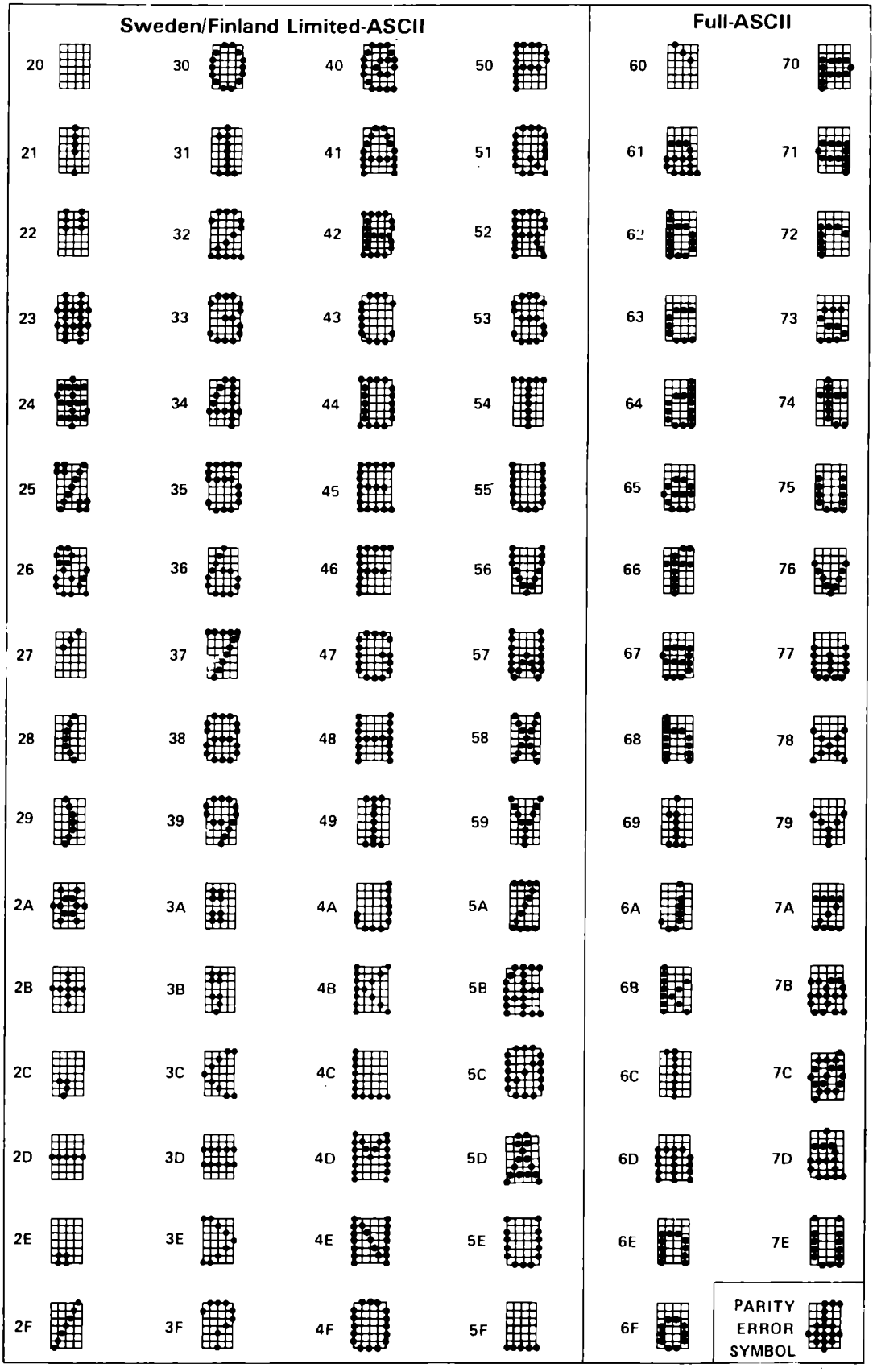


Figure A-7. Sweden/Finland Limited Character Set (SWL and SWF) 994386-97

Spanish Character Set
(ASCII)

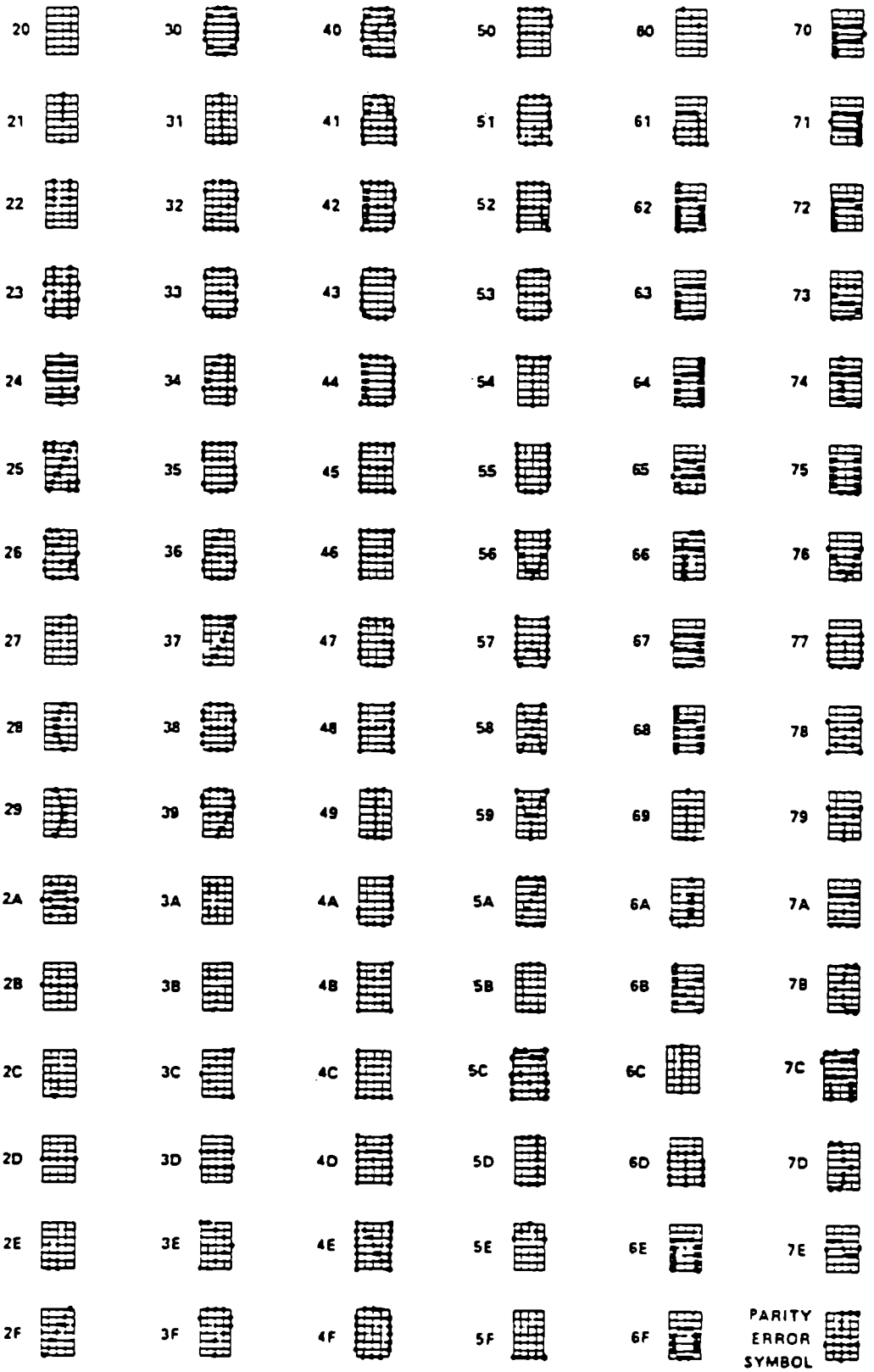
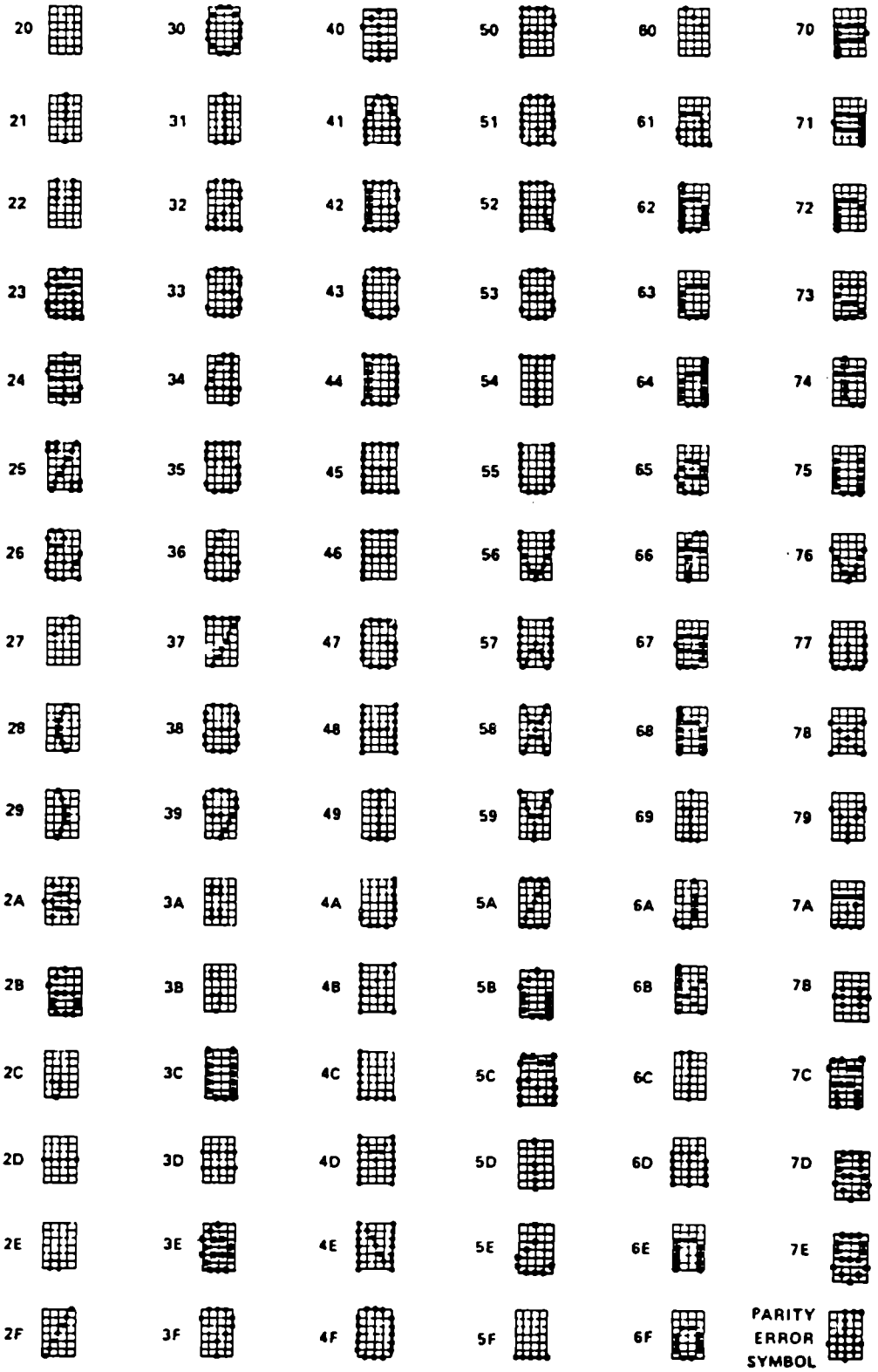


Figure A-8. Spanish Character Set (ASCII)

994386-98

Spanish Character Set (Text Editing)



994386-99

Figure A-9. Spanish Character Set (Text Editing)

Appendix B

ASCII Control and Character Code

The standard Model 810 printer character set is the limited-ASCII, 64-printable-character set. The full-ASCII set of 95 printable characters is offered as an option. If a character from the optional character list (b7, b6, b5 = 111 or 110) is received by a printer with the limited-ASCII configuration, the corresponding uppercase character from b7, b6, b5 = 101 or 100 will be printed. The following table describes the ASCII code and character set recognized by the printer. (Other character sets can be substituted.)

						CONTROL CODE		STANDARD CHARACTERS				OPTIONAL CHARACTERS (EXCEPT DEL)	
b7 →						0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
Bits ↓	b4	b3	b2	b1	Column / Row	0	1	2	3	4	5	6	7
	0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	11	VT	ESC	+	;	K	[	k	{
	1	1	0	0	12	FF	FS	,	<	L	\	l	¦
	1	1	0	1	13	CR	GS	—	=	M	]	m	}
	1	1	1	0	14	SO	RS	.	>	N	^	n	~
	1	1	1	1	15	SI	US	/	?	O	_	o	DEL

*Shaded boxes indicate control codes not recognized by the Model 810 printer

Control Codes Recognized by Model 810 Printer:

BEL	bell
BS	backspace
CR	carriage return
DC1	select printer
DC2	tab to line
DC3	deselect printer
DC4	tab to address
DEL	delete
ESC + 1	set vertical tabs
ESC + 2	set form length
ESC + 3	set horizontal tabs
ESC + 4	set 6 lines/inch
ESC + 5	set 8 lines/inch
ESC + 6	set 10 characters per inch
ESC + 7	set 16.5 characters per inch (optional)
ESC + 8	store vertical format (optional)
ESC + 9	recall vertical format (optional)
ESC + :	select line width
ESC + ;	set full line width
FF	form feed
HT	horizontal tab
LF	line feed
NUL	null
SI	shift in (optional)
SO	shift out (optional)
VT	vertical tab

Appendix C

Model 810 Printer Versions, Options, and Accessories

C.1 GENERAL

This appendix describes the Model 810 printer versions and optional available equipment. To assist the reader in interpreting the data in the tables, a list of designations and their definitions is presented in Table C-1.

Table C-1. List of Designations

Designation	Definition	Designation	Definition
BSC	Basic	LBP	Line Buffer Parallel
DNB	Data (Terminal) Not Busy	LBT	Current Loop I/F
DNF	Danish-Norwegian, Full[1]	NDE	Non Delete Recognition
DNL	Danish-Norwegian, Ltd.[2]	BRO	Baud Rate Option
DTR	Data Terminal Ready	PLT	Parallel I/F
EXP	Expanded Limited	SPF	Spanish, Full[1]
FLC	Form Length Control	SPT	Spanish Text Edit, Full[1]
FCO	Form Length + Compressed Print	SWF	Swedish, Finnish Full ASCII
FUL	Full ASCII	SWL	Swedish-Finnish Limited
GRF	German Full	TTY	Current Loop
GRL	German Limited	UKF	United Kingdom—Full ASCII
IRC	Inverse Reverse Channel	UKL	United Kingdom—Limited
ISC	Signal Ground Isolated from Chassis Ground	VFC	Vertical Format Control
KAT	Katakana	VCO	Vertical Format Control Plus Compressed Print
KTS	Katakana Special	DCO	Disable Control Option (DC1 and DC3)
LBE	Line Buffer EIA		

[1]Full ASCII = 95 printable characters
[2]Limited ASCII = 64 printable characters

C.2 STANDARD PRINTERS

Model 810 printers that are standard (without options) come with the following characteristics:

1. Domestic power cord
2. EIA-232-C interface
3. Limited ASCII character set
4. Recognition of "DELETE" character
5. Data terminal ready = ONLINE
6. Secondary request to send (reverse channel): + EIA level = READY: − EIA level = BUSY.
7. 120V AC power supply
8. Signal ground and chassis ground connected

C.3 MODEL 810 PRINTER EQUIPMENT LISTS

Tables C-2, C-3, and C-4 list available equipment, TI part numbers, and letter designations.

Table C-2. Printer Versions

Description	Part Number	Designation
Printer Assembly		
810 printer (basic)	0994292-0001	BSC
100 V		100
220 V		220
240 V		240
Non-Recognition of DELETE Character		NDE
DTR = ONLINE and NOT BUSY		DNB
Inverse Reverse Channel		IRC
810 printer (forms length)	0994292-0002	FLC
100 V		100
220 V		220
240 V		240
Non-Recognition of DELETE Character		NDE
DTR = ONLINE and NOT BUSY		DNB
RC = - when READY; + when BUSY		IRC
810 printer (VFC)	0994292-0003	VFC
100 V		100
220 V		220
240 V		240
Non-Recognition of DELETE Character		NDE
DTR = ONLINE and NOT BUSY		DNB
RC = - when READY; + when BUSY		IRC
810 printer (FL & Compr PR)	0994293-0001	FCO
100 V		100
220 V		220
240 V		240
Non-Recognition of DELETE Character		NDE
DTR = ONLINE and NOT BUSY		DNB
RC = - when READY; + when BUSY		IRC
810 printer (VFC & Compr PR)	0994293-0002	VCO
100 V		100
220 V		220
240 V		240
Non-Recognition of DELETE Character		NDE
DTR = ONLINE and NOT BUSY		DNB
RC = - when READY; + when BUSY		IRC

Table C-3. Printer Options

Description	Part Number	Designation
Communications Options		
Kit, Parallel I/F (TI)	0994401-0002	PLT
Kit, TTY I/F	0994402-0001	TTY
Kit, Line Buffer Board, EIA I/F	0994511-0001	LBE
Kit, Line Buffer Board, TTY I/F	0994512-0001	LBT
Kit, Line Buffer Board, Parallel I/F	0994513-0001	LBP
Character Set Options (Factory Installed Only)		
Kit, Char Set ENG LTD ASCII	0994395-0001	UKL
Kit, Char Set D—N LTD ASCII w/o VFC	0994395-0002	DNL
Kit, Char Set S—F LTD ASCII w/o VFC	0994395-0003	SWL
Kit, Char Set GERMAN LTD ASCII w/o VFC	0994395-0004	GRL
Kit, Char Set Expanded LTD ASCII w/o VFC	0994395-0008	EXP
Kit, Char Set U.S. Full ASCII w/ or w/o VFC (–1 processor only)	0994395-0010	FUL
Kit, Char Set ENG Full ASCII w/o VFC	0994395-0011	UKF
Kit, Char Set D—N Full ASCII w/o VFC	0994395-0012	DNF
Kit, Char Set S—F Full ASCII w/o VFC	0994395-0013	SWF
Kit, Char Set GERMAN Full ASCII w/o VFC	0994395-0014	GRF
Kit, Char Set KATAKANA w/o VFC	0994395-0015	KAT
Kit, Char Set KATAKANA Special w/o VFC	0994395-0016	KTS
Kit, Char Set US Full ASCII w/o VFC (–2 processor only)	0994395-0019	FUL
Kit Char Set ENG LTD ASCII with VFC	0994395-0101	UKL
Kit, Char Set D—N LTD ASCII with VFC	0994395-0102	DNL
Kit, Char Set S—F LTD ASCII with VFC	0994395-0103	SWL
Kit, Char Set GERMAN LTD ASCII with VFC	0994395-0104	GRL
Kit, Char Set Expanded LTD ASCII wtih VFC	0994395-0108	EXP
Kit, Char Set ENG Full ASCII with VFC	0994395-0111	UKF
Kit, Char Set D—N Full ASCII with VFC	0994395-0112	DNF
Kit, Char Set S—F Full ASCII with VFC	0994395-0113	SWF
Kit, Char Set GERMAN Full ASCII with VFC	0994395-0114	GRF
Kit, Char Set KATAKANA with VFC	0994395-0115	KAT
Kit, Char Set KATAKANA Special with VFC	0994395-0116	KTS
Kit, Char Set US Full ASCII with VFC (–2 processor only)	0994395-0119	FUL
Kit, Char Set SPANISH Full ASCII	0994395-0023	SPF
Kit, Char Set SPANISH Text Edit	0994395-0099	SPT

Table C-3. Printer Options (Concluded)

Description	Part Number	Designation
Communications Options (Field Installed Only)		
Kit, Parallel I/F (TI)	0994401-8002	PLT
Kit, TTY I/F	0994402-8001	TTY
Kit, EIA RS-232-C I/F	0994407-8001	
Kit, Line Buffer Board, EIA I/F	0994511-8001	LBE
Kit Line Buffer Board, TTY I/F	0994512-8001	LBT
Kit Line Buffer Board, Parallel I/F	0994513-8001	LBP
Character Set Options (Field Installed Only)		
Kit, Char Set ENG LTD ASCII w/o VFC	0994395-8001	UKL
Kit, Char Set D–N LTD ASCII w/o VFC	0994395-8002	DNL
Kit, Char Set S–F LTD ASCII w/o VFC	0994395-8003	SWL
Kit, Char Set GERMAN LTD ASCII w/o VFC	0994395-8004	GRL
Kit, Char Set Expanded LTD ASCII w/o VFC	0994395-8008	EXP
Kit Char Set US Full ASCII w/ or w/o VFC (–1 processor only)	0994395-8010	FUL
Kit, Char Set ENG Full ASCII w/o VFC	0994395-8011	UKF
Kit, Char Set D–N Full ASCII w/o VFC	0994395-8012	DNF
Kit, Char Set S–F Full ASCII w/o VFC	0994395-8013	SWF
Kit, Char Set GERMAN Full ASCII w/o VFC	0994395-8014	GRF
Kit, Char Set KATAKANA w/o VFC	0994395-8015	KAT
Kit, Char Set KATAKANA Special w/o VFC	0994395-8016	KTS
Kit, Char Set US Full ASCII w/o VFC (–2 processor only)	0994395-8019	FUL
Kit, Char Set ENG LTD ASCII with VFC	0994395-8101	UKL
Kit, Char Set D–N LTD ASCII with VFC	0994395-8102	DNL
Kit, Char Set S–F LTD ASCII with VFC	0994395-8103	SWL
Kit, Char Set GERMAN LTD ASCII with VFC	0994395-8104	GRL
Kit, Char Set Expanded LTD ASCII with VFC	0994395-8108	EXP
Kit, Char Set ENG Full ASCII with VFC	0994395-8111	UKF
Kit, Char Set D–N Full ASCII with VFC	0994395-8112	DNF
Kit, Char Set S–F Full ASCII with VFC	0994395-8113	SWF
Kit, Char Set GERMAN Full ASCII with VFC	0994395-8114	GRF
Kit, Char Set KATAKANA with VFC	0994395-8115	KAT
Kit, Char Set KATAKANA Special with VFC	0994395-8116	KTS
Kit, Char Set US Full ASCII with VFC (–2 processor only)	0994395-8119	FUL
Kit, Char Set SPANISH ASCII	0994395-8023	SPF
Kit, Char Set SPANISH Text Edit	0994395-8099	SPT
Stand Options		
Stand–w/o Top	0994423-0001	
Basket, Paper–Stand	0994400-0001	
Baud Rate Option		
Kit, Baud Rate Option	0994445-0001	BRO
Baud Rate Option (Field Installed Only)		
Kit, Baud Rate Option	0994445-8001	BRO

Table C-4. Printer Accessories

DESCRIPTION	PART NUMBER
Ribbon, Black Nylon Matrix—40 yard	0996241-0001
Ribbon, Black Nylon Matrix—Pack of 6	0996241-0002
Basket Kit, Paper, Terminal Mounted	0994442-0002
Cord Set, Power—Domestic	0996289-0001
Cord Set, Power—Western Europe	0996290-0001
Cord Set, Power—w/o Connector	0996348-0001
103 Data Set Cable Assy.	0993204-0001
202/212 Data Set Cable Assy.	0993205-0001
Data Terminal Cable Assy.	0993210-0001
Cable Assy., EIA—742	0969626-0001
Cable Assy., EIA Interface	0959372-0001
Cable Assy., 1200 Baud	0959372-0002
Cable Assy., EIA (103A) I/F	0983848-0001
Cable Assy., Extension, EIA	0975056-0010
Cable Assy., Extension, EIA	0975056-0020
Connector, Plug, Electrical	0414127-0001
Cable Assy., EIA Extension	0993211-0001
Extender Board	0994399-0001
Cable Assy., 742 Aux. EIA I/F	0973265-0001
Operators Manual, 810 Printer	0994353-9701
Maintenance Manual, 810 Printer	0994386-9701
Index, Model 810 Printer Shipping Container	0994436-9901
Terminal Stand Kit	0999841-0001
Basket Kit, Paper, Stand Mounted	0999839-0001

Appendix D

TMS 8080A Microprocessor

This appendix contains a reprint of the "TMS 8080A Microprocessor" Data Manual (dated August 1976) for your reference.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TMS 8080A MICROPROCESSOR

1. ARCHITECTURE

1.1 INTRODUCTION

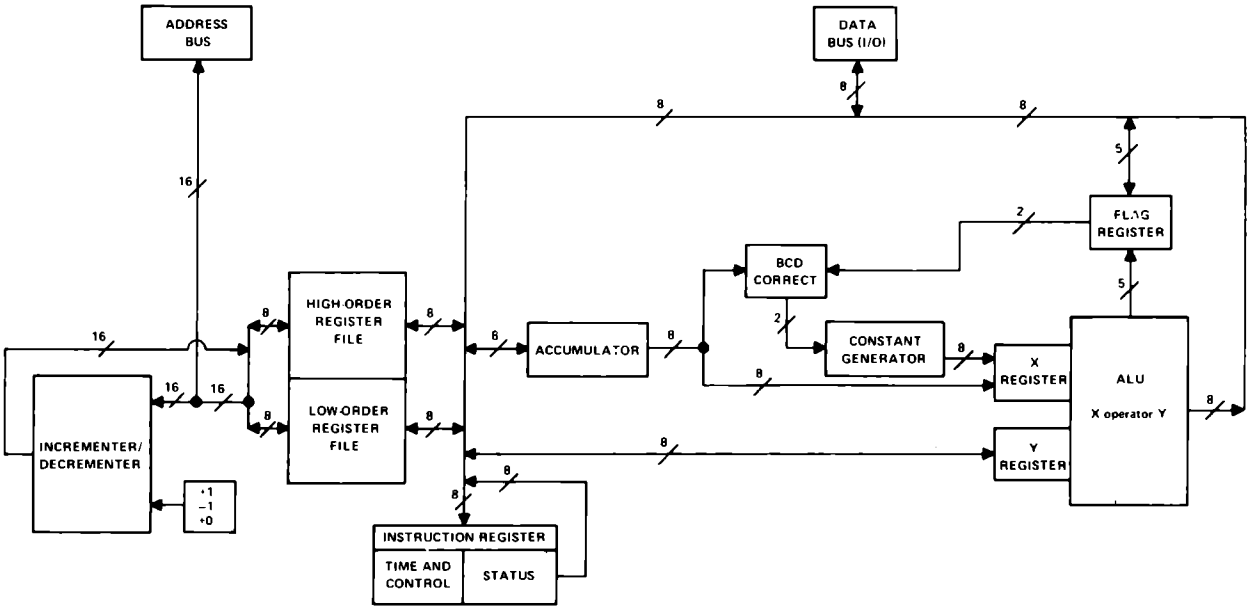
The TMS 8080A is an 8-bit parallel central processing unit (CPU) fabricated on a single chip using a high-speed N-channel silicon-gate process. (See Figure 1). A complete microcomputer system with a 2-μs instruction cycle can be formed by interfacing this circuit with any appropriate memory. Separate 8-bit data and 16-bit address buses simplify the interface and allow direct addressing of 65,536 bytes of memory. Up to 256 input and 256 output ports are also provided with direct addressing. Control signals are brought directly out of the processor and all signals, excluding clocks, are TTL compatible.

1.2 THE STACK

The TMS 8080A incorporates a stack architecture in which a portion of external memory is used as a pushdown stack for storing data from working registers and internal machine status. A 16-bit stack pointer (SP) is provided to facilitate stack location in the memory and to allow almost unlimited interrupt handling capability. The CALL and RST (restart) instructions use the SP to store the program counter (PC) into the stack. The RET (return) instruction uses the SP to acquire the previous PC value. Additional instructions allow data from registers and flags to be saved in the stack.

1.3 REGISTERS

The TMS 8080A has three categories of registers: general registers, program control registers, and internal registers. The general registers and program control registers are listed in Table 1. The internal registers are not accessible by the programmer. They include the instruction register, which holds the present instruction, and several temporary storage registers to hold internal data or latch input and output addresses and data.



994386-100

FIGURE 1–TMS 8080A FUNCTIONAL BLOCK DIAGRAM

1.4 THE ARITHMETIC UNIT

Arithmetic operations are performed in an 8-bit parallel arithmetic unit that has both binary and decimal capabilities. Four testable internal flag bits are provided to facilitate program control, and a fifth flag is used for decimal corrections. Table 2 defines these flags and their operation. Decimal corrections are performed with the DAA instruction. The DAA corrects the result of binary arithmetic operation on BCD data as shown in Table 3.

1.5 STATUS AND CONTROL

Two types of status are provided by the TMS 8080A. Certain status is indicated by dedicated control lines. Additional status is transmitted on the data bus during the beginning of each instruction cycle (machine cycle). Table 4 indicates the pin functions of the TMS 8080A. Table 5 defines the status information that is presented during the beginning of each machine cycle (SYNC time) on the data bus.

1.6 I/O OPERATIONS

Input/output operations (I/O) are performed using the IN and OUT instructions. The second byte of these instructions indicates the device address (256 device addresses). When an IN instruction is executed, the input device address appears in duplicate on A7 through A0 and A15 through A8, along with $\overline{WO}$ and INP status on the data bus. The addressed input device then puts its input data on the data bus for entry into the accumulator. When an OUT instruction is executed, the same operation occurs except that the data bus has OUT status and then has output data.

Direct memory access channels (DMA) can be OR-tied directly with the data and address buses through the use of the HOLD and HLDA (hold acknowledge) controls. When a HOLD request is accepted by the CPU, HLDA goes high, the address and data lines are forced to a high-impedance or "floating" condition, and the CPU stops until the HOLD request is removed.

Interfacing with different speed memories is easily accomplished by use of the WAIT and READY pins. During each machine cycle, the CPU polls the READY input and enters a wait condition until the READY line becomes true. When the WAIT output pin is high, it indicates that the CPU has entered the wait state.

Designing interrupt driven systems is simplified through the use of vectored interrupts. At the end of each instruction, the CPU polls the INT input to determine if an interrupt request is being made. This action does not occur if the CPU is in the HOLD state or if interrupts are disabled. The INTE output indicates if the interrupt logic is enabled (INTE is high). When a request is honored, the INTA status bit becomes high, and an RST instruction may be inserted to force the CPU to jump to one of eight possible locations. Enabling or disabling interrupts is controlled by special instructions (EI or DI). The interrupt input is automatically disabled when an interrupt request is accepted or when a RESET signal is received.

1.7 INSTRUCTION TIMING

The execution time of the instructions varies depending on the operation required and the number of memory references needed. A machine cycle is defined to be a memory referencing operation and is either 3, 4, or 5 state times long. A state time (designated S) is a full cycle of clocks $\phi 1$ and $\phi 2$. (NOTE: The exception to this rule is the DAD instruction, which consists of 1 memory reference in 10 state times). The first machine cycle (designated M1) is either 4 or 5 state times long and is the "instruction fetch" cycle with the program counter appearing on the address bus. The CPU then continues with as many M cycles as necessary to complete the execution of the instruction (up to a maximum of 5). Thus the instruction execution time varies from 4 state times (several including ADDr) to 18 (XTHL). The WAIT or HOLD conditions may affect the execution time since they can be used to control the machine (for example to "single step") and the HALT instruction forces the CPU to stop until an interrupt is received. As the instruction execution is completed (or in the HALT state) the INT pin is polled for an interrupt. In the event of an interrupt, the PC will not be incremented during the next M1 and an RST instruction can be inserted.

TABLE 1
TMS 8080A REGISTERS

NAME	DESIGNATOR	LENGTH	PURPOSE
Accumulator	A	8	Used for arithmetic, logical, and I/O operations
B Register	B	8	General or most significant 8 bits of double register BC
C Register	C	8	General or least significant 8 bits of double register BC
D Register	D	8	General or most significant 8 bits of double register DE
E Register	E	8	General or least significant 8 bits of double register DE
H Register	H	8	General or most significant 8 bits of double register HL
L Register	L	8	General or least significant 8 bits of double register HL
Program Counter	PC	16	Contains address of next byte to be fetched
Stack Pointer	SP	16	Contains address of the last byte of data saved in the memory stack
Flag Register	F	5	Five flags (C, Z, S, P, C1)

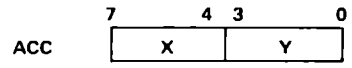
NOTE: Registers B and C may be used together as a single 16-bit register, likewise, D and E, and H and L.

TABLE 2

FLAG DESCRIPTIONS

SYMBOL	TESTABLE	DESCRIPTION
C	YES	C is the carry/borrow out of the MSB (most significant bit) of the ALU (Arithment Logic Unit). A TRUE condition (C = 1) indicates overflow for addition or underflow for subtraction.
Z	YES	A TRUE condition (Z = 1) indicates that the output of the ALU is equal to zero.
S	YES	A TRUE condition (S = 1) indicates that the MSB of the ALU output is equal to a one (1).
P	YES	A TRUE condition (P = 1) indicates that the output of the ALU has even parity (the number of bits equal to one is even).
C1	NO	C1 is the carry out of the fourth bit of the ALU (TRUE condition). C1 is used only for BCD correction with the DAA instruction.

TABLE 3
FUNCTION OF THE DAA INSTRUCTION
Assume the accumulator (A) contains two BCD digits, X and Y



ACCUMULATOR BEFORE DAA				ACCUMULATOR AFTER DAA			
C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$	C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$
0	X < 10	0	Y < 10	0	X	0	Y
0	X < 10	1	Y < 10	0	X	0	Y + 6
0	X < 9	0	Y ≥ 10	0	X + 1	1	Y + 6
1	X < 10	0	Y < 10	1	X + 6	0	Y
1	X < 10	1	Y < 10	1	X + 6	0	Y + 6
1	X < 10	0	Y ≥ 10	1	X + 7	1	Y + 6
0	X ≥ 10	0	Y < 10	1	X + 6	0	Y
0	X ≥ 10	1	Y < 10	1	X + 6	0	Y + 6
0	X ≥ 9	0	Y ≥ 10	1	X + 7	1	Y + 6

NOTE: The corrections shown in Table 3 are sufficient for addition. For subtraction, the programmer must account for the borrow condition that can occur and give erroneous results. The most straight forward method is to set A = 99_{16} and carry = 1. Then add the minuend to A after subtracting the subtrahend from A.

TABLE 4
TMS 8080A PIN DEFINITIONS

SIGNATURE	PIN	I/O	DESCRIPTION
A15 (MSB)	36	OUT	A15 through A0 comprise the address bus. True memory or I/O device addresses appear on this 3-state bus during the first state time of each instruction cycle.
A14	39	OUT	
A13	38	OUT	
A12	37	OUT	
A11	40	OUT	
A10	1	OUT	
A9	35	OUT	
A8	34	OUT	
A7	33	OUT	
A6	32	OUT	
A5	31	OUT	
A4	30	OUT	
A3	29	OUT	
A2	27	OUT	
A1	26	OUT	
A0 (LSB)	25	OUT	
D7 (MSB)	6	IN/OUT	D7 through D0 comprise the bidirectional 3-state data bus. Memory, status, or I/O data is transferred on this bus.
D6	5	IN/OUT	
D5	4	IN/OUT	
D4	3	IN/OUT	
D3	7	IN/OUT	
D2	8	IN/OUT	
D1	9	IN/OUT	
D0 (LSB)	10	IN/OUT	
V_{SS}	2		Ground reference
V_{BB}	11		Supply voltage (−5 V nominal)
V_{CC}	20		Supply voltage (5 V nominal)
V_{DD}	28		Supply voltage (12 V nominal)
$\phi 1$	22	IN	Phase 1 clock.
$\phi 2$	15	IN	Phase 2 clock. See page 19 for $\phi 1$ and $\phi 2$ timing
RESET	12	IN	Reset. When active (high) for a minimum of 3 clock cycles, the RESET input causes the TMS 8080A to be reset. PC is cleared, interrupts are disabled, and after RESET, instruction execution starts at memory location 0. To prevent a lockup condition, a HALT instruction must not be used in location 0.
HOLD	13	IN	Hold signal. When active (high) HOLD causes the TMS 8080A to enter a hold state and float (put the 3-state address and data bus in a high-impedance state). The chip acknowledges entering the hold state with the HLDA signal and will not accept interrupts until it leaves the hold state.
INT	14	IN	Interrupt request. When active (high) INT indicates to the TMS 8080A that an interrupt is being requested. The TMS 8080A polls INT during a HALT or at the end of an instruction. The request will be accepted except when INTE is low or the CPU is in the HOLD condition.
INTE	16	OUT	Interrupts enabled. INTE indicates that an interrupt will be accepted by the TMS 8080A unless it is in the hold state. INTE is set to a high logic level by the EI (Enable Interrupt) instruction and reset to a low logic level by the DI (Disable Interrupt) instruction. INTE is also reset when an interrupt is accepted and by a high on RESET.
DBIN	17	OUT	Data bus in. DBIN indicates whether the data bus is in an input or an output mode. (high = input, low = output).

TABLE 4 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{WR}$	18	OUT	Write. When active (low) $\overline{WR}$ indicates a write operation on the data bus to memory or to an I/O port.
SYNC	19	OUT	Synchronizing control line. When active (high) SYNC indicates the beginning of each machine cycle of the TMS 8080A. Status information is also present on the data bus during SYNC for external latches.
HLDA	21	OUT	Hold acknowledge. When active (high) HLDA indicates that the TMS 8080A is in a hold state.
READY	23	IN	Ready control line. An active (high) level indicates to the TMS 8080A that an external device has completed the transfer of data to or from the data bus. READY is used in conjunction with WAIT for different memory speeds.
WAIT	24	OUT	Wait status. When active (high) WAIT indicates that the TMS 8080A has entered a wait state pending a READY signal from memory.

TABLE 5

TMS 8080A STATUS

SIGNATURE	DATA BUS BIT	DESCRIPTION
INTA	D0	Interrupt acknowledge.
$\overline{WO}$	D1	Indicates that current machine cycle will be a read (input) (high = read) or a write (output) (low = write) operation.
STACK	D2	Indicates that address is stack address from the SP.
HLTA	D3	HALT instruction acknowledge.
OUT	D4	Indicates that the address bus has an output device address and the data bus has output data.
M1	D5	Indicates instruction acquisition for first byte.
INP	D6	Indicates address bus has address of input device.
MEMR	D7	Indicates that data bus will be used for memory read data.

2. TMS 8080A INSTRUCTION SET

2.1 INSTRUCTION FORMATS

TMS 8080A instructions are either one, two, or three bytes long and are stored as binary integers in successive memory locations in the format shown below.

One-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE

Two-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D8 D5 D4 D3 D2 D1 D0	OPERAND

Three-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D6 D5 D4 D3 D2 D1 D0	LOW ADDRESS OR OPERAND 1
D7 D6 D5 D4 D3 D2 D1 D0	HIGH ADDRESS OR OPERAND 2

2.2 INSTRUCTION SET DESCRIPTION

Operations resulting from the execution of TMS 8080A instructions are described in this section. The flags that are affected by each instruction are given after the description.

2.2.1 INSTRUCTION SYMBOLS

SYMBOL	DESCRIPTION	
$<b_2>$	Second byte of instruction	
$<b_3>$	Third byte of instruction	
r_a	Register #	Register Name
	000	B
	001	C
	010	D
	011	E
	100	H
	101	L
	111	A
r_b	Register #	Register Name
	00	BC
	01	DE
	10	HL
	11	SP
r_c	Register #	Register Name
	0	BC
	1	DE
r_d	Register #	Register Name
	00	BC
	01	DE
	10	HL
r_{dL}	Least significant 8 bits of r_d	
r_{dH}	Most significant 8 bits of r_d	
f	Flags	True condition
	Zero (Z)	Result is zero
	Carry (C)	Carry/borrow out of MSB is one
	Parity (P)	Parity of result is even
	Sign (S)	MSB of result is one
	Carry 1 (C1)	Carry out of fourth bit is one
M	Memory address defined by registers H and L	
( )	Contents of specified address or register	
[ ]	Contents at address contained in specified register	
←	Is transferred to	
↔	Exchange	
Am	Bit m of A register (accumulator)	
| |	Flags affected	
b_2	Single byte immediate operand	
b_3b_2	Double byte immediate operand	
$(nnn)_8$	(nnn) is an octal (base 8) number	

2.2.2 ACCUMULATOR GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
ACI	b_2	2	2/7	(A) ← (A) + <b_2>+(carry), add the second byte of the instruction and the contents of the carry flag to register A and place in A. {C,Z,S,P,C1}
ADC	M	1	2/7	(A) ← (A) + (M) + (carry). {C,Z,S,P,C1}
ADC	r_a	1	1/4	(A) ← (A) + (r_a) + (carry). {C,Z,S,P,C1}
ADD	M	1	2/7	(A) ← (A) + (M), add the contents of M to register A and place in A. {C,Z,S,P,C1}
ADD	r_a	1	1/4	(A) ← (A) + (r_a). {C,Z,S,P,C1}
ADI	b_2	2	2/7	(A) ← (A) + <b_2>. {C,Z,S,P,C1}
ANA	M	1	2/7	(A) ← (A) AND (M), take the logical AND of M and register A and place in A. The carry flag will be reset low. {C,Z,S,P,C1}
ANA	r_a	1	1/4	(A) ← (A) AND (r_a). {C,Z,S,P,C1}
ANI	b_2	2	2/7	(A) ← (A) AND <b_2>. {C,Z,S,P,C1}
CMA		1	1/4	(A) ← ($\overline{A}$), complement A.
CMC		1	1/4	(carry) ← ($\overline{carry}$), complement the carry flag. {C}
CMP	M	1	2/7	(A) − (M), compare the contents of M to register A and set the flags accordingly. {C,Z,S,P,C1} (A) = (M) Z = 1 (A) ≠ (M) Z = 0 (A) < (M) C = 1 (A) > (M) C = 0
CMP	r_a	1	1/4	(A) − (r_a). {C,Z,S,P,C1}
CPI	b_2	2	2/7	(A)−<b_2>. {C,Z,S,P,C1}
DAA		1	1/4	(A)←BCD correction of (A). The 8 bit A contents is corrected to form two 4 bit BCD digits after a binary arithmetic operation. A fifth flag C1 indicates the overflow from A_3. The carry flag C indicates the overflow from A_7 (See Table 3). {C,Z,S,P,C1}
DAD	r_b	1	1/10	(HL) ← (HL) + (r_b), add the contents of double register r_b to double register HL and place in HL. {C}
LDA	b_3b_2	3	4/13	(A)←[<b_3> <b_2>]
LDAX	r_c	1	2/7	(A)←[(r_c)]
ORA	M	1	2/7	(A) ← (A) OR (M), take the logical OR of the contents of M and register A and place in A. The carry flag will be reset. {C,Z,S,P,C1}
ORA	r_a	1	1/4	(A) ← (A) OR (r_a). {C,Z,S,P,C1}
ORI	b_2	2	2/7	(A) ← (A) OR <b_2>. {C,Z,S,P,C1}
RAL		1	1/4	A_{m+1}←A_m, A_0←(carry), (carry)←(A_7). Shift the contents of register A to the left one bit through the carry flag. {C}
RAR		1	1/4	A_m←A_m+1, A_7←(carry), (carry)←A_0. {C}
RLC		1	1/4	A_{m+1}←A_m, A_0←A_7 (carry)←(A_7). Shift the contents of register A to the left one bit. Shift A_7 into A and into the carry flag. {C}
RRC		1	1/4	A_m←A_{m+1}, A_7←A_0, (carry)←(A_0). {C}

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
SBB	M	1	2/7	(A)←(A)−(M)−(carry), subtract the contents of M and the contents of the carry flag from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). {C,Z,S,P,C1}
SBB	r_a	1	1/4	(A)←(A)−(r_a)−(carry). {C,Z,S,P,C1}
SBI	b_2	2	2/7	(A)←(A)−<b_2>−(carry). {C,Z,S,P,C1}
STA	b_3b_2	3	4/13	[<b_3> <b_2>]←(A), store contents of A in memory address given in bytes 2 and 3.
STAX	r_c	1	2/7	[(r_c)]←(A), store contents of A in memory address given in BC or DE.
STC		1	1/4	(carry)←1, set carry flag to a 1 (true condition).
SUB	M	1	2/7	(A)←(A)−(M), subtract the contents of M from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). {C,Z,S,P,C1}
SUB	r_a	1	1/4	(A)←(A)−(r_a). {C,Z,S,P,C1}
SUI	b_2	2	2/7	(A)←(A)−<b_2>. {C,Z,S,P,C1}
XRA	M	1	2/7	(A)←(A) XOR (M), take the exclusive OR of the contents of M and register A and place in A. The carry flag will be reset. {C,Z,S,P,C1}
XRA	r_a	1	1/4	(A)←(A) XOR (r_a). {C,Z,S,P,C1}
XRI	b_2	2	2/7	(A)←(A) XOR <b_2>. {C,Z,S,P,C1}

2.2.3 INPUT/OUTPUT INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
IN	b_2	2	3/10	(A)←(input data from data bus), byte 2 is sent on bits A7-A0 and A15-A8 as the input device address. INP status is given on the data bus.
OUT	b_2	2	3/10	(Output data)←(A), byte 2 is sent on bits A7-A0 and A15-A8 as the output device address. OUT status is given on the data bus.

2.2.4 MACHINE INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
HLT		1	2/7	Halt, all machine operations stop. All registers are maintained. Only an interrupt can return the TMS 8080A to the run mode. Note that a HLT should not be placed in location zero, otherwise after the reset pin is active, the TMS 8080A will enter a nonrecoverable state (until power is removed), i.e., in halt with interrupts disabled. This condition also occurs if a HLT is executed while interrupts are disabled. HLTA status is given on the data bus.
NOP		1	1/4	(PC)←(PC)+1, no operation.

2.2.5 PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
CALL	b_3b_2	3	5/17	[(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, transfer PC to the stack address given by SP, decrement SP twice, and jump unconditionally to address given in bytes 2 and 3.
Conditional call instructions for true flags:				
(f)			5/17 (Pass)	If (f) = 1, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PS)←<b_3> <b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, then execute a call. Otherwise, execute the next instruction.
CC (carry)	b_3b_2	3	3/11 (Fail)	
CPE (parity)	b_3b_2	3		
CM (sign)	b_3b_2	3		
CZ (zero)	b_3b_2	3		
Conditional call instructions for false flags:				
(f)			5/17 (Pass)	If (f) = 0, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, otherwise (PC)←(PC)+3.
CNC (carry)	b_3b_2	3	3/11 (Fail)	
CPO (parity)	b_3b_2	3		
CP (sign)	b_3b_2	3		
CNZ (zero)	b_3b_2	3		
DI		1	1/4	Disable interrupts. INTE is driven false to indicate that no interrupts will be accepted.
EI		1	1/4	Enable interrupts. INTE is driven true to indicate that an interrupt will be accepted. Execution of this instruction is delayed to allow the next instruction to be executed before the INT input is polled.
JMP	b_3b_2	3	3/10	(PC)←<b_3> <b_2>, jump unconditionally to address given in bytes 2 and 3.
Conditional jump instructions for true flags:				
(f)			3/10	If (f) = 1, (PC)←<b_3><b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, execute a JMP. Otherwise, execute the next instruction.
JC (carry)	b_3b_2	3		
JPE (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JZ (zero)	b_3b_2	3		
Conditional jump instructions for false flags:				
(f)			3/10	If (f) = 0, (PC)←<b_3> <b_2>, otherwise (PC)←(PC)+3.
JNC (carry)	b_3b_2	3		
JPO (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JNZ (zero)	b_3b_2	3		
PCHL		1	1/5	(PC)←(HL)
POP	PSW	1	3/10	(F)←[(SP)], (A)←[(SP)+1], (SP)←(SP)+2, restore the last stack values addressed by SP into A and F. Increment SP twice.
POP	r_d	1	3/10	(r_{dL})←[(SP)], (r_{dH})←[(SP)+1], (SP)←(SP)+2.
PUSH	PSW	1	3/11	[(SP)−1]←(A), [(SP)−2]←(F), (SP)←(SP)−2, save the contents of A and F into the stack addressed by SP. Decrement SP twice.
PUSH	r_d	1	3/11	(SP)−1]←(r_{dL}), [(SP)−2]←(r_{dH}), (SP)←(SP)−2.
RET		1	3/10	(PC)←[(SP)] [(SP)+1], (SP)←(SP)+2, return to program at memory address given by last values in the stack. The SP is incremented by two.

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
Conditional return instructions for true flags:				
(f)			3/11 (Pass)	If (f) = 1, (PC)←[(SP)] [(SP+1], (SP)←(SP)+2. If the flag specified, f, is 1, execute a RET. Otherwise, execute the next instruction.
RC (carry)	C	1	1/5 (Fail)	
RPE (parity)	P	1		
RM (sign)	S	1		
RZ (zero)	Z	1		
Conditional return instructions for false flags:				
(f)			3/11 (Pass)	If (f) = 0, (PC)←[(SP)] [(SP)+1], (SP)←(SP)+2.
RNC (carry)	C	1	1/5 (Fail)	
RPO (parity)	P	1		
RP (sign)	S	1		
RNZ (zero)	Z	1		
RST		1	3/11	[(SP)−1] [(SP)−2] ←(PC) (SP)←(SP)−2, (PC)←0000R0$_8$ where R is a 3 bit field in RST (RST=3R7$_8$). Transfer PC to the stack address given by SP, decrement SP twice, and jump to the address specified by R.
SPHL		1	1/5	(SP)←(HL).

2.2.6 REGISTER GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
DCR	M	1	3/10	(M)←(M)−1, decrement the contents of memory location specified by H and L. {Z,S,P,C1}
DCR	r_a	1	1/5	(r_a)←(r_a)−1, decrement the contents of register r_a. {Z,S,P,C1}
DCX	r_b	1	1/5	(r_b)←(r_b)−1, decrement double registers BC, DE, HL, or SP.
INR	M	1	3/10	(M)←(M)+1, increment the contents of memory location specified by H and L. {Z,S,P,C1}
INR	r_a	1	1/5	(r_a)←(r_a)+1, increment the contents of register r_a. {Z,S,P,C1}
INX	r_b	1	1/5	(r_b)←(r_b)+1, increment double registers BC, DE, HL, or SP.
LHLD	b_3b_2	3	5/16	(L)←[<b_3> <b_2>]; (H)← [<b_3> <b_2>+1], load registers H and L with contents of the two memory locations specified by bytes 3 and 2.
LXI	$r_bb_3b_2$	3	3/10	(r_{bH})←<b_3>; (r_{bL})←<b_2>, load double registers BC, DE, HL, or SP immediate with bytes 3, 2, respectively.
MVI	M,b_2	2	3/10	(M)←<b_2>, store immediate byte 2 in the address specified by HL
MVI	r_ab_2	2	2/7	(r_a)←<b_2>, load register r_a immediate with byte 2 of the instruction.
MOV	Mr_a	1	2/7	(M)←(r_a), store register r_a in the memory location addressed by H and L.
MOV	r_aM	1	2/7	(r_a)←(M), load register r_a with contents of memory addressed by HL.
MOV	$r_{a1}r_{a2}$	1	1/5	(r_{a1})←(r_{a2}), load register r_{a1} with contents of r_{a2}, r_{a2} contents remain unchanged.
SHLD	b_3b_2	3	5/16	[<b_3> <b_2>]←(L); [<b_3> <b_2>+1)]←(H), store the contents of H and L into two successive memory locations specified by bytes 3 and 2.
XCHG		1	1/4	(H)↔(D); (L)↔(E), exchange double registers HL and DE
XTHL		1	5/18	(L)↔[(SP)], (H)↔[(SP)+1], (SP)=(SP), exchange the top of the stack with register HL.

2.3 INSTRUCTION SET OPCODES ALPHABETICALLY LISTED

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
ACI	2	Add to A, immediate value plus carry†		C	E	7
ADC M	1	Add to A, specified memory value plus carry†		8	E	7
ADC r	1	Add to A, specified register value plus carry†	B	8	8	4
			C	8	9	
			D	8	A	
			E	8	B	
			H	8	C	
			L	8	D	
			A	8	F	
ADD M	1	Add to A, specified memory value†		8	6	7
ADD r	1	Add to A, specified register value†	B	8	0	4
			C	8	1	
			D	8	2	
			E	8	3	
			H	8	4	
			L	8	5	
			A	8	7	
ADI	2	Add to A, immediate value†		C	6	7
ANA M	1	Logical AND with A, specified memory value†		A	6	7
ANAr	1	Logical AND with A, specified register value†	B	A	0	4
			C	A	1	
			D	A	2	
			E	A	3	
			H	A	4	
			L	A	5	
			A	A	7	
ANI	2	Logical AND with A, immediate value†		E	6	7
CALL	3	Unconditional call		C	D	17
CC	3	Call if C flag true		D	C	11/17
CM	3	Call if S flag true		F	C	11/17
CMA	1	Logically invert A		2	F	4
CMC	1	Logically invert C flag‡		3	F	4
CMP M	1	Compare with A, specified memory value†		B	E	7
CMP r	1	Compare with A, specified register value				
			B	B	8	4
			C	B	9	
			D	B	A	
			E	B	B	
			H	B	C	
			L	B	D	
			A	B	F	
CNC	3	Call if C flag false		D	4	11/17
CNZ	3	Call if Z flag false		C	4	11/17
CP	3	Call if S flag false		F	4	11/17
CPE	3	Call if P flag true (even parity)		E	C	11/17
CPI	2	Compare with A, immediate value†		F	E	7
CPO	3	Call if P flag false (odd parity)		E	4	11/17
CZ	3	Call if Z flag true		C	C	11/17
DAA	1	Decimal convert A value†		2	7	4

*Two possible cycle times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES
DAD B	1	16-bit add, BC to HL‡		0	9	10
DAD D	1	16-bit add, DE to HL‡		1	9	10
DAD H	1	16-bit add, HL to HL‡		2	9	10
DAD SP	1	16-bit add, SP to HL‡		3	9	10
DCR M	1	Subtract 1 from specified memory value§		3	5	10
DCR r	1	Subtract 1 from specified register value§	B	0	5	5
			C	0	D	
			D	1	5	
			E	1	D	
			H	2	5	
			L	2	D	
			A	3	D	
DCX B	1	Subtract 1 from double register BC		0	B	5
DCX D	1	Subtract 1 from double register DE		1	B	5
DCX H	1	Subtract 1 from double register HL		2	B	5
DCX SP	1	Subtract 1 from stack pointer		3	B	5
DI	1	Disable interrupt input		F	3	4
EI	1	Enable interrupt input		F	B	4
HLT	1	Halt until interrupted		7	6	7
IN	2	Input data to A		D	B	10
INR M	1	Add 1 to specified memory value§		3	4	10
INR r	1	Add 1 to specified register value§	B	0	4	5
			C	0	C	
			D	1	4	
			E	1	C	
			H	2	4	
			L	2	C	
			A	3	C	
INX B	1	Add 1 to double register BC		0	3	5
INX D	1	Add 1 to double register DE		1	3	5
INX H	1	Add 1 to double register HL		2	3	5
INX SP	1	Add 1 to SP		3	3	5
JC	3	Jump if C flag true		D	A	10
JM	3	Jump if S flag true		F	A	10
JMP	3	Unconditional jump		C	3	10
JNC	3	Jump if C flag false		D	2	10
JNZ	3	Jump if Z flag false		C	2	10
JP	3	Jump if S flag false		F	2	10
JPE	3	Jump if P flag true		E	A	10
JPO	3	Jump if P falg false		E	2	10
JZ	3	Jump if Z flag true		C	A	10
LDA	1	Load A using direct address		3	A	13
LDAX B	1	Load A using indirect address (BC)		0	A	7
LDAX D	1	Load A using indirect address (DE)		1	A	7
LHLD	3	Load HL using direct address		2	A	16
LXI B	3	Load BC with immediate value		0	1	10
LXI D	3	Load DE with immediate value		1	1	10
LXI H	3	Load HL with immediate value		2	1	10
LXI SP	3	Load SP with immediate value		3	1	10

‡Only carry flag affected.
§All flags except carry affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES
MOV M,r	1	Move register value to memory	B	7	0	7
			C	7	1	
			D	7	2	
			E	7	3	
			H	7	4	
			L	7	5	
			A	7	7	
MOV r,M	1	Move memory value to register	B	4	6	7
			C	4	E	
			D	5	6	
			E	5	E	
			H	6	6	
			L	6	E	
			A	7	E	
MOV r_1, r_2	1	Move register value to register	B,B	4	0	5
			B,C	4	1	
			B,D	4	2	
			B,E	4	3	
			B,H	4	4	
			B,L	4	5	
			B,A	4	7	
			C,B	4	8	
			C,C	4	9	
			C,D	4	A	
			C,E	4	B	
			C,H	4	C	
			C,L	4	D	
			C,A	4	F	
			D,B	5	0	
			D,C	5	1	
			D,D	5	2	
			D,E	5	3	
			D,H	5	4	
			H,L	5	5	
			D,A	5	7	
			E,B	5	8	
			E,C	5	9	
			E,D	5	A	
			E,E	5	B	
			E,H	5	C	
			E,L	5	D	
			E,A	5	F	
			H,B	6	0	
			H,C	6	1	
			H,D	6	2	
			H,E	6	3	
			H,H	6	4	
			H,L	6	5	
			H,A	6	7	
			L,B	6	8	

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
MOV r_1, r_2	1	Move register value to register (continued)	L,C	6	9	
			L,D	6	A	
			L,E	6	B	
			L,H	6	C	
			L,L	6	D	
			L,A	6	F	
			A,B	7	8	
			A,C	7	9	
			A,D	7	A	
			A,E	7	B	
			A,H	7	C	
			A,L	7	D	
			A,A	7	F	
MVI M	2	Move immediate value to memory		3	6	10
MVI r	2	Move immediate value to register	B	0	6	7
			C	0	E	
			D	1	6	
			E	1	E	
			H	2	6	
			L	2	E	
			A	3	E	
NOP	1	4-clock-cycle delay	4	0	0	4
ORA M	1	Inclusive OR with A, specified memory value†		B	6	7
ORA r	1	Inclusive OR with A, specified register value†	B	B	0	4
			C	B	1	
			D	B	2	
			E	B	3	
			H	B	4	
			L	B	5	
			A	B	7	
ORI	2	Inclusive OR with A, immediate value†		F	6	7
OUT	2	Output data from accumulator		D	3	10
PCHL	1	Move HL to PC		E	9	5
POP B	1	Load BC from stack		C	1	10
POP D	1	Load DE from stack		D	1	10
POP H	1	Load HL from stack		E	1	10
POP PSW	1	Load AF from stack†		F	1	10
PUSH B	1	Move BC to stack		C	5	11
PUSH D	1	Move DE to stack		D	5	11
PUSH H	2	Move HL to stack		E	5	11
PUSH PSW	1	Move AF to stack		F	5	11
RAL	1	Left rotate A value through C flag‡		1	7	4
RAR	1	Right rotate A value through C flag‡		1	F	4
RC	1	Return if C flag true		D	8	5/11
RET	1	Unconditional return		C	9	10
RLC	1	Left rotate A value‡		0	7	4
RM	1	Return if S flag true		F	8	5/11
RNC	1	Return if C flag false		D	0	5/11
RNZ	1	Return if Z flag false		C	0	5/11
RP	1	Return if S flag false		F	0	5/11

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
RPE	1	Return if P flag true		E	8	5/11
RPO	1	Return if P flag false		E	0	5/11
RRC	1	Right rotate A value ‡		0	F	4
RST	1	1-byte call (restart)				11
			$PC \leftarrow 0000_{16}$	C	7	
			$PC \leftarrow 0008_{16}$	C	F	
			$PC \leftarrow 0010_{16}$	D	7	
			$PC \leftarrow 0018_{16}$	D	F	
			$PC \leftarrow 0020_{16}$	E	7	
			$PC \leftarrow 0028_{16}$	E	F	
			$PC \leftarrow 0030_{16}$	F	7	
			$PC \leftarrow 0038_{16}$	F	F	
RZ	1	Return if Z flag true		C	8	5/11
SBB M	1	Subtract from A, specified memory value plus borrow†		9	E	7
SBB r	1	Subtract from A, specified register value plus borrow†	B	9	8	4
			C	9	9	
			D	9	A	
			E	9	B	
			H	9	C	
			L	9	D	
			A	9	F	
SBI	2	Subtract from A, immediate value plus borrow†		D	E	7
SHLD	3	Store HL value at direct address		2	2	16
SPHL	1	Move HL value to SP		F	9	5
STA	3	Store A value at direct address		3	2	13
STAX B	1	Store A value at indirect address (BC)		0	2	7
STAX D	1	Store A value at indirect address (DE)		1	2	7
STC	1	Set C flag true‡		3	7	4
SUB M	1	Subtract from A, specified memory value†		9	6	7
SUB r	1	Subtract from A, specified register value†	B	9	0	4
			C	9	1	
			D	9	2	
			E	9	3	
			H	9	4	
			L	9	5	
			A	9	7	
SUI	2	Subtract from A, immediate value†		D	6	7
XCHG	1	Exchange contents of HL with DE		E	B	4
XRA M	1	Exclusive OR with A, specified memory value†		A	E	7
XRA r	1	Exclusive OR with A, specified register value†	B	A	8	4
			C	A	9	
			D	A	A	
			E	A	B	
			H	A	C	
			L	A	D	
			A	A	F	
XRI	2	Exclusive OR with A, immediate value†		E	E	7
XTHL	1	Exchange contents of HL with top of stack		E	3	18

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

3. TMS 8080A ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	1.5 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks) (see Note 2)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{IH(\phi)}$	9		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 3)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 3)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current (any input except clocks and data bus)	V_I = 0 V to V_{CC}			±10	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = 0 V to V_{DD}			±10	μA
$I_{I(DB)}$	Input current, data bus	$V_{I(DB)}$ = 0 V to V_{CC}			−100	μA
$I_{I(hold)}$	Address or data bus input current during hold	$V_{I(ad)}$ or $V_{I(DB)}$ = V_{CC}			10	μA
		$V_{I(ad)}$ or $V_{I(DB)}$ = 0 V			−100	
V_{OH}	High-level output voltage	I_{OH} = 150 μA	3.7			V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA			0.45 V	
$I_{BB(av)}$	Average supply current from V_{BB}	Operating at $t_{c(\phi)}$ = 480 ns, T_A = 25°C		−0.01	−1	mA
$I_{CC(av)}$	Average supply current from V_{CC}			60	80	
$I_{DD(av)}$	Average supply current from V_{DD}			50	75	
C_i	Capacitance, any input except clock	V_{CC} = V_{DD} = V_{SS} = 0 V, V_{BB} = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V		10	20	pF
$C_{i(\phi)}$	Clock input capacitance			15	25	
C_o	Output capacitance			10	20	

†All typical values are at T_A = 25°C and nominal voltages.

NOTES: 2. Active pull-up resistors of nominally 2 kΩ will be switched onto the data bus when DBIN is high and the data input voltage is more positive than V_{IH} min.

3. The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

		MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time (see Note 5)	480	2000	ns
$t_{r(\phi)}$	Clock rise time	5	50	ns
$t_{f(\phi)}$	Clock fall time	5	50	ns
$t_{w(\phi1)}$	Pulse width, clock 1 high	60		ns
$t_{w(\phi2)}$	Pulse width, clock 2 high	220		ns
$t_{d(\phi1L-\phi2)}$	Delay time, clock 1 low to clock 2	0		ns
$t_{d(\phi2-\phi1)}$	Delay time, clock 2 to clock 1	70		ns
$t_{d(\phi1H-\phi2)}$	Delay time, clock 1 high to clock 2 (time between leading edges)	80		ns
$t_{su(da-\phi1)}$	Data setup time with respect to clock 1	30		ns
$t_{su(da-\phi2)}$	Data setup time with respect to clock 2	150		ns
$t_{su(hold)}$	Hold input setup time	140		ns
$t_{su(int)}$	Interrupt input setup time	120		ns
$t_{su(rdy)}$	Ready input setup time	120		ns
$t_{h(da)}$	Data hold time (see Note 6)	$t_{PD(DBI)}$		ns
$t_{h(hold)}$	Hold input hold time	0		ns
$t_{h(int)}$	Interrupt input hold time	0		ns
$t_{h(rdy)}$	Ready input hold time	0		ns

NOTES: 5. $t_{c(\phi)} = t_{d(\phi1L-\phi2)} + t_{r(\phi2)} + t_{w(\phi2)} + t_{f(\phi2)} + t_{d(\phi2-\phi1)} + t_{r(\phi1)}$. 480 ns $\leqslant t_{c(\phi)} \leqslant$ 2000 ns.
6. The data input should be enabled using the DBIN status signal. No bus conflict can then occur and the data hold time requirement is thus assured.

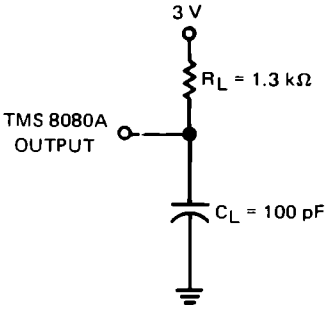
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PD(ad)}$	Propagation delay time, clock 2 to address outputs	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
$t_{PD(da)}$	Propagation delay time, clock 2 to data bus			220	ns
$t_{PD(cont)}$	Propagation delay time, clocks to control outputs			120	ns
$t_{PD(DBI)}$	Propagation delay time, clock 2 to DBIN output		25	140	ns
$t_{PD(int)}$	Propagation delay time, clock 2 to INTE output			200	ns
t_{DI}	Time for data bus to enter input mode			$t_{PD(DBI)}$	ns
t_{PXZ}	Disable time to high-impedance state during hold (address outputs and data bus)			120	ns

The time that the address outputs and output data will remain stable after $\overline{WR}$ goes high, t_{WA} and $t_{WD} \geqslant t_{d(\phi1H-\phi2)}$.
The time between address outputs becoming stable and $\overline{WR}$ going low, $t_{AW} \leqslant 2\,t_{c(\phi)} - t_{d(\phi1H-\phi2)} - t_{r(\phi)} - 120$ ns.
The time between output data becoming stable and $\overline{WR}$ going low, $t_{DW} \geqslant t_{c(\phi)} - t_{d(\phi1H-\phi2)} - t_{r(\phi)} - 150$ ns.
The following are relevant when interfacing to devices requiring V_{IH} min of 3.3 V:

a) Maximum output rise time (t_{TLH}) from 0.8 V to 3.3 V is 140 ns with C_L as specified for the propagation delay times above.

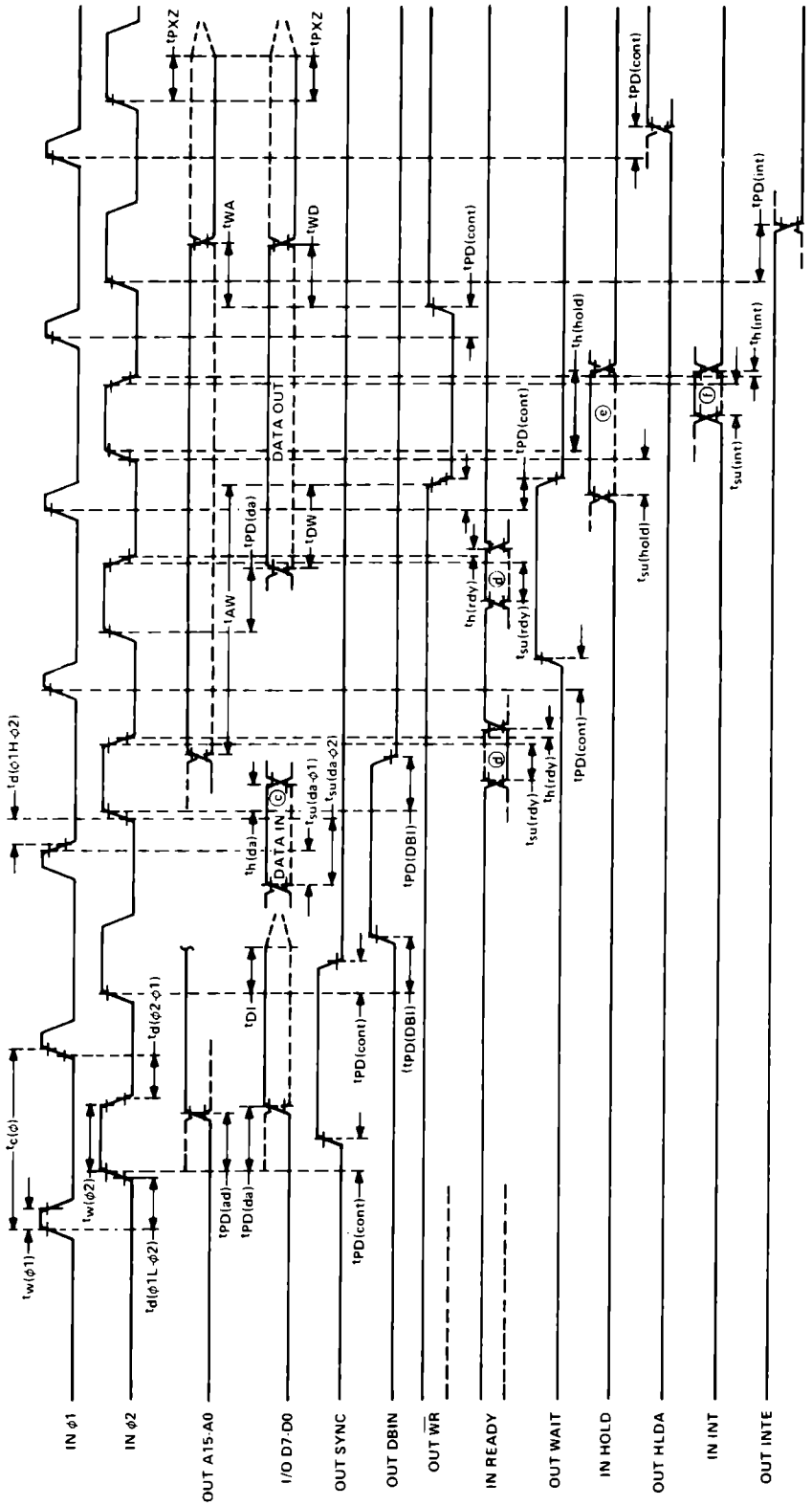
b) Maximum propagation delay times when measured to $V_{ref(H)}$ = 3 V (instead of 2 V) will be 60 ns more than as specified above with C_L as specified.



C_L includes probe and jig capacitance.

LOAD CIRCUIT 994386-147

voltage waveforms (see notes a and b)



NOTES:
a. This timing diagram shows timing relationships only, it does not represent any specific machine cycle.
b. Time measurements are made at the following reference voltages: Clock, $V_{ref(H)} = 9.5$ V, $V_{ref(L)} = 1$ V. Other inputs, $V_{ref(H)} = 2$ V, $V_{ref(L)} = 0.8$ V.
c. Data in must be stable for this period when DBIN is high during S3. Requirements for both $t_{su(da-\phi1)}$ and $t_{su(da-\phi2)}$ must be satisfied.
d. The ready signal must be stable for this period during S2 or SW. This requires external synchronization.
e. The hold signal must be stable for this period during S2 or SW when entering the hold mode and during S3, S4, S5 and SWH when in the hold mode. This requires external synchronization.
f. The interrupt signal must be stable during this period on the last clock cycle of any instruction to be recognized on the following instruction. External synchronization is not required.

FIGURE 2

994386-101

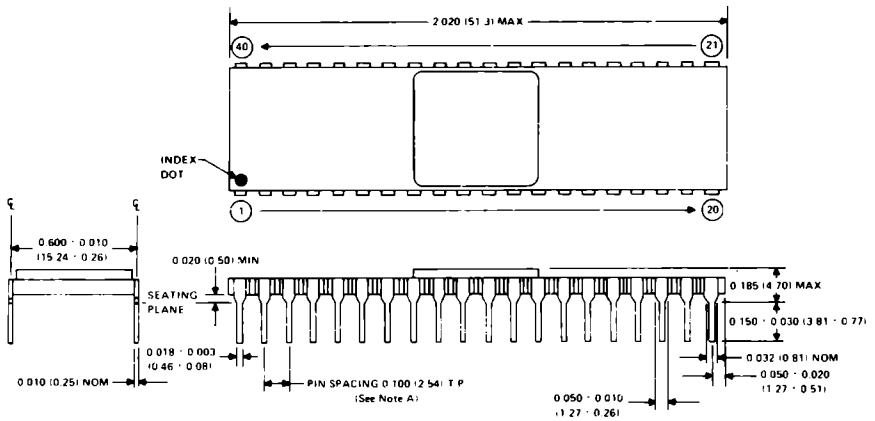
3.6 TERMINAL ASSIGNMENTS

TMS 8080A

A10	1	40	A11
V_{SS}	2	39	A14
D4	3	38	A13
D5	4	37	A12
D6	5	36	A15
D7	6	35	A9
D3	7	34	A8
D2	8	33	A7
D1	9	32	A6
D0	10	31	A5
V_{BB}	11	30	A4
RESET	12	29	A3
HOLD	13	28	V_{DD}
INT	14	27	A2
$\phi 2$	15	26	A1
INTE	16	25	A0
DBIN	17	24	WAIT
$\overline{WR}$	18	23	READY
SYNC	19	22	$\phi 1$
V_{CC}	20	21	HLDA

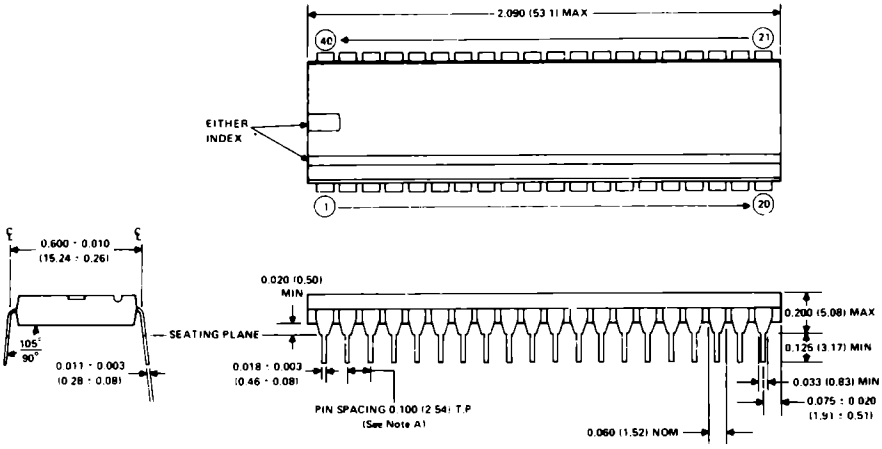
3.7 MECHANICAL DATA

TMS 8080A JL—40-PIN CERAMIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

TMS 8080A NL—40-PIN PLASTIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inch (and parenthetically in millimeters for reference only). Inch dimensions govern.

Appendix E

TMS 5501 I/O Controller

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 5501 is a multifunction input/output circuit for use with TI's TMS 8080A CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080A and has compatible timing, signal levels, and power supply requirements. The TMS 5501 provides a TMS 8080A microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.

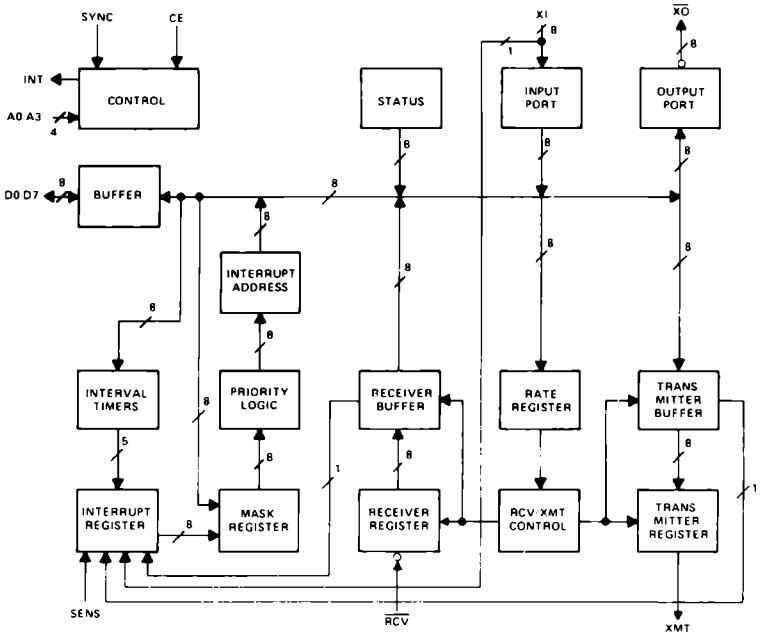


FIGURE 1–TMS 5501 BLOCK DIAGRAM 994386-102

The I/O section of the TMS 5501 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μs to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080A-compatible interrupt logic with masking capability.

Data transfers between the TMS 5501 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080A uses four of its memory-address lines to select one of 14 commands to which the TMS 5501 will respond. These commands allow the CPU to:

- read the receiver buffer
- read the input port
- read the interrupt address
- read TMS 5501 status
- issue discrete commands
- load baud rate register
- load the transmitter buffer
- load the output port
- load the mask register
- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the TMS 5501 command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

1.2 SUMMARY OF OPERATION

Addressing the TMS 5501

A convenient method for addressing the TMS 5501 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5501 address inputs to the four lowest order bits of the bus. This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080A is not required.

Communications Functions

The communications section of the TMS 5501 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate – A CPU command selects a baud rate of 110, 150, 300, 1200, 2400, 4800, or 9600 baud.

Incoming character detection – The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission – The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals – Via the data bus, the TMS 5501 signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

Data Interface

The TMS 5501 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{XO}$ pins of the TMS 5501 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5501 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

Interval Timers

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5501 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

Servicing Interrupts

The TMS 5501 provides a TMS 8080A system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undersired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080A. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, X17, if selected by a discrete command from the TMS 8080A (See Figure 4). The TMS 5501 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080A. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080A only if there is no higher priority interrupt that has not been accepted by the TMS 8080A. The TMS 5501 prioritizes interrupts in the order shown below:

1st – Interval Timer #1
2nd – Interval Timer #2
3rd – External Sensor
4th – Interval Timer #3
5th – Receiver Buffer Loaded
6th – Transmitter Buffer Emptied
7th – Interval Timer #4
8th – Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5501 provides two methods of servicing interrupts; an interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5501 is tied to the INT input of the TMS 8080A. The sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) The TMS 5501 INT output, tied to the TMS 8080A INT input, goes high signaling the TMS 8080A that an interrupt has occured. (3) If the TMS 8080A is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5501 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5501 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080A polls the TMS 5501 to see if an interrupt has occurred by issuing a read-TMS 5501-status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080A will then issue a read-interrupt-address command, which causes the TMS 5501 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080A.

1.3 APPLICATIONS

Communications Terminals

The functions of the TMS 5501 make it particularly useful in TMS 8080A-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

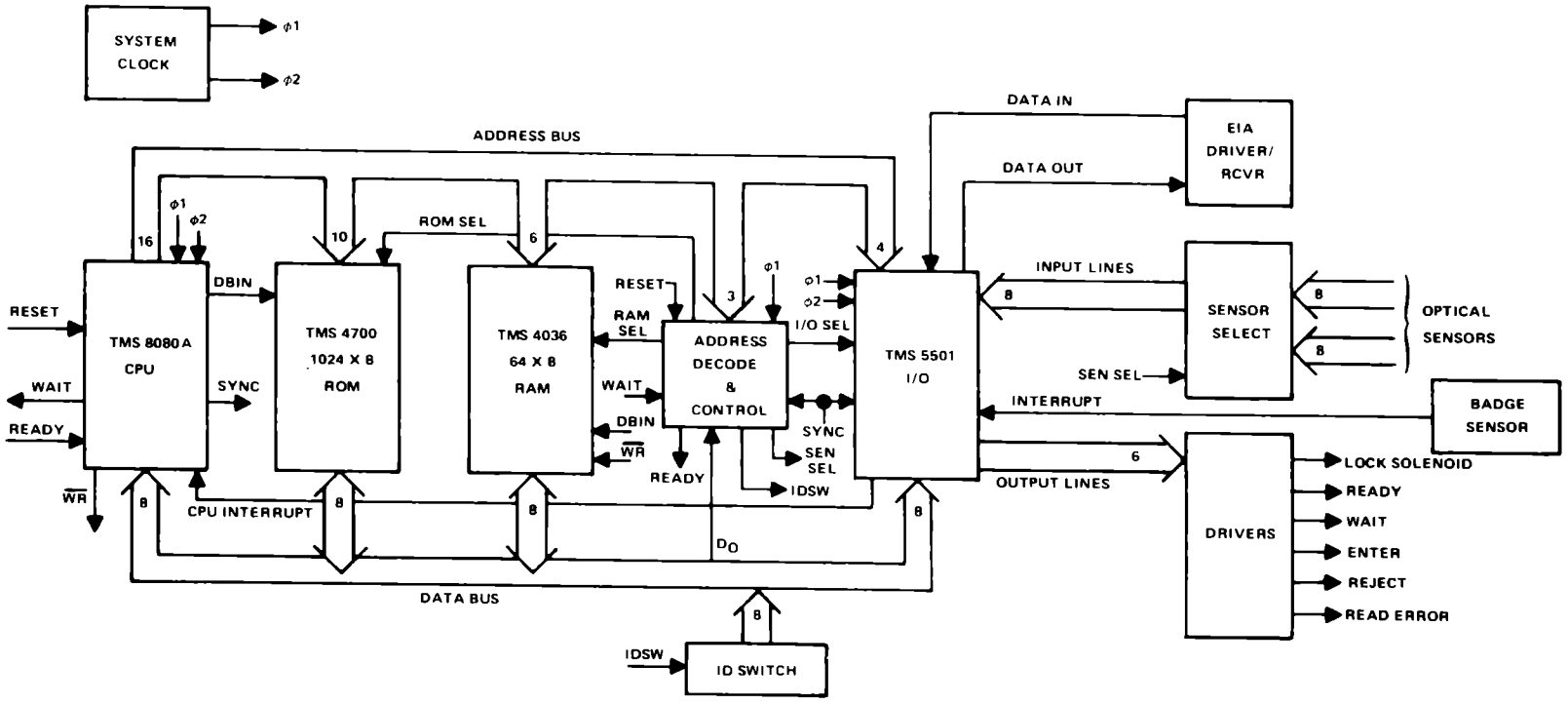


FIGURE 2–ACCESS CONTROL SYSTEM BLOCK DIAGRAM

994386-103

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024 x 8 ROM that contains the system program, and the TMS 4036 is a 64 x 8 RAM that serves as the stack for the TMS 8080A and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5501 onto the data bus at the correct time in the CPU cycle. The clock generator consists of four TTL circuits along with a crystal, needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5501 handles the asynchronous serial communication between the TMS 8080A and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080A to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5501 signals the TMS 8080A when the badge reader or the communication lines need service. The functions that the TMS 5501 is to perform are selected by an address from the TMS 8080A with the highest order address line tied to the TMS 5501 chip enable input and the four lowest order lines tied to the address inputs.

2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5501 consists of:

INTERFACE SIGNALS – a definition of each of the circuit's external connections

COMMANDS – the address required to select each of the TMS 5501 commands and a description of the response to the command.

2.1 INTERFACE SIGNALS

The TMS 5501 communicates with the TMS 8080A via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5501 pin assignments and describes the function of each pin.

TABLE 1
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
CE	18	Chip enable—When CE is low, the TMS 5501 address decoding is inhibited, which prevents execution of any of the TMS 5501 commands.
A3	17	Address bus—A3 through A0 are the lines that are addressed by the TMS 8080A to select a particular TMS 5501 function.
A2	16	
A1	15	
A0	14	
SYNC	19	Synchronizing signal—The SYNC signal is issued by the TMS 8080A and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5501 will monitor the data bus bits DO (interrupt acknowledge) and D1 ($\overline{WO}$, data output function).
$\overline{RCV}$	5	Receiver serial data input line—$\overline{RCV}$ must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry.

TABLE 1 (continued)
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
XI 0	39	External inputs—These eight external inputs are gated to the data bus when the read-external-inputs function is addressed. External input n is gated to data bus bit n without conversion.
XI 1	38	
XI 2	37	
XI 3	36	
XI 4	35	
XI 5	34	
XI 6	33	
XI 7	32	
SENS	22	External interrupt sensing – A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080A.
		OUTPUTS
$\overline{XO}$ 0	24	External outputs—These eight external outputs are driven by the complement of the output register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load-output register command, the external output n will be a low (high). The external outputs change only when a load-output-register function is addressed.
$\overline{XO}$ 1	25	
$\overline{XO}$ 2	26	
$\overline{XO}$ 3	27	
$\overline{XO}$ 4	28	
$\overline{XO}$ 5	29	
$\overline{XO}$ 6	30	
$\overline{XO}$ 7	31	
XMT	40	Transmitter serial data output line—This line remains high when the TMS 5501 is not transmitting.
		DATA BUS INPUT/OUTPUT
D0	13	Data bus—Data transfers between the TMS 5501 and the TMS 8080A are made via the 8-bit bidirectional data bus. D0 is the LSB. D7 is the MSB.
D1	12	
D2	11	
D3	10	
D4	9	
D5	8	
D6	7	
D7	6	
INT	23	Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set.
		POWER AND CLOCKS
V_{SS}	4	Ground reference
V_{BB}	1	Supply voltage (−5 V nominal)
V_{CC}	2	Supply voltage (5 V nominal)
V_{DD}	3	Supply voltage (12 V nominal)
$\phi 1$	20	Phase 1 clock
$\phi 2$	21	Phase 2 clock

2.2 TMS 5501 COMMANDS

The TMS 5501 operates as memory device for the TMS 8080A. Functions are initiated via the TMS 8080A address bus and the TMS 5501 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

TABLE 2
COMMAND ADDRESS DECODING
When Chip Enable Is High

A3	A2	A1	A0	COMMAND	FUNCTION	PARAGRAPH
L	L	L	L	Read receiver buffer	RBn → Dn	2.2.1
L	L	L	H	Read external inputs	XIn → Dn	2.2.2
L	L	H	L	Read interrupt address	RST → Dn	2.2.3
L	L	H	H	Read TMS 5501 status	(Status) → Dn	2.2.4
L	H	L	L	Issue discrete commands	See Figure 4	2.2.5
L	H	L	H	Load rate register	See Figure 4	2.2.6
L	H	H	L	Load transmitter buffer	Dn → TBn	2.2.7
L	H	H	H	Load output port	Dn → $\overline{XO}$n	2.2.8
H	L	L	L	Load mask register	Dn → MRn	2.2.9
H	L	L	H	Load interval timer 1	Dn → Timer 1	2.2.10
H	L	H	L	Load interval timer 2	Dn → Timer 2	2.2.10
H	L	H	H	Load interval timer 3	Dn → Timer 3	2.2.10
H	H	L	L	Load interval timer 4	Dn → Timer 4	2.2.10
H	H	L	H	Load interval timer 5	Dn → Timer 5	2.2.10
H	H	H	L	No function		
H	H	H	H	No function		

RBn ≡ Receiver buffer bit n
Dn ≡ Data bus I/O terminal n
XIn ≡ External input terminal n
RST ≡ 11 (IA_2) (IA_1) (IA_0) 1 1 1 (see Table 3)
TBn ≡ Transmit buffer bit n
$\overline{XO}$n ≡ Output register bit n
MRn ≡ Mask register bit n

TABLE 3
RST INSTRUCTIONS

DATA BUS BIT								INTERRUPT CAUSED BY
0	1	2	3	4	5	6	7	
H	H	H	L	L	L	H	H	Interval Timer 1
H	H	H	H	L	L	H	H	Interval Timer 2
H	H	H	L	H	L	H	H	External Sensor
H	H	H	H	H	L	H	H	Interval Timer 3
H	H	H	L	L	H	H	H	Receiver Buffer
H	H	H	H	L	H	H	H	Transmitter Buffer
H	H	H	L	H	H	H	H	Interval Timer 4
H	H	H	H	H	H	H	H	Interval Timer 5 or X17

The following paragraphs define the functions of the TMS 5501 commands.

2.2.1 Read receiver buffer

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080A and clears the receiver-buffer-loaded flag.

2.2.2 Read external input lines

Addressing the read-external-inputs function transfers the states of the eight external input lines to the TMS 8080A.

2.2.3 Read interrupt address

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5501 status function should be addressed in order to determine whether or not an interrupt condition is pending.

2.2.4 Read TMS 5501 status

Addressing the read-TMS 5501-status function gates the various status conditions of the TMS 5501 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

BIT:	7	6	5	4	3	2	1	0
	START BIT DETECT	FULL BIT DETECT	INTRPT PENDING	XMIT BUFFER EMPTY	RCV BUFFER LOADED	SERIAL RCVD	OVERRUN ERROR	FRAME ERROR

FIGURE 3–DATA BUS ASSIGNMENTS FOR TMS 5501 STATUS 994386-104

Bit 0, framing error

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5501 status will remain high until the next valid character is received.

Bit 1, overrun error

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

Bit 2, serial received data

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

Bit 3, receiver buffer loaded

A high in bit 3 indiciates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

Bit 4, transmitter buffer empty
A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

Bit 5, interrupt pending
A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

Bit 6, full bit detected
A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

Bit 7, start bit detected
A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

2.2.5 Issue discrete commands

Addressing the discrete command function causes the TMS 5501 to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

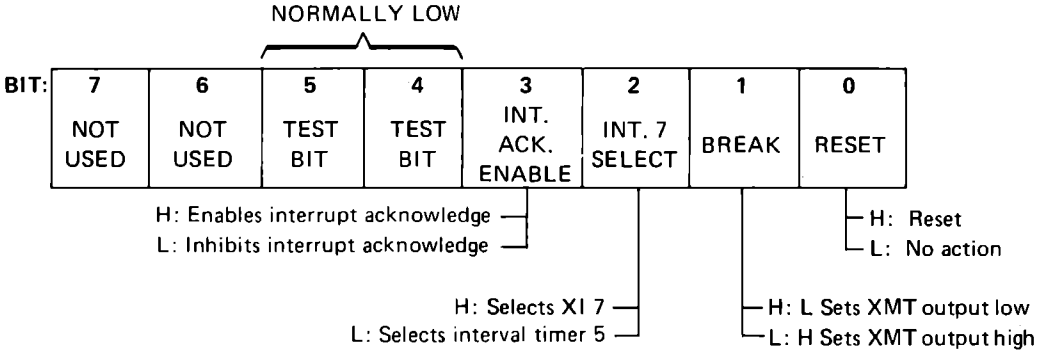


FIGURE 4–DISCRETE COMMAND FORMAT 994386-105

Bit 0, reset
A high in bit 0 will cause the following:

1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-detected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.
2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080A.
3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.
4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

Bit 1, break
A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

Bit 2, interrupt 7 select
Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects the interrupt 7 source to be interval timer 5.

Bit 3, interrupt acknowledge enable
The TMS 5501 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interrupt acknowledge is being issued.

A high in bit 3 enables the TMS 5501 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 5501 to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5501. For correct system operation both bits must be kept low.

Bit 6 and bit 7 are not used and can assume any value.

2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5501 to load the rate register from the data bus and interpret the data bits (See Figure 5) as follows.

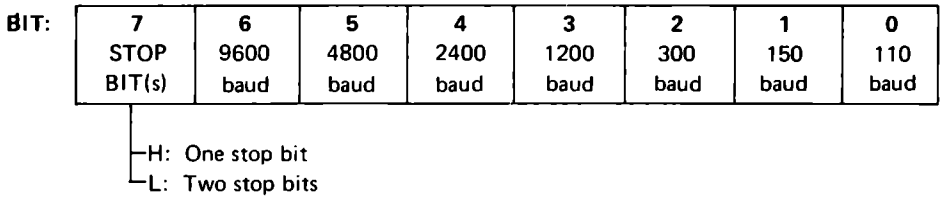


FIGURE 5–DATA BUS ASSIGNMENTS FOR RATE COMMANDS 994386-106

Bits 0 through 6, rate select

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through 6 will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0 110 baud
Bit 1 150 baud
Bit 2 300 baud
Bit 3 1200 baud
Bit 4 2400 baud
Bit 5 4800 baud
Bit 6 9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver and the transmitter circuitry will be inhibited.

Bit 7, stop bits

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO\ 0}$ through $\overline{XO\ 7}$ as the complement of the data bus until new data is loaded.

2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μs (data bus = LLLLLLLH) to 16,320 μs (data bus HHHHHHHH) are counted in 64-μs, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1) . . .	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	. . . . . 1.1 W
Operating free-air temperature range	. . 0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{IH(\phi)}$	9		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 2)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

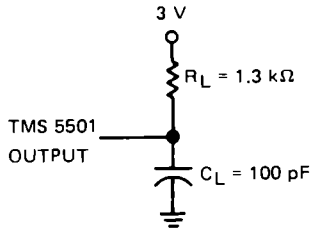
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input current (any input except clocks and data bus)	V_I = 0 V to V_{CC}		±10	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = 0 V to V_{DD}		±10	μA
$I_{I(DB)}$	Input current, data bus	$V_{I(DB)}$ = 0 V to V_{CC}, CE at 0 V		−50	μA
V_{OH}	High-level output voltage	I_{OH} = 400 μA	3.7		V
V_{OL}	Low-level output voltage	I_{OL} = 1.7 mA,		0.45	V
$I_{BB(av)}$	Average supply current from V_{BB}	Operating at $t_{c(\phi)}$ = 480 ns, T_A = 25°C		−1	mA
$I_{CC(av)}$	Average supply current from V_{CC}			100	
$I_{DD(av)}$	Average supply current from V_{DD}			40	
C_i	Capacitance, any input except clock	V_{CC} = V_{DD} = V_{SS} = 0 V, V_{BB} = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V		10	pF
$C_{I(\phi)}$	Clock input capacitance			75	
C_o	Output capacitance			20	

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 5 AND 6)

		MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	480	2000	ns
$t_{r(\phi)}$	Clock rise time	5	50	ns
$t_{f(\phi)}$	Clock fall time	5	50	ns
$t_{w(\phi1)}$	Pulse width, clock 1 high	60		ns
$t_{w(\phi2)}$	Pulse width, clock 2 high	200	300	ns
$t_{d(\phi1L-\phi2)}$	Delay time, clock 1 low to clock 2	0		ns
$t_{d(\phi2-\phi1)}$	Delay time, clock 2 to clock 1	70		ns
$t_{d(\phi1H-\phi2)}$	Delay time, clock 1 high to clock 2 (time between leading edges)	80		ns
$t_{su(ad)}$	Address setup time	50		ns
$t_{su(CE)}$	Chip-enable setup time	50		ns
$t_{su(da)}$	Data setup time	50		ns
$t_{su(sync)}$	Sync setup time	50		ns
$t_{su(XI)}$	External input setup time	50		ns
$t_{h(ad)}$	Address hold time	0		ns
$t_{h(CE)}$	Chip-enable hold time	10		ns
$t_{h(da)}$	Data hold time	10		ns
$t_{h(sync)}$	Sync hold time	10		ns
$t_{h(XI)}$	External input hold time	40		ns
$t_{w(sens\ H)}$	Pulse width, sensor input high	500		ns
$t_{w(sens\ L)}$	Pulse width, sensor input low	500		ns
$t_{d(sens-int)}$	Delay time, sensor to interrupt (time between leading edges)		2000	ns
$t_{d(rst-int)}$	Delay time, RST instruction to interrupt (time between trailing edges)		500	ns

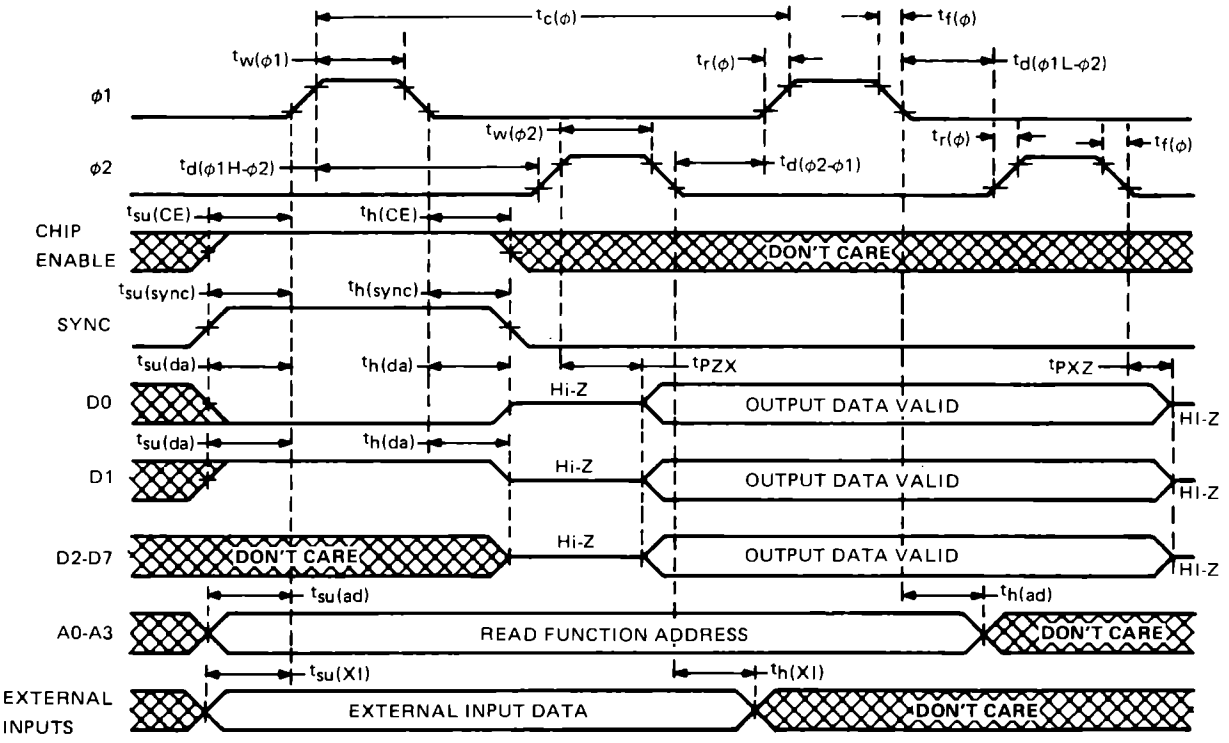
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PZX}	Data bus output enable time	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
t_{PXZ}	Data bus output disable time to high-impedance state			180	ns
t_{PD}	External data output propagation delay time from φ2			200	ns



C_L includes probe and jig capacitance

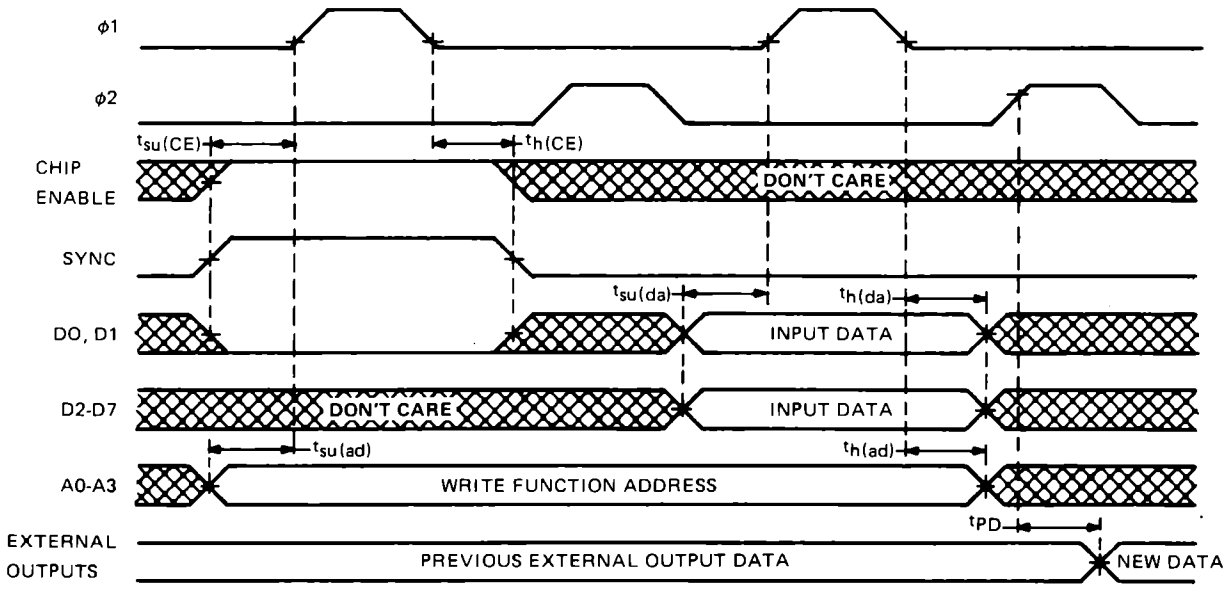
LOAD CIRCUIT



NOTE: For φ1 or φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

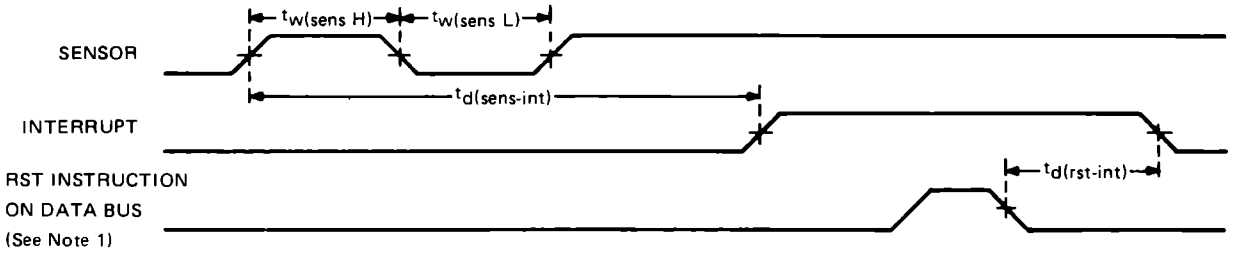
FIGURE 6—READ CYCLE TIMING

994386-107



NOTE: For $\phi 1$ and $\phi 2$ inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 7–WRITE CYCLE TIMING 994386-108

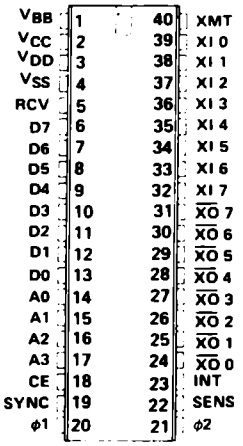


NOTES: 1. The RST instruction occurs during the output data valid time of the read cycle.
2. All timing points are 50% of V_{IH}.

FIGURE 8–SENSOR/INTERRUPT TIMING 994386-109

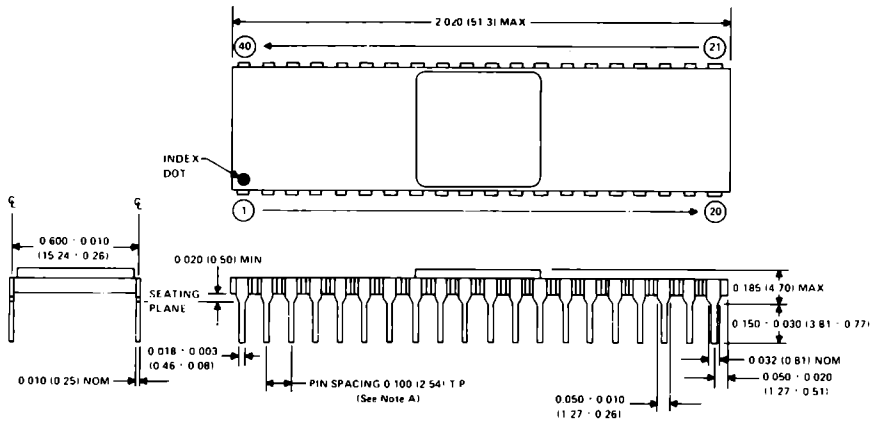
3.6 TERMINAL ASSIGNMENTS

TMS 5501



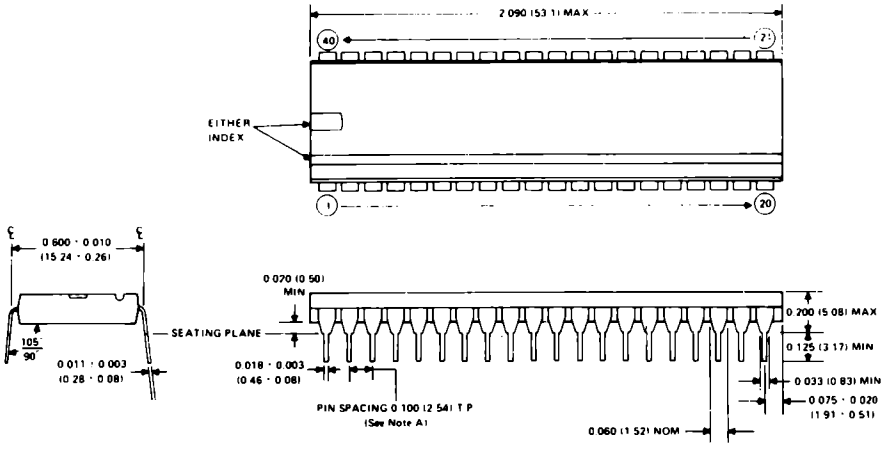
3.7 MECHANICAL DATA

TMS 5501 JL–40-PIN CERAMIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

TMS 5501 NL–40-PIN PLASTIC PACKAGE



NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inch (and parenthetically in millimeters for reference only). Inch dimensions govern.

Appendix F

Installation of Optional Kits

This appendix contains installation instructions on the following kits:

Parallel (TI) Interface Kit

Serial Interface Option Kits

Character Set Option Kit

Baud Rate Option Kit

Line Buffer Option Kit

Terminal Stand Paper Basket Kit

Terminal Paper Basket Kit

TI Publication 994410-9701
Issued 11 April 1977

INSTALLATION INSTRUCTIONS

PARALLEL (TI) INTERFACE KIT

MODEL 810 PRINTER

Kit Part Number	Kit Use
994401-0002	Factory installation kit to allow Model 810 Printer to receive from a parallel data source
994401-8002	Field installation kit to allow Model 810 Printer to receive from a parallel data source

1.0 General

The Parallel (TI compatible) Interface Option Kit consists of necessary cables and hardware to allow the Texas Instruments Model 810 Printer to receive signals from parallel data source.

NOTE

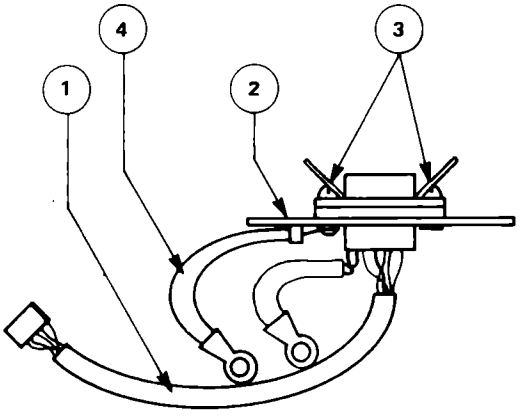
Installation of this kit requires the removal of other optional interfaces (i.e., TTY Interface).

2.0 INSTALLATION

These instructions explain how to install the Parallel Interface Option Kit on the Model 810 Printer (Part Numbers 994292, 994293).

WARNING

Disconnect power cord to prevent possible electrical shock.



1. Parallel Interface
2. Auxiliary Input Panal
3. Screw, and Lock Washers
4. Safety Ground Strap

994386-110

Figure 1. Detail of Parallel Interface Cable with Safety Ground Strap

- Refer to Figure 2 and proceed as follows:

1. Remove printer cover and electronics cover (refer to Operating Instructions for Model 810 Printer, Manual Number 994353-9701).

2. Remove auxiliary input panel from rear of printer as follows:

   a. Unplug existing option interface cable (if present between panel and motherboard) from motherboard.

   b. Slide auxiliary input panel up and out of upper right rear slots in printer base.

3. Install new auxiliary input panel assembled in step 1 as follows:

   a. Slide auxiliary input panel (with parallel interface cable attached) into upper right rear slots in printer base. Panel should be oriented so that the word PARALLEL can be read from outside rear of printer.

   b. Connect loose end of parallel interface cable (Part Number 994359-1) to connector J14 motherboard (note that connector is keyed for proper orientation).

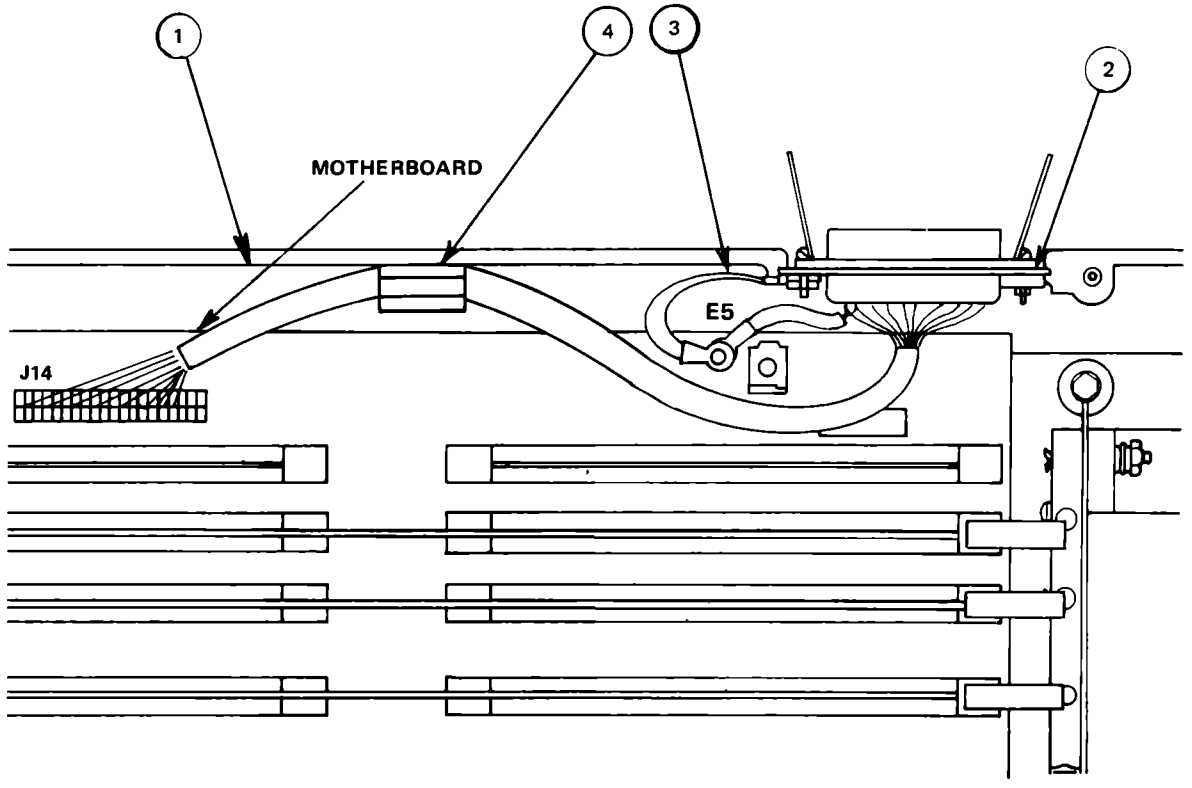
   c. Fasten loose end of safety ground strap (Part Number 960967-3) and ground strap from parallel interface cable to terminal E5 using external tooth lock washer and nut.

3.0 EXTERNAL INSTALLATION

The Model 810 Printer can be connected to parallel interface source using a cable built around the connector plug (Part Number 414127-1) provided with this kit. This connector mates with the connector mounted on the auxiliary input panel. Refer to the Model 810 Printer Operating Instructions (Part Number 994353-9701) for pin out information.

4.0 CONFIGURATION LABEL

If the Model 810 Printer is upgraded using Kit Part Number 994401-8002, the configuration label located on the under side of the printer access door should be replaced with configuration label (Part Number 994351-0001) supplied with this kit. Items on the new label should be check marked the same as items check marked on the old label (except for the interface option). Check the PLT block (√ PLT) only under the interface option.



1. Parallel Interface Cable, Part Number 994359-1
2. Auxiliary Input Panel, Part Number 994333-2
3. Safety Ground Strap, Part Number 960967-3
4. Clip, Part Number 996729-1

994386-111

Figure 2. Parallel Interface Installation on Model 810 Printer.

Installation and Application Instructions
Model 810 RO Printer
Serial Interface Option Kits

(TI Part Numbers 994402-8001, 2230789-8001, 2230790-8001)

1 INTRODUCTION

1.1 General Description

Serial interface options to the Model 810 and other hardware-compatible Texas Instruments printers are:

- TTY 20-mA Current-Loop Option (TI Part No. 994402-0001)
- RS-422 Serial Interface Option (TI Part No. 2230789-0001)
- TTY 20-mA Current-Loop Option (TI Part No. 2230790-0001)

NOTE

DC1/DC3 protocol is available only on Model 810 Printers that are equipped with the LQ upgrade option. TTY 20-mA Current-Loop Option, TI Part No. 994402-0001, does not support DC1/DC3 protocol.

These options provide two-way communication with the user's equipment over a four-conductor cable. This cable can be 300 to 1200 meters (1000 to 4000 feet) long depending on the interface and system configuration. This is in contrast to a maximum length of 15 m (50 ft) for the standard RS-232-C serial interface cable.

1.1.1 Printer Ready/Busy Protocols. The printer receives data and control signals from the user equipment over one conductor pair while transmitting status information to the user equipment on the other pair. The printer reports ready/busy status using either the "break-on-busy" or DC1/DC3 protocol. Protocol is field selectable by the jumper placement on pins of the interface option board. "Ready" indicates the printer is online and ready to receive and print data. "Busy" indicates any one of the following printer conditions: offline, paper out, carriage jammed, or the receive data buffer is full. Break-on-busy protocol is functionally equivalent to the READY/BUSY (reverse channel) signal at pin 11 of the standard EIA* RS-232-C interface. A MARK (low) signal is transmitted while the printer is ready and a SPACE (high) signal is transmitted while the printer is busy.

For inverted reverse channel (IRC), the printer transmits a MARK signal when busy and a SPACE signal when ready.

For DC1/DC3 protocol, the printer transmits a single ASCII† DC1 control character each time it becomes ready and a single DC3 character each time it becomes busy.

1.1.2 Serial Interface Compatibility and Installation. Each of these serial interface options occupies card slot XA3-P1. Any other option, such as the line-buffered (LB) interface or a customer-provided option, must be removed from XA3-P1. Card slot XA3-P2 remains available for other options, such as the half-sized LQ upgrade board, assembly 2232575 (part of the Model 810LQ Printer Kit TI Part No. 2360091-0002). These interface options are physically incompatible with the original full-sized LQ upgrade board TI Part No. 2360095-0001.

1.1.3 Serial Interfaces, Cables, and Connectors. The standard RS-232-C interface remains available when an interface option is installed, but only one interface cable can be connected. The RS-232-C interface is affected differently by each of the TTY interface options (TI Part No. 994402-0001 and TI Part No. 2230790-0001), as described in subsection 1.2. The RS-232-C interface is unaffected by installation of

* Electronics Industries of America

† American Standard Code for Information Interchange

the RS-422 option except for one significant improvement. Unused control inputs, including Data Set Ready, Carrier Detect, and Clear to Send, do not need to be biased ON to receive data. Floating control inputs are sensed as ON so long as the RS-422 interface option is installed.

An auxiliary interface connector/internal cable assembly is supplied with each of these option kits. Any parallel interface (PLT) cable previously installed must be removed in order to install the auxiliary connector.

1.2 TTY Option Kits — TI Part Numbers 994402-8001 and 2230790-8001

Both TTY options provide a full-duplex (four-wire), 20-mA neutral current-loop interface with two signal levels. A MARK is represented by the presence of current flow and a SPACE is represented by the absence of current flow. The TTY transmit data (status) and return pair (TTYXMTD and TTYXMTD/R) and the TTY receive data pair (TTYRCVD and TTYRCVD/R) must be connected to the user equipment to form two independent loops. A series connection of the transmit and receive circuits to form a single two-wire loop results in received data errors due to lack of synchronization of the transmitted status and received data. Additional application information and specifications are given in Appendix A.

Option kit TI Part No. 994402-8001 (Rev.G and earlier) is the original TTY interface designed for the Model 810 Printer and includes the current-loop board, assembly 994305-0001. Because the transmitter circuit performs logical inversion, this interface supports only the break-on-busy protocol; this interface is incompatible with DC1/DC3 protocol of the LQ upgrade option. Both the transmit and receive loops are passive. The printer cannot provide power to either loop. The RS-232-C interface remains available to receive data and transmit status, but ignores all control signal inputs.

Option kit TI Part No. 2230790-8001 includes the second-generation current-loop board, assembly 2230497-0001. Because this assembly eliminates the inversion of transmitted data, it is compatible with both the DC1/DC3 and break-on-busy protocols as well as any data transmission from the printer to the user equipment. This assembly includes several other enhancements:

- Either or both of the current loops (transmit and receive) can be powered from the internal supplies of the printer.
- The RS-232-C interface, including control signal inputs, is fully functional with the new assembly installed, and unused control inputs need not be biased ON in order to receive data.
- Either the normal or the inverted READY/BUSY signal (IRC — inverted reverse channel — suboption) can be *selected* for the RS-232-C interface without affecting the operation of the current loop.

NOTE

Interface cable TI Part No. 2230504-0001 is not compatible with TTY option installation configured for active-mode receive. A recommended cable for use with both the TTY and the RS-232-C interfaces is not provided. Refer to pin-out tables when you build or specify a cable for use with both interfaces.

For service purposes, assembly 2230497-0001, properly configured, can always be substituted for the current-loop board, assembly 994305-0001. However, assembly 994305-0001 can be substituted for assembly 2230497-0001 only if none of the enhanced features of the newer assembly are required in the user application.

Option kit TI Part No. 994402-8001 (Rev. H and later) includes board assembly 2230497-0001 in place of assembly 994305-0001. Effectively, this kit is identical to option kit TI Part No. 2230790-8001. However, the drawing structure does permit the substitution of the kit TI Part No. 2230790-8001 under certain circumstances. Specify TI Part No. 2230790-8001 when ordering kits for applications requiring the enhanced capabilities of board assembly 2230497-0001.

Each of the TTY option kits, now available, consists of the items listed in Table 1.

Table 1. TTY Current-Loop Interface Option Kits — List of Materials

Item	TI Part No.	Description	Quantity
1	2230479-0001	PWB Assy, TTY Interface	1
2	994361-0001	Cable Assy, TTY Interface	1
3	996225-0001	Fastener, Pushnut	2
4	994294-0001	Card Guide, Center	1
5	231792-0004	Color Dot, Yellow	1
6	2210084-0014	SEMS (screw), slotted	2
7	2222694-0001	Lead, Electrical Ground	1
8	960967-0004	Lead, Electrical Ground	1
9	994531-0001	Label, Configuration	1
10	539409-0001	Connector, Plug, 9 Pos.	1
11	539430-0003	Contact, Pin, 24-20 AWG	5
12	2210305-0001	Hood, Strain Relief	1

Current-loop signal pin-outs at the nine-pin auxiliary interface connector, J19, are the same for both option board assemblies, TI Part No. 994305-0001 and TI Part No. 2230497-0001. The pin-out is given in Table 2.

Table 2. Pin-out for TTY Connector J19

Pin	Signal (J19)
1	TTYXMTD
2	TTYXMTD/R
3	Signal ground
4	TTYRCVD/R
5	TTYRCVD

Signal pin-out at the RS-232 connector, J13, depends on which TTY current-loop option board is installed. The pin-outs for both boards are listed in Table 3.

Table 3. Pin-outs for RS-232 Connector J13

Pin *	TI Part No. 994305-0001	TI Part No. 2230497-0001
1	Protective Ground	Protective Ground
2	Transmitted Data	Transmitted Data
3	Received Data	Received Data
4	Request To Send†	Request To Send†
5		Clear To Send
6		Data Set Ready
7	Signal Ground	Signal Ground
8		Carrier Detect
9	+ 12 volt bias	+ 12 volt bias
10	− 12 volt bias	− 12 volt bias
11	Ready/Busy	Ready/Busy
15		TTYRCVD/R
17		TTYRCVD
19		TTYXMTD
20	Data Terminal Ready	Data Terminal Ready
24		TTYXMTD/R

* Pins not listed have no connection.

†For the Model 810, Request To Send is biased OFF when the LQ upgrade option is not installed and ON when it is installed.

1.3 RS-422 Option Kit — TI Part Number 2230789-8001

The RS-422 option provides a transmitted status signal pair and a received data signal pair at RS-422 signal levels. The transmitted status signal pair is designated Send + and Send − ; the received data signal pair is designated Receive + and Receive − . RS-422 follows a negative logic convention to define the significance of a signal in terms of the voltage polarity of one conductor with respect to the second conductor within a pair, as indicated:

Transmit	Receive	MARK	SPACE
Send +	Receive +	Negative	Positive
Send −	Receive −	Positive	Negative

The RS-422 option is compatible with the International Business Machines (IBM) minicomputer and is capable of reliable communication at distances to 1200 m (4000 ft) at data rates up to 9600 baud. Refer to *EIA Standard RS-422* and to Appendix B of these instructions for additional application information.

NOTE

Interface cable TI Part No. 2230504-0001 is not compatible with an RS-422 option installation. A recommended cable for use with both RS-422 and RS-232-C interfaces is not provided. Refer to pin-out tables when you build or specify a cable for use with both interfaces.

The RS-422 option kit consists of the items listed in Table 4.

Table 4. RS-422 Option Kit — List of Materials

Item	TI Part No.	Description	Quantity
1	2230497-0002	PWB Assy, RS-422 Interface	1
2	2230787-0002	Cable Assy, RS-422 (internal)	1
3	996225-0001	Fastener, Pushnut	2
4	994294-0001	Card Guide, Center	1
5	231792-0004	Color Dot, Yellow	1
6	2210084-0014	SEMS (screw), slotted	2
7	2222694-0001	Lead, Electrical Ground	1
8	960967-0004	Lead, Electrical Ground	1
9	994531-0001	Label, Configuration	1

The RS-422 signals are available at both J13, the standard RS-232 connector, and at J19, a 25-pin interface connector supplied with this option. J19 provides IBM Series/1-compatible pin-outs for RS-422 signals only. J13 provides simultaneous availability of RS-422 data signals and RS-232-C control signals for users who do not require IBM pin-for-pin compatibility. Pin assignments for both connectors are listed in Table 5.

Table 5. Pin-outs for RS-232 Connector (J13) and RS-422 Connector (J19)

Pin*	J13	J19
1	Protective Ground	
2	Transmitted Data	
3	Received Data	
4	Request To Send	
5	Clear To Send	
6	Data Set Ready	
7	Signal Ground	Signal Ground
8	Carrier Detect	
9	+ 12 volt bias	
10	− 12 volt bias	
11	Ready/Busy	
15	RS-422 Receive +	RS-422 Receive +
17	RS-422 Receive −	RS-422 Receive −
19	RS-422 Send +	RS-422 Send +
20	Data Terminal Ready	
24	RS-422 Send −	
25		RS-422 Send −

* Pins not listed have no connection.

2 SYSTEM CONSIDERATIONS

2.1 Balanced Versus Unbalanced Circuits

RS-232-C interface signals are inherently unbalanced, or "single-ended." That is, the binary state of a signal is indicated by the polarity of voltage on a single conductor with respect to a reference, that is "signal ground." The fact that return currents for all interface signals flow in both directions sharing a common signal-ground conductor is one potential source of data errors in RS-232-C circuits.

The signal-ground reference is usually connected to earth ground by connecting signal ground to the equipment frame or chassis in at least one unit of data equipment. For safety reasons the equipment frame connects to earth ground by way of the safety ground (green wire ground) in the equipment power cord. Connecting signal and chassis grounds in both units of equipment results in a "ground loop." The interface signal return currents then divide between the signal-ground conductor and the earth. Any shift in ground potential or flow of earth current due to lightning strikes, power-line disturbances, or even leakage currents within the equipment, can cause noise current to flow in the interconnecting cable. This current can cause data errors and even catastrophic equipment failure.

To avoid ground loops, signal and chassis grounds are usually connected in only one unit of equipment (a single-point ground system). The single-point ground cannot eliminate ground loops completely, however, because of capacitive coupling between signal ground and earth at multiple points in the system. Thus, all unbalanced interface signals, such as RS-232-C, are relatively susceptible to noise. This restricts their use to low-data-rate communications over short distances.

RS-422 circuits are balanced, or "differential". That is, the binary state of a signal is indicated by the polarity of one conductor with respect to a second paired conductor that provides a dedicated return path for the interface signal current. While the voltage of each of the conductors typically is referenced to earth ground, any electrical disturbance theoretically induces the same voltage with respect to earth on both conductors. The net effect at the receiver input terminals is zero. Such a circuit is referred to as "perfectly balanced." However, perfectly balanced circuits rarely exist except in theory.

In the case of the RS-422 circuits, differing paths to earth from each of the signal conductors exist due to stray capacitances, leakage resistance, and the power-line connections through the driver and receiver circuits. These differing paths partially unbalance the circuit and allow some of the voltages induced with respect to earth (common-mode noise) and ground potential shifts between transmitter and receiver to be converted to voltage differences between the conductors (differential-mode noise). This noise can cause

data errors and possible circuit failure if the breakdown voltage of a circuit is exceeded.

Even with these limitations, balanced RS-422 circuits are capable of communication at higher frequencies and over longer distances than unbalanced circuits. This option provides reliable communication at 9600 baud over distances of 1200 m (4000 ft).

The TTY current-loop circuits are also balanced in the sense that a dedicated return-current conductor is provided for each signal. Unlike RS-422, the binary state of a signal is indicated by the presence or absence, rather than the direction, of current flow. Due to the magnitude of the currents that must be switched, the communication range of this option is restricted by the circuit design. The maximum achievable range also is highly dependent upon the system configuration, as described in Appendix A. The TTY current-loop option does offer the possible advantage of optical isolation between the printer and the user equipment, minimizing the effects of ground potential shifts.

2.2 Cabling and Grounding

A twisted pair, No. 24 AWG or larger, is required for each interface signal and signal return. A cable shield or a shield around each pair should be used to minimize noise susceptibility as well as radiation from the cable. Shielded telephone cable is adequate for most applications. However, lower capacitance cable, with individually shielded conductor pairs, is recommended for maximum performance of the TTY current-loop option. The shield or shields should be terminated at only one end, preferably at the user's equipment. If the shield must be terminated at the printer, bond the shield to a conductive backshell on the cable connector so that the connector-retaining hardware connects the shield to the printer chassis.

Careful attention should be given to cable routing to avoid noise interference, particularly with long cables. Route cables as far as possible from ac-power wiring, radio transmitting antenna feeders, and similar noise sources. Also avoid parallel routing of cables. The use of grounded, metallic cable trays or conduit is highly recommended. In extreme noise environments, a double-shielded cable may be required. The inner shield or shields should be terminated in the same manner as single-shielded cables. The outer shield, which must be insulated from the inner shield, should be bonded to earth ground at both ends of the cable, as close as practicable to the equipment, but not in contact with the chassis of either the printer or the user equipment. The outer shield should also be grounded at as many intermediate points as possible.

Outdoor cables connecting two or more buildings require special installation procedures. The cable installation must act to prevent data errors and possible equipment damage. More importantly, the installation must guard against the hazards of personnel injury or death resulting from electrical shock or fire due to lightning strikes. Outdoor cables require a comprehensive system of shielding, bonding, and grounding. Protective devices at the cable entrances to each building must be installed. Unless you are experienced in this field, you should obtain the assistance of a registered professional engineer to supervise the design and construction of the installation. You can also consider an alternate means of communication, such as a fiber-optic link, which is less susceptible to lightning damage.

The preferred system-grounding arrangement is the connection of the signal ground to the chassis or frame ground (protective ground) in both the user equipment and the printer. This method provides satisfactory operation for TTY current loops if there is total optical isolation of the interface signals between the printer and the user equipment.

The preferred system grounding is also satisfactory for operation of the RS-422 option if the two earth ground points are at a potential difference of less than 4 volts. Data errors can indicate that this condition is not satisfied. If this is the case, disconnect signal ground from chassis ground in the printer only (ISC — isolated signal and chassis ground — suboption for the Model 810 Printer) and connect signal ground of the printer to signal ground of the user equipment. This alternative requires an additional conductor in the cable. Do not attempt to use a cable shield for the signal ground connection.

3 INSTALLATION PROCEDURES

3.1 Preparation

Before installing a serial interface, check the operation of the printer. If a data source with an RS-232-C interface is available, connect it to the printer and print several pages of data. If a data source is not available, print several pages of the self-test pattern. Follow the directions in the printer operating instructions.

CAUTION

Prevent possible component damage caused by electrostatic discharge. Before handling the printer, interface cables, and electronic assemblies, discharge static electricity from hands, tools, and containers by touching them to a grounded surface. In low-humidity conditions, use of a high-impedance, grounded-conductive floor mat or wrist strap is recommended. Remember that the printer probably is not grounded after the power cord is disconnected.

WARNING

Set the power ON/OFF switch to OFF and disconnect the power cord before beginning installation to prevent possible electrical shock.

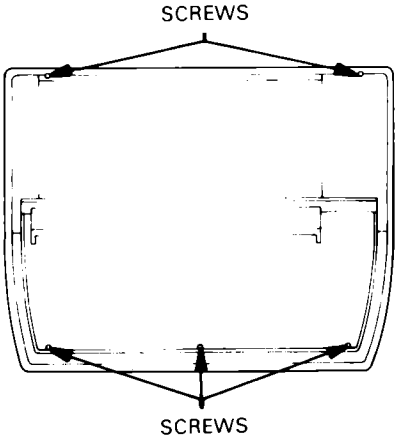
Disconnect all signal cables before disconnecting the power cord. Always reconnect the power cord before connecting signal cables.

3.2 Serial Interface Option Installation

Steps for installing a serial interface option are as follows:

1. Remove the five screws that secure the printer cover. Three screws are located under the access cover, as shown in Figure 1. Two screws are located at the left- and right-rear corners of the printer. Lift off the printer cover.

OVERHEAD VIEW



2360090-1

Figure 1. Locations of Printer Cover Screws

2. Loosen or remove, as required, the three screws shown in Figure 2 that retain the electronics cover. Lift the electronics cover up and off.

3. Remove any printed wiring board installed in the board slot for connector XA3P1, shown in Figure 3.

4. Remove the Model 810 processor board, assembly 994244, from the board slot for connectors XA2P1 and XA2P2.

5. Remove the resistor pack from motherboard socket XU1. Store the resistor pack for reinstallation should the interface option be removed at a later time.

6. If a center card guide already is installed between connectors XA3P1 and XA3P2, proceed to step 7. If not, install the guide supplied with the option kit as follows:

   a. Remove the pushnut fasteners (if installed) from each of the two short posts that protrude through the motherboard between XA3P1 and XA3P2.

   b. Position the card guide on the motherboard so that the short posts protrude through holes in the bottom mounting

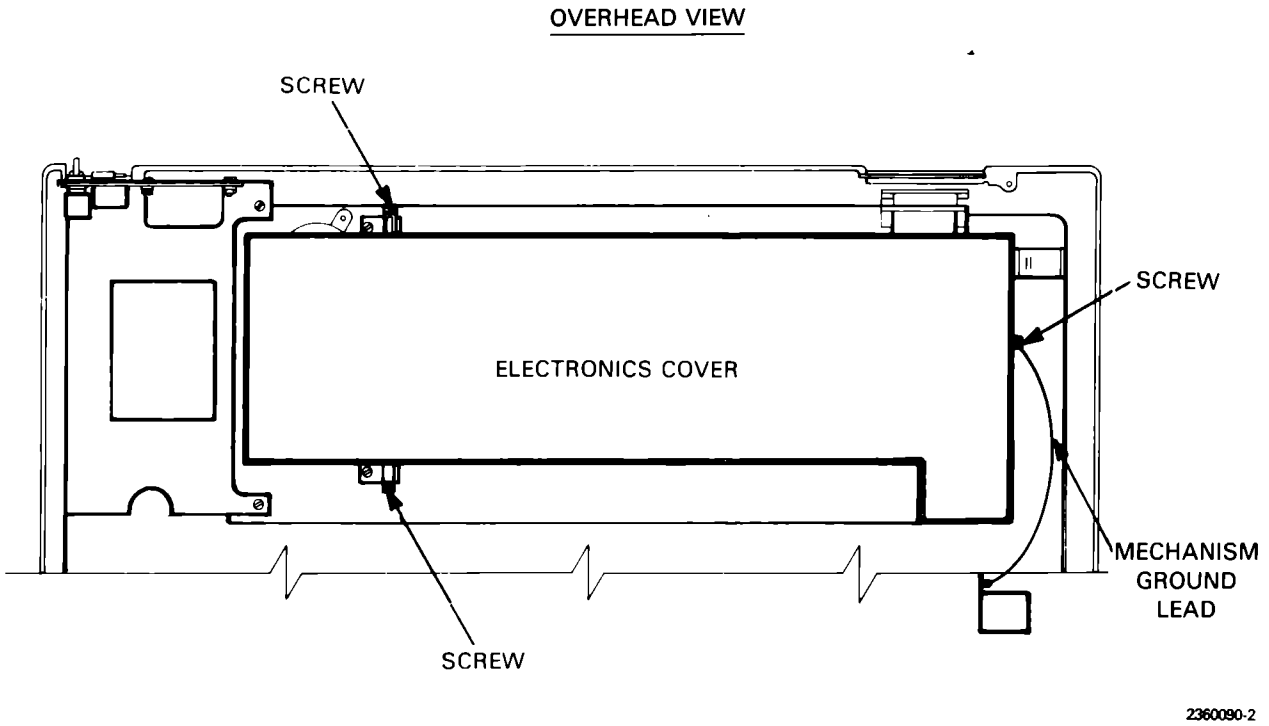


Figure 2. Locations of Electronics Cover Screws

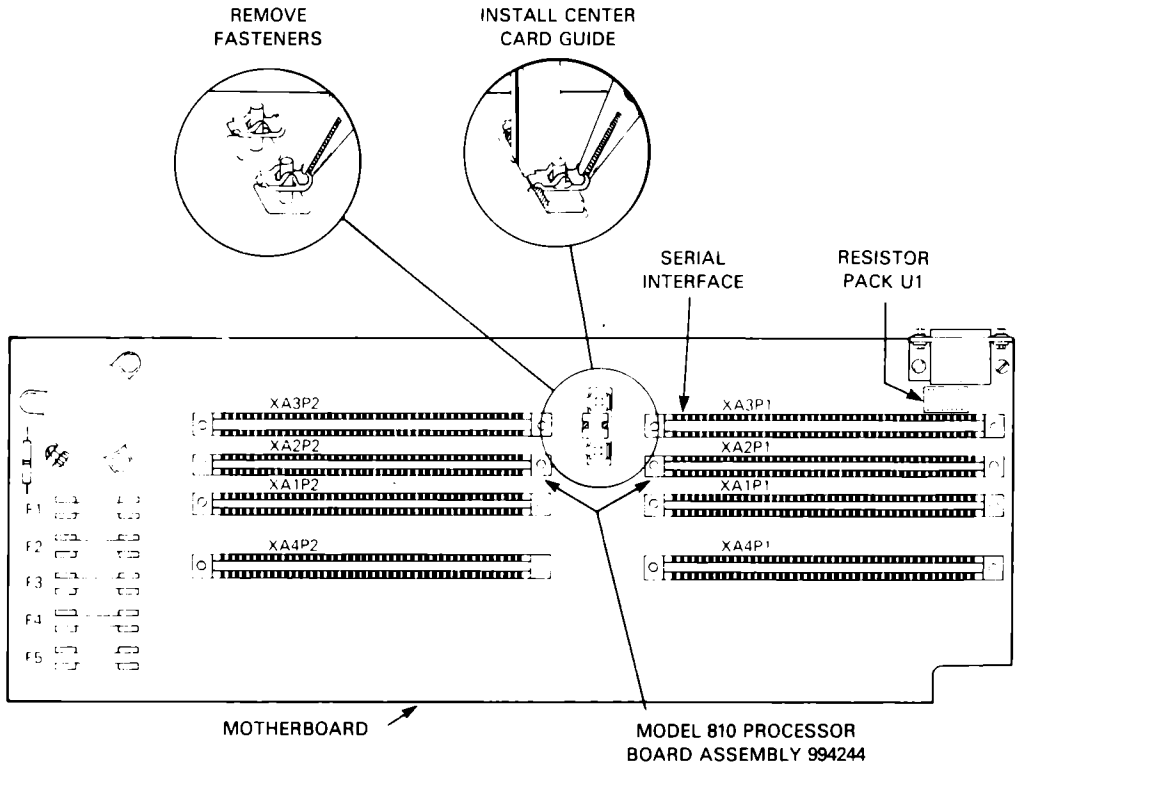


Figure 3. Printer Component Locations

surface of the guide. Note that the guide is not symmetrical; position the guide so that its vertical surfaces are centered between the connectors.

c. Lock the card guide in place by placing a pushnut fastener (TI Part No. 996255-0001) on each post and then push the fasteners down firmly.

7. Remove the auxiliary input panel located on the rear of the printer above the RS-232 connector, as shown in Figure 4.

a. If an existing option interface cable is present between the panel and the motherboard, unplug the cable from the motherboard.

b. Slide the auxiliary panel up and out of the slots in the printer base.

8. Install the new auxiliary panel and cable assembly as follows:

a. Slide the panel down into the slots on the printer base.

b. Connect the cable to the group of pins marked J15 on the motherboard. Figure 4 shows the proper orientation of the cable connector.

c. Connect the green safety ground wire, attached to the auxiliary panel, to the RS-232 connector, as shown in Figure 5.

9. Verify that the printer grounding option matches the desired system configuration as follows:

a. If earth ground is to be used as the common signal reference, verify that a jumper is installed between motherboard terminals E6 and E7. These terminals are located left of the card guide between XA1 and XA2. Early versions of the motherboard have a jumper wire installed in this location.

b. If a single-point grounding system is desired, remove the E6 to E7 jumper. If single-point grounding is used, a signal ground connection to user equipment must be made in the interface cable.

10. Configure the serial interface option board, shown in Figure 6, for the desired system configuration as follows:

NOTE

Not applicable to the first-generation TTY current-loop board, assembly 994305-0001.

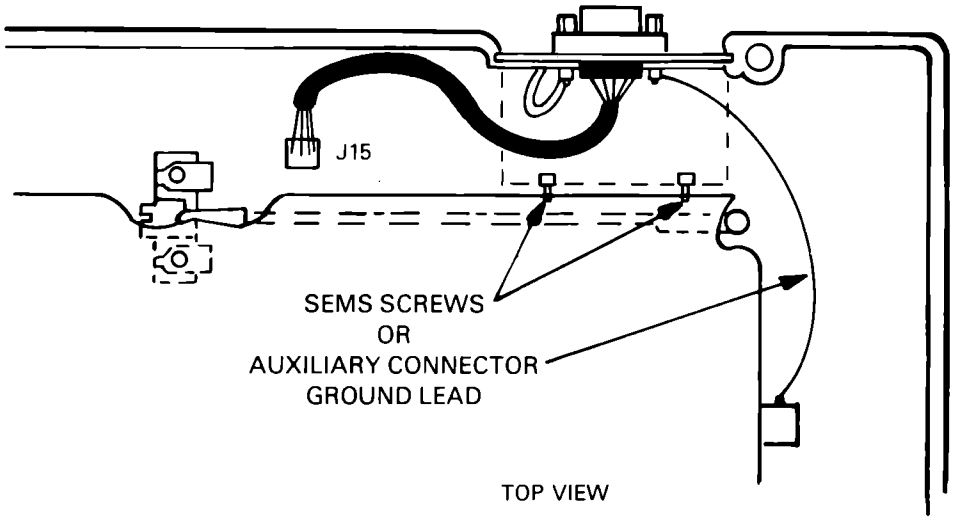


Figure 4. Serial Interface Cable Connection to Connector J15

a. Remove the option board from the antistatic bag and place it component side up on the bag.

b. Verify that the four LOOPBACK/NORMAL jumpers are in the NORMAL position (closest to the edge connector tabs). E20 – E21, E23 – E24, E26 – E27, and E29 – E30 are jumpered.

c. If the RS-232-C Transmit Data signal is desired at the option board transmit outputs (as when using the DC1/DC3 protocol capability of the Model 810LQ Printer), jumper E4 – E5.

d. When the Ready/Busy signal is desired at the transmit outputs, examine the Model 810 processor board and note the position of the IRC suboption jumper on terminals E7, E8, and E9. If Normal Reverse Channel is selected on the Model 810 processor board (E8 – E9 jumpered), jumper E5 to E6 on the option board. If Inverted Reverse Channel is selected on the Model 810 processor board (E7 – E8 jumpered), jumper E5 to E35 on the option board.

NOTE

E8 must be jumpered to E9 on the Model 810 processor board when installing the option board, assembly 994305-0001.

The jumper arrangements described provide a continuous MARK signal at the Receive Data input of the user equipment when the printer is ready to receive data. A continuous SPACE signal is provided when the printer is offline, out of paper, jammed, or the receive data buffer is full.

e. For the TTY current-loop option *only*, verify that jumpers are installed on E8 – E9, E11 – E12, E14 – E15, and E17 – E18. These are the standard shipping configurations and provide for passive-mode operation (loop current supplied by user equipment) of both the transmit and receive loops. If active-mode operation (loop current supplied by the printer) is desired, change the jumper positions as follows:

- Transmit loop: E7 – E8, E10 – E11
- Receive loop: E13 – E14, E16 – E17

CAUTION

Read Appendix A before selecting active-mode operation for either loop.

11. Replace the Model 810 processor board in the board slot for connectors XA2P1 and XA2P2.

12. Install the interface option board in the board slot for connector XA3P1. Position the board so that the yellow dot on the card guide is adjacent to the yellow ejector.

3.3 Installing the Nine-Pin Connector

No interface cable or connector is supplied with the RS-422 option, because the user frequently has an existing cable with the required industry-standard 25-pin connector. However, a nine-pin connector kit is provided with the TTY current-loop options for installation on the user-supplied cable.

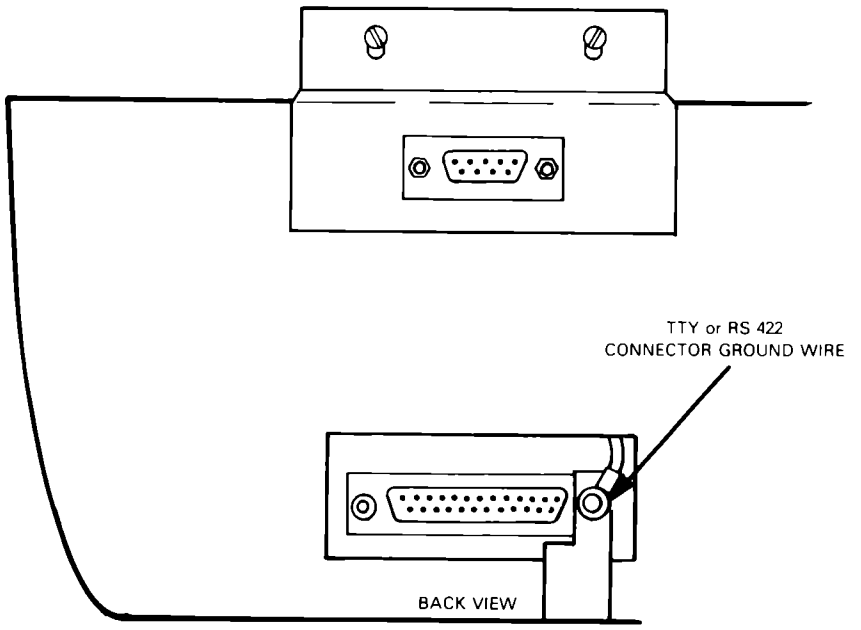
To assemble the connector kit, see Figure 7 and follow these steps:

1. Crimp contacts onto the wires of the user cable.

2. Insert the contacts into the correct locations in the connector housing (1).

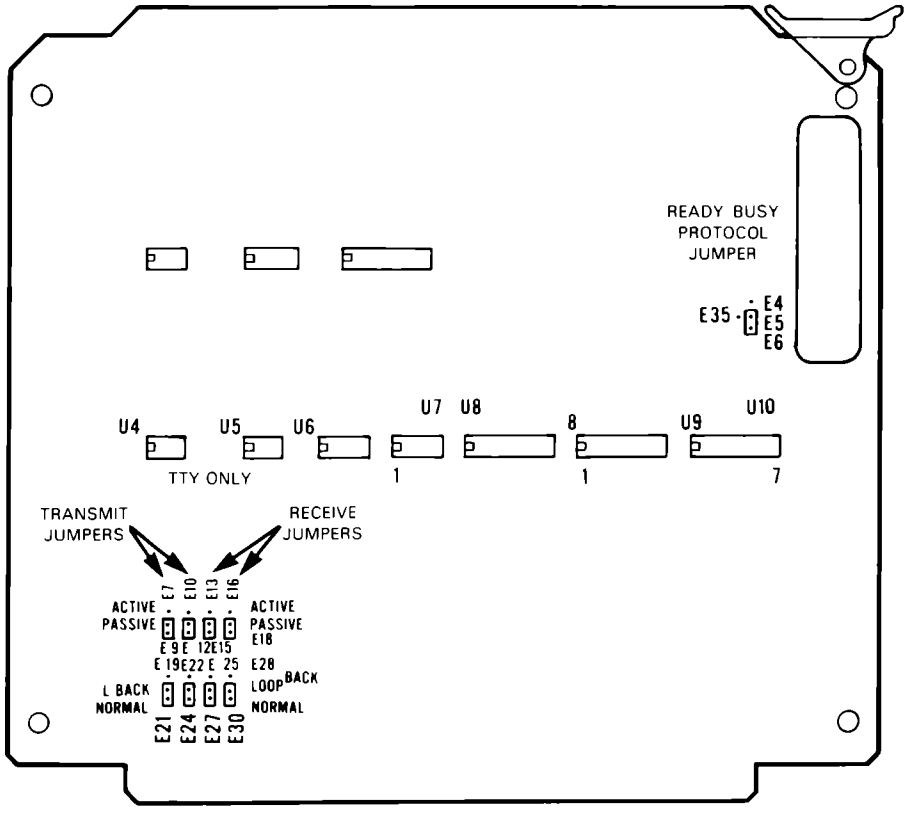
3. Install the connector in the hood (2). Note pin 1 orientation.

4. Install the retainer (3) in the hood.



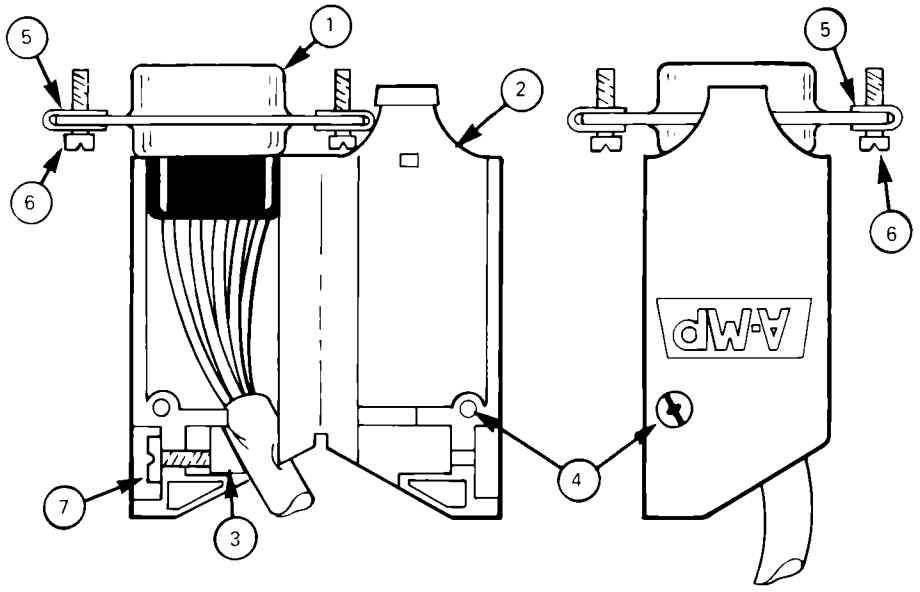
2230792-3

Figure 5. Ground Wire Connected to the RS-232 Connector



2230792-4

Figure 6. Serial Interface Option Board — Jumper Locations



Legend:

1. Connector housing
2. Hood
3. Retainer
4. Screw (hood)
5. Retainer clips
6. Screws (connector)
7. Screw (cable retainer)

2230792-5

Figure 7. Nine-Pin Connector Kit

5. Install the screw (4) in the hood.

6. Install the retainer clips (5) and screws (6) in the connector. Be sure that the threaded side of the clip is next to the screw head.

7. Install the cable retainer screw (7) in the connector.

3.4 Initial Checkout

Steps for initial checkout of the serial interface option are as follows:

WARNING

Do not allow anyone other than experienced technical personnel to operate the printer with the covers removed. Do not leave the printer unattended unless all covers are secured in place or the power cord and all signal cables are disconnected. Failure to follow these precautions may result in a serious fire or electrical shock hazard.

1. Connect the power cord and set the power **ON/OFF** switch to **ON.** Verify that the printer completes its power-up cycle normally. All controls and indicators should function as they did before the option was installed. Print several lines of the internal self-test pattern. If the printer does not function normally, set the power **ON/OFF** switch to **OFF,** remove the interface option board, and repeat this procedure. If operation is correct with the option board removed, the board is defective and must be replaced.

2. If the preliminary test results are satisfactory with the option installed, set the power **ON/OFF** switch to **OFF** and connect the interface cable to the user equipment. Only one interface cable at a time should be connected. If an RS-232-C data source was used for testing before

modification, remove the screw and green cable used to ground the TTY or RS-422 connector and reconnect the RS-232-C data source. Repeat the original test procedure. If nothing prints, the interface option board is probably defective. Verify this by repeating the test with the option board removed and the resistor pack reinstalled. If problems are encountered with the RS-232-C interface, follow the troubleshooting procedures listed in the printer maintenance manual to correct them. If data is printed but with numerous data errors or missing blocks of data, a system problem exists probably caused by changes made to the system grounding or ready/busy signaling during the installation. Ignore these problems for the moment and proceed to step 3.

3. Disconnect the RS-232 cable, if installed. Connect the option interface cable between the printer and the user equipment. Transmit data to the printer. If printer operation is satisfactory, proceed directly to subsection 3.5. If the option interface does not operate satisfactorily, troubleshoot as follows:

   a. If nothing prints, first verify that the printer port on the user equipment is functional. Do this by successfully transmitting data from user equipment to another printer or a CRT terminal. Use the same interface cable if possible. If the port is functional, verify that the interface cable connections are compatible with the printer. In the case of the RS-422 option, be sure that the interface cable is connected to the proper receptacle on the printer. J13 and J19 are identical physically, but are wired differently.

      Reread the interface documentation available for the user equipment. If all else fails, a break-out box and dual-trace oscilloscope are required to locate the signals in the interface connector. If the interface connections are correct and communication is still not successful, a ready/busy protocol incompatibility may exist. If this fails, try a different option board that is properly configured.

   b. If completely garbled data is printed, ensure that the user equipment and the printer are set to the same baud rate. For an RS-422 interface, reverse the polarity of printer Receive + and Receive – at the interface connector.

   c. If printed data is recognizable but the data error rate is unacceptable, try changing the system-grounding method. If the earth ground reference method is used, check the integrity and noise level of the earth ground connections at both the printer and the user equipment. If this fails, reexamine the design and construction of the interface cable.

If none of these steps results in satisfactory operation, a conference between the installer, the user's technical personnel, and the manufacturer of the user equipment should resolve the problem.

3.5 Installation Completion

After satisfactory operation with the user equipment has been accomplished, complete the installation as follows:

1. Set the power **ON/OFF** switch to **OFF**, disconnect the interface cable, and disconnect the power cord.

2. Replace the electronics cover. Do not tighten the mounting screws at this time. Reconnect the mechanism ground wire by installing the ring lug on the cover mounting screw above the fan before inserting the screw. If your printer is not equipped with a ground lead from the mechanism to the card cage cover, install the ground lead, TI Part No. 960967-0004, supplied in the kit. Temporarily remove the upper spacer mounting screw from the right side-plate of the mechanism, adjacent to the paper motor. Slide one ring lug of the ground lead over the screw; replace the screw and tighten it firmly. Place the other ring lug over the right-end electronics cover mounting screw, insert the screw through the cover

and into its mounting hole in the fan bracket, and tighten the screw finger-tight.

3. Fasten the auxiliary interface connector panel to the electronics cover using the two SEMS screws supplied with the option kit. If the electronics cover is without screw mounting holes, install the other ground lead, TI Part No. 2222694-0001, supplied in the kit. Attach the ground lead ring lug to the auxiliary connector panel using the connector mounting hardware. Slide the spade lug under the electronics cover mounting screw. Do not rely on interference fit of the bracket to the cover for chassis ground connection of the auxiliary connector panel; the panel must be grounded by one of the methods described to minimize radiated interference and susceptibility to electrostatic discharge.

4. Tighten the three electronics cover mounting screws.

5. Replace the printer cover and tighten the five mounting screws.

6. Compare the blank configuration label supplied with the option kit to the label inside the printer access door. Write the corresponding codes on the new label so that it reflects the new configuration of the printer. Do not mark the code for any option removed. Checkmark ISC if chassis and signal grounds have been disconnected; otherwise, leave this space blank. Checkmark IRC if the inverted reverse channel suboption is installed on the Model 810 processor board; otherwise, leave this space blank. Checkmark TTY for the current-loop option or write RS-422 in the "Other" location of the label, as appropriate. After you have filled in this information, remove the protective backing from the new label. Place the new label on over the old label and press on.

7. Reconnect the power cord and interface cable and perform a final check of printer operation in the user system.

Serial Interface Instructions

Appendix A

Current-Loop Interface

A.1 SPECIFICATIONS

Physical and environmental specifications of the printer are not affected by the TTY current-loop options.

CAUTION

Operation outside of specification limits can cause data errors and possible shortened life or catastrophic failure of circuit components.

The electrical specifications of the options are listed as follows:

Transmitter

- Maximum differential-mode voltage: 50-V dc
- Maximum loop current: 100-mA dc (passive mode), 40-mA dc (active mode)
- Maximum voltage drop for MARK: 1.5-V dc at 20 mA
- Maximum leakage current for SPACE: 0.5 mA at 50-V dc
- Maximum common-mode voltage: 50-V dc, continuous or switched at configured transmission rate

Receiver

- Maximum loop-current capability: 100-mA dc (passive mode), 40-mA dc (active mode)
- Minimum loop current required for MARK detection: 16.0-mA dc
- Maximum loop current permitted for SPACE detection: 5.0-mA dc
- Maximum voltage drop: 3.0-V dc at 20 mA
- Maximum common-mode voltage: 50-V dc, continuous or switched at configured transmission rate

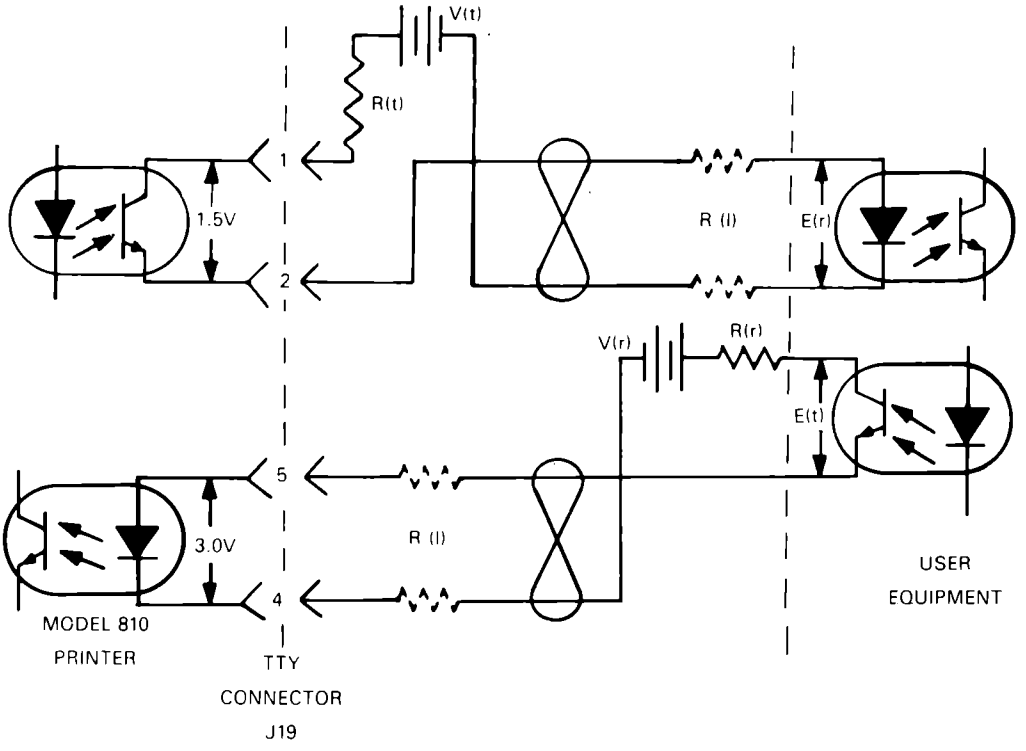
A.2 SYSTEM CONFIGURATIONS

A.2.1 Externally Powered Loops

The ideal system configuration is shown in Figure A-1. The transmit and receive loops are each powered from a separate, floating supply. Note that the supply for each loop is physically located adjacent to the loop transmitter, minimizing current transients, cable cross-talk, and distortion associated with charging and discharging the cable capacitance. This configuration is capable of providing reliable communication at 9600 baud at distances of 900 m (3000 ft) or more using two twisted pairs of No. 22 or No. 24 AWG wire for the loop cable.

The following guidelines apply to the system configuration of Figure A-1:

1. The loop supplies may be either current-regulated 20-mA supplies specifically designed for current-loop applications or constant voltage supplies in series with current-limiting resistors as shown. Choose the lowest voltage supply that provides adequate loop current by considering the voltage drops across the transmitter, the receiver, and the loop-cable resistance. A 10-V dc to 15-V dc supply is usually ideal. Do not exceed the maximum voltage specifications of either the printer or the user equipment. Use caution when selecting or using constant current supplies. Many of these devices



2230792-6

Figure A-1. Externally Powered Current Loops

are designed for very-long-distance communication applications and, as a result, their open-circuit voltage greatly exceeds the specifications of the printer.

2. If constant voltage supplies are used, select the series resistors to set the loop currents as closely as possible to 20 mA, which can be computed using equations *a* and *b* as follows:

$$a.\quad 0.020 = \frac{V(t) - 1.5 - E(r)}{R(t) + R(l)}$$

where:

V(t) = transmitter supply voltage
R(t) = transmitter series resistor
E(r) = voltage drop across the user's receiver
R(l) = transmit loop resistance (cable resistance)

$$b.\quad 0.020 = \frac{V(r) - 3.0 - E(t)}{R(r) + R(l)}$$

where:

V(r) = receiver source voltage
R(r) = receiver series resistor
E(t) = voltage drop across the user's transmitter
R(l) = receive loop resistance (cable resistance)

A.2.2 Separate Internally Powered Loops

Few users go to the added expense of providing two separate loop supplies as in Figure A-1. The same results, with certain restrictions, can be achieved with the configuration of Figure A-2. The transmit loop is powered by the printer (active-mode transmitter) and the receive loop is powered by the user equipment (printer passive-mode receiver configuration).

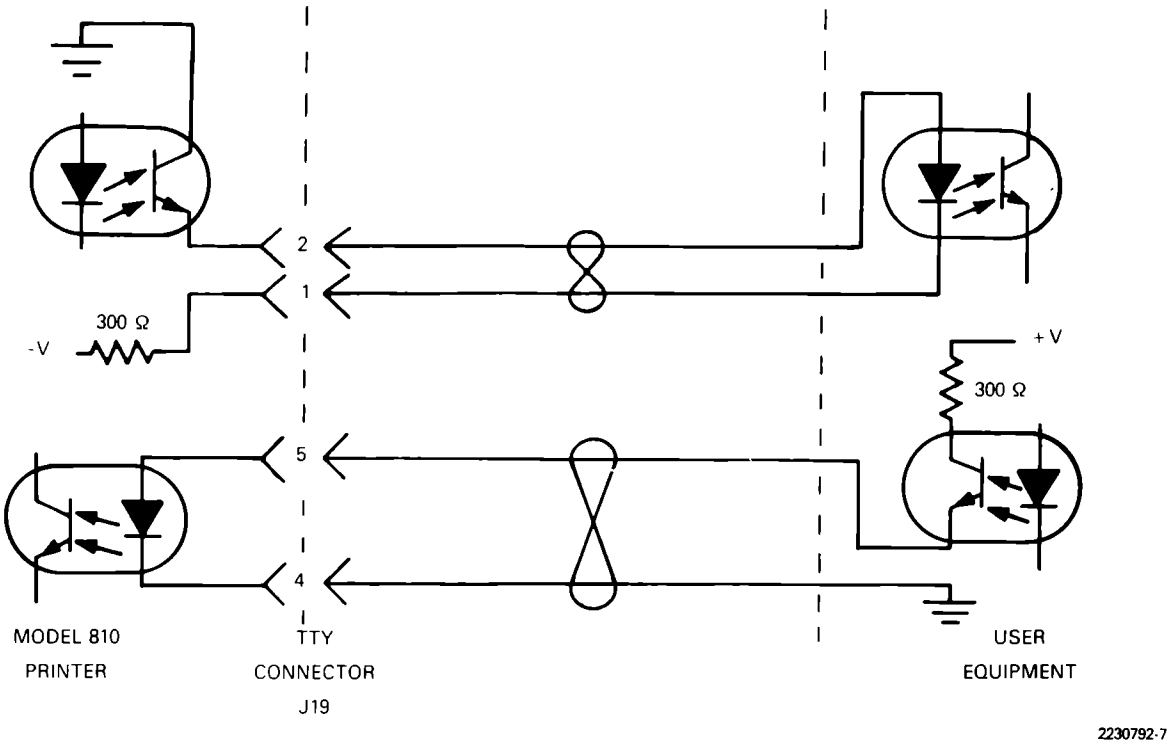


Figure A-2. Current Loops Powered by Printer and User Equipment

The following restrictions apply to the configuration of Figure A-2:

1. The user equipment receiver must provide electrical isolation from the transmit loop. The printer receiver must be connected in the passive mode. Failure to satisfy either condition creates a ground loop that can cause data errors and possible equipment damage.

2. Any cable shield, if used, can be connected to chassis ground at one end of the cable only. Connecting the frames of the printer and the user equipment by means of the signal cable can create a ground loop and violate safety codes.

3. Because the interface cable is now connected directly to the power supplies of both the printer and the user equipment, the likelihood of equipment damage due to signal-line transients and the need for signal-line protection are greatly increased. Do not use the printer with either the transmitter or receiver connected in the active mode when communicating over outdoor cables.

4. Note the changes in loop terminations in the printer and user equipment when the printer transmitter is connected in the active mode.

A.2.3 Combined Internally Powered Loops

In the more commonly used configurations, both loops are powered either by the user equipment (Figure A-3), by the printer (Figure A-4), or by a single external supply located at one end of the cable. These configurations are usually capable of reliable communications up to 300 m (1000 ft). Depending on the cable design and the characteristics of the user equipment, communication at longer distances is possible, particularly at lower baud rates. The major problem with these configurations is that the transmitter located at the far end of the cable, away from the loop supply, must discharge the cable capacitance each time it closes. This results in increased signal distortion

by causing high-peak currents in the transmitter and induced noise pulses in the other loop.

The following recommendations should be followed if both loops are powered by either the user equipment or the printer:

1. Keep the loop supply voltage as low as possible to minimize switching transients.

2. For best performance, power the loops from the user equipment and use "break-on-busy" protocol. This is the usual system configuration when using the TTY current-loop option, board assembly 994305-0001, which has no provisions for powering the loops from the printer.

3. Observe all appropriate precautions and recommendations listed previously when communicating over outdoor cables. In particular, do not configure the printer for active mode.

4. Note the changes in loop terminations in the printer and user equipment when the printer is connected for active-mode and passive-mode operation.

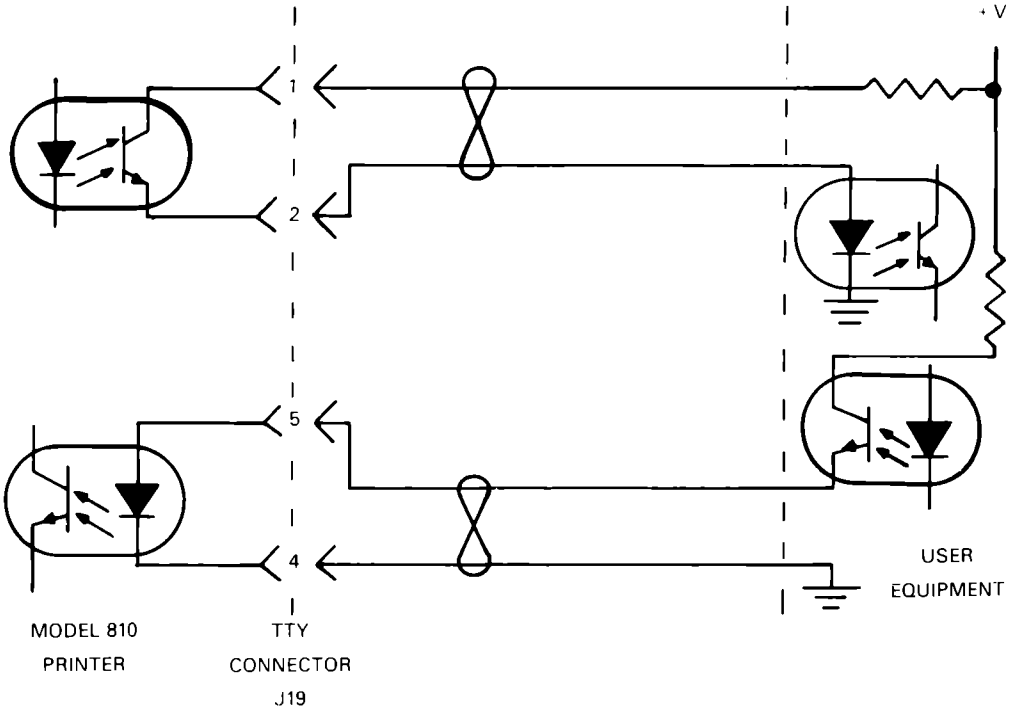


Figure A-3. Both Loops Powered by User Equipment

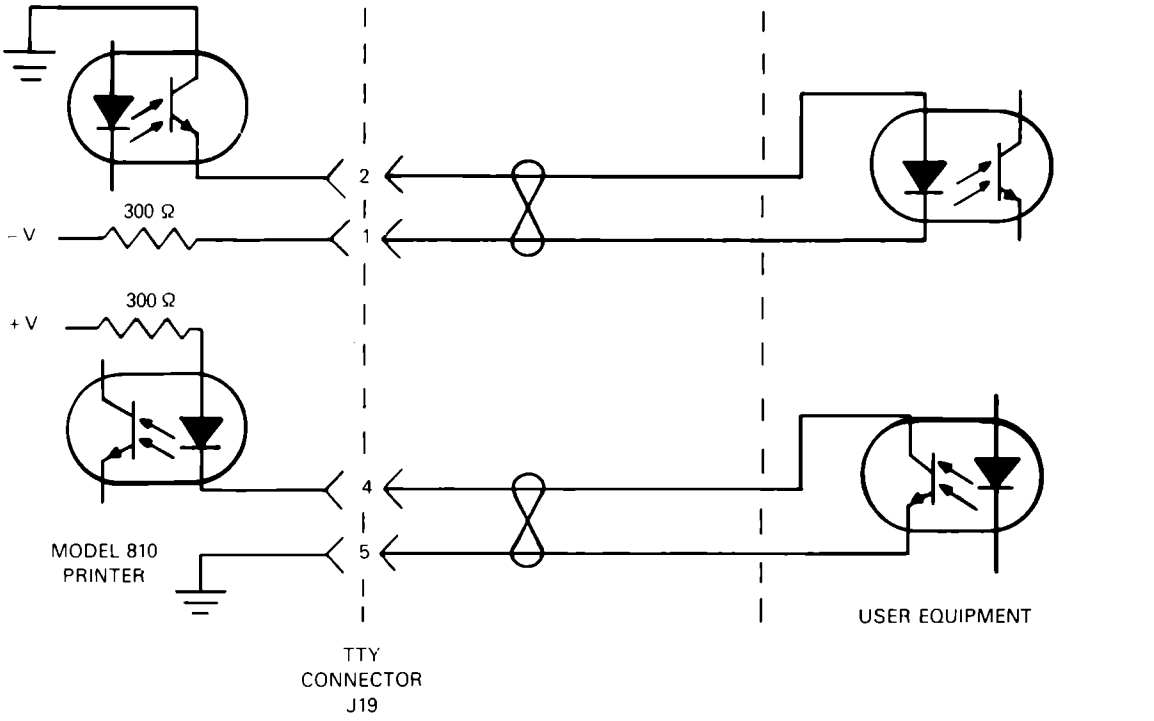


Figure A-4. Both Loops Powered by Printer

Serial Interface Instructions

Appendix B

RS-422 Interface

B.1 DIFFERENCES BETWEEN THE RS-232-C AND RS-422 INTERFACES

Before installing this option, the user should understand some significant differences between the RS-232-C and RS-422 interfaces.

RS-232-C is a complete definition of the interface between two units of data equipment for the purpose of interchanging serial binary data signals. It encompasses the physical interface (connector), transmission line, line driver and receiver electrical characteristics, and protocol (signal names and definitions, timing, and connector pin assignments).

RS-422 defines only the "electrical characteristics of balanced voltage digital interface circuits;" that is, the standard defines only the circuit characteristics for line driver and receiver circuits and the transmission line interconnecting them. A companion specification, RS-423, provides a similar definition of single-ended (unbalanced) circuits. RS-423 circuits are compatible with, but not identical to, RS-232-C circuits.

A third specification, RS-449, is roughly equivalent to a second-generation version of RS-232-C in that it is a complete definition of the interface between data communications equipment and data processing equipment. Rather than define the electrical characteristics of the interface circuits, however, RS-449 specifies the use of RS-422 circuits for high-frequency data and timing signals and RS-423 circuits for on/off control signals. The RS-449 interface is seldom used on any but the most complex data processing and communications equipment. The RS-422 and RS-423 circuits, however, are gaining increasing popularity in nonstandardized applications, such as local area networks and computer peripheral interfaces.

B.2 SIGNAL POLARITY

The nomenclature of the RS-422 signals can be somewhat misleading because negative logic convention is followed. Send – positive with respect to Send + and Receive – positive with respect to Receive + signifies MARK for data or **ON** for a control function. Note that RS-422 uses the same voltage significance for both data and control functions while for RS-232-C, a positive voltage signifies **ON** for control functions while a negative voltage signifies MARK for data.

Signal nomenclature and polarity of the serial interface option conform to the RS-422 definition and to the interface specification of the IBM Series/1 computer. Equipment of other manufacturers may use the opposite polarity and nomenclature. If this situation is encountered, reverse connections in the interface cable to the printer to obtain the correct polarity. This is another advantage inherent in differential balanced circuits.

INSTALLATION INSTRUCTIONS

CHARACTER SET OPTION KIT

MODEL 810 PRINTER

1.0 GENERAL

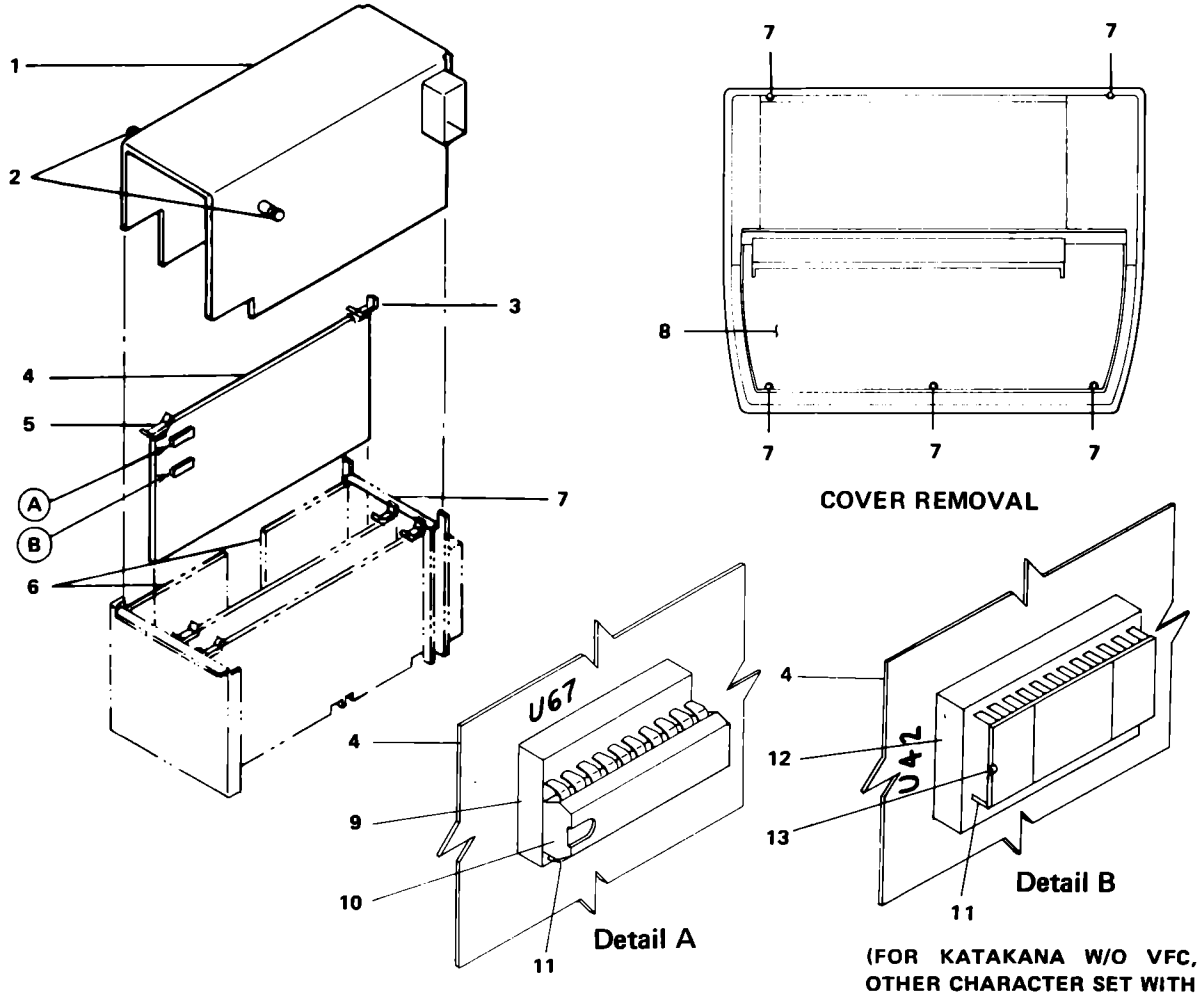
The character set option kit consists of a programmed PROM (and ROM for Katakana without VFC or other character set with VFC) which will be installed on the processor board assembly.

2.0 INSTALLATION

These instructions explain how to install the character set option kit in the Model 810 Printer. Refer to Figure 1 and proceed as follows:

WARNING

Disconnect power cord to prevent possible electrical shock.



(FOR KATAKANA W/O VFC, OR OTHER CHARACTER SET WITH VFC KIT.)

1. ELECTRONICS COVER
2. CAPTIVE SCREWS
3. GREEN EJECTOR
4. PROCESSOR BOARD (3rd BOARD FROM FRONT)
5. WHITE EJECTOR
6. OPTION BOARDS
7. SCREW
8. ACCESS DOOR
9. SOCKET XU67
10. PROM
11. PIN 1 OF PROM OR ROM
12. SOCKET XU42
13. ROM

994386-112

2. INSTALLATION (Continued)

1. Open access door.

2. Remove five screws securing cover.

3. Remove cover and locate electronics cover (at rear, right side of printer).

4. Loosen one screw and two captive screws on electronics cover.

5. Remove electronics cover.

6. Pull up on green ejector and white ejector to remove processor board (third board from front of printer).

7. Remove any PROM installed in socket XU67.

NOTE

Pin 1 of PROM must be at lower left side of socket XU67.

8. Install PROM supplied with kit in socket XU67.

9. For Katakana without VFC, or other character set with VFC Kit, install ROM (996279-0005) in socket XU42.

10. For all Katakana Kits install Dual Char Set Parity Selection Label (994451-0001) over corresponding portion (switch indications 4, 5, 6, 7) of Instruction Label (994352-0001) on underside of access door.

11. Replace processor board, electronics cover, and cover.

12. If the field installation kit is used, apply new configuration label as follows:

    a. Open access door and note original configuration label located on underside of access door.

    b. On new configuration label supplied with kit, check-mark those items which are checked on the original configuration label (except for character set options).

    c. On new configuration label, check that the mnemonic for the character set option that was installed is correct.

    d. Remove backing from new configuration label and apply new configuration label over original configuration label.

13. Close access door.

NOTES: 1. Expanded character kits are to be used with printers containing mechanisms 994291-0003 and 994291-0004 ONLY.
2. U.S. Full ASCII kits with dash nos. 0010, 8010, 0110, 8110 are to be used on processor board 994244-0001 ONLY.
3. U.S. Full ASCII kits with dash nos. 8019, 8119 are to be used on processor board 994244-0002 ONLY.
4. Kits with dash numbers 0023, 8023, 0024, and 8024 must have prom TI Part No. 994434-0099 installed in U67 and prom TI Part No. 994434-0023 or 994434-0024 installed in U55.

INSTALLATION INSTRUCTIONS

BAUD RATE OPTION KIT

MODEL 810 PRINTER

Kit Part Number	Kit Use
994445-0001, 994445-8001	Provides Baud rates of 110, 200, 300, 1200, 2400, 600 and 9600

1.0 GENERAL

The baud rate option kit consists of a TMS 5504 I/O and timer device which will be installed on th processor board assembly. Factory installation kits are identified as Part Number 994445-0001, fiel installation kits are identified as Part Number 994445-8001.

2.0 INSTALLATION

These instructions explain how to install the baud rate option kit in the Texas Instruments Model 81(Printer. Refer to Figure 1 and proceed as follows:

WARNING

Disconnect power cord to prevent possible electrical shock.

1. Open access door.
2. Remove five screws securing cover.
3. Remove cover and locate electronics cover (at rear, right side of printer).
4. Loosen one screw and two captive screws on electronics cover.
5. Remove electronics cover.
6. Pull up on green ejector and white ejector to remove processor board (third board from front o printer).
7. Remove any device installed in socket XU48.
8. Install TMS 5504 supplied with kit in socket XU48.

NOTE

Pin 1 of 5504 must be at lower right side of socket XU48.

9. Replace processor board, electronics cover, and cover.

10. If the field installation kit is used, apply new labels as follows:

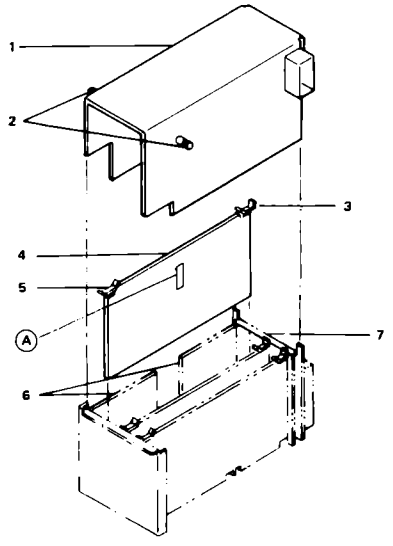
    a. Open access door and note original configuration label located on underside of access door.

    b. On new configuration label supplied with kit, check-mark those items which are checked on the original configuration label.

    c. On new configuration label, under processor option check mark the baud rate option (BRO).

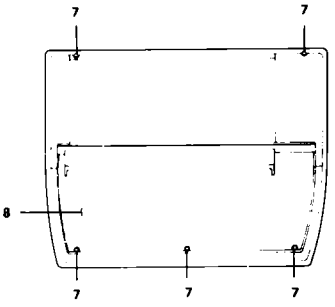
    d. Remove backing from new configuration label and apply new configuration label over original configuration label.

11. Close access door.

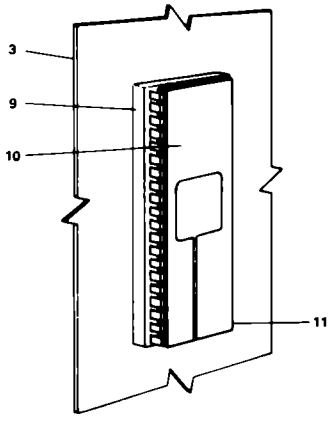


1. ELECTRONIC COVER
2. CAPTIVE SCREWS
3. GREEN EJECTOR
4. PROCESSOR BOARD (3rd BOARD FROM FRONT)
5. WHITE EJECTOR
6. OPTION BOARDS
7. SCREW
8. ACCESS DOOR
9. SOCKET XU48
10. TMS 5504
11. PIN 1 OF TMS 5504

A0001318



COVER REMOVAL



DETAIL A

994386-113

TI PUBLICATION 994515-9701
REVISION D

INSTALLATION INSTRUCTIONS
LINE BUFFER OPTION
MODEL 810 PRINTER

Kit Part Number	Kit Use
994511-0001	Factory installed kit enabling printer to receive data from an EIA source
994511-8001	Field installed kit, same capability as 994511 (above)
994512-0001	Factory installed kit enabling printer to receive data from a TTY current loop source
994512-8001	Field installed kit, same capability as 994512 (above)
994513-0001	Factory installed kit enabling printer to receive input from a parallel data source
994513-8001	Field installed kit, same capability as 994513 (above)

1.0 GENERAL

The Line Buffer Kit is available in three versions to accommodate three types of data sources:

Source	Version
EIA	LBE
TTY	LBT
PARALLEL	LBP

These kits convert the standard data input buffer from a 256-character FIFO to a 132-character line buffer. In addition, certain interface signals and status lines are changed.

WARNING

Before proceeding with the installation, remove the electrical power cable from the Model 810 Printer.

No special tools are required for this conversion; however, the following manuals should be at hand for ready reference:

Model 810 Maintenance Manual	994386-9701
Model 810 Operators' Manual	994353-9701

2.0 INSTALLATION — LBE OPTION KIT — P/N 994511

1. Remove printer and electronics cover.

2. Remove processor board (green ejector) and modify it for LBE as follows:

   a. Assembly no. 994244-0002 Rev P or later: Install jumper plugs from E11 to E12 and E13 to E15.

   b. Assembly No. 994244-0002 Rev N. Remove network SN7404 from U11 socket and clip network pins 2 and 6. Install network in socket U11.

   c. Assembly No. 994244-0002, Rev M or earlier. Cut pins 2 and 6 on network U11. Do not cut runs on PCB.

   d. Processor board jumpers must be configured to deselect DNB and IRC. Set jumper plugs for E4-E5 and E8-E9. (If BRO option is desired, the TMS 5501 (U48) must be replaced with a TMS 5504.)

3. Reinstall processor board in card slot XA2 (color code — green).

4. Remove resistor pack (U1) from socket XU1 on the motherboard. Save network for reconverting printer for use without LBE option card.

5. Set up Line Buffer strappable options per Table A-1.

6. A new configuration label is supplied with this kit. Fill out the label with the new configuration and install on the inside of the access door.

7. Affix the yellow color dot, P/N 231792-4 on the card file rail, XA3P1/XA3P2.

8. Install the Line Buffer Option board (994503-0002) in card slot XA3 (color code — yellow).

9. Replace electronics cover and printer cover.

10. Reconnect ac power.

2.1 INSTALLATION — LBT OPTION KIT — P/N 994512

1. Refer to Figure 2 and proceed as follows:

   a. Remove printer cover and electronics cover.

   b. Remove auxiliary input panel from rear of printer as follows:

      (1) Unplug existing option interface cable (if present) between panel and motherboard from motherboard.
      (2) Slide auxiliary input panel up and out of upper right rear slots in printer base.

2. Install all new auxiliary input panel (refer to figure 1) as follows:

   a. Slide auxiliary input panel with (TTY I/F) cable P/N 994361-1 to connector J15 on motherboard. Note that connector is keyed for proper orientation.

   b. Fasten loose end of safety ground strap (P/N 960967-3) to terminal E5 using external tooth lock washer and nut.

3. Remove the processor board (green ejector) and modify for Line Buffer Option (LBT) as follows:

   a. Assembly No. 994244-0002 Rev P or later: Install jumper plugs from E11 to E12 and E13 to E15.

   b. Assembly No. 994244-0002, Rev. N. Remove the network SN7404N from U11 socket and clip network pins 2 and 6. Reinstall network in socket U11.

   c. Assembly No. 994244-0002, Rev M or earlier. Cut pins 2 and 6 on network U11. Do not cut runs on PCB.

   d. Processor board jumpers must be configured to deselect DNB and IRC. Set jumper plugs for E4-E5 and E8-E9. (If BRO option is desired, the TMS 5501 (U48) must be replaced with a TMS 5504.)

4. Reinstall processor board in card slot XA2 (color code — green).

5. Remove resistor pack (U1) from socket XU1 on the motherboard. Save network for reconverting the printer for use without the LBT option card.

6. Set up line buffer card strappable options per Table A-2.

7. Affix the yellow dot (P/N 231792-4) as shown (Figure 2).

8. Install the Line Buffer Option board (P/N 994503-0002) in card slot XA3 (color code — yellow).

9. A new configuration label is supplied with this kit. Transfer all configuration information to the new label and install on inside of access door.

10. Reinstall electronics cover and printer cover.

11. Reconnect ac power.

2.2 INSTALLATION — LBP OPTION KIT — P/N 994513-0001

1. Remove printer cover and electronics cover.

2. Remove auxiliary input panel from rear of printer as follows:

   a. Unplug existing option interface cable (if present) between panel and motherboard from motherboard.

   b. Slide auxiliary input panel up and out of upper right rear slots in printer base.

3. Install new auxiliary input panel as follows:

   a. Slide auxiliary input panel (with parallel interface cable attached) into upper right rear slots in printer base. Panel should be oriented so that the word "PARALLEL" can be read from outside rear of the printer.

   b. Connect loose end of parallel interface cable (P/N 994359-2) to connector J14 on motherboard. Note that the connector is keyed for proper orientation.

   c. Fasten loose end of safety ground strap (P/N 960967-3) and ground strap from parallel interface cable to terminal E5 using external tooth lock washer and nut.

4. Remove the processor board (green ejector) and modify for Line Buffer Option (LBP) as follows:

   a. Assembly No. 994244-0002 Rev P or later. Install jumper plugs from E11 to E12 and E13 to E15.

   b. Assembly No. 994244-0002 Rev N. Remove network SN7404N from U11 socket and clip network pins 2 and 6. Reinstall network in socket U11.

   c. Assembly No. 994244-0002 Rev M or earlier. Cut pins 2 and 6 on network U11. Do not cut runs on PCB.

   d. Processor board jumpers must be configured to deselect DNB and IRC. Set jumper plugs for E4-E5 and E8-E9.

5. Reinstall processor board in card slot XA2 (color code — green).

6. Remove resistor pack, U1, from socket, XU1, on the motherboard. Save network for reconverting printer for use without the LBP option.

7. Set up Line Buffer strappable options per Table A-3.

8. Affix the yellow dot (P/N 231792-4) as shown in Figure 4.

9. Install the Line Buffer Option board (994503-0001) in card slot XA3 (color code — yellow).

10. A new configuration label is supplied with this kit. Transfer all configuration information to the new label and install on the inside of the access door.

11. Replace electronics cover and printer cover.

12. Reconnect ac power.

3.0 LINE BUFFER STRAPPABLE OPTIONS

DSC OPTION

Functional on LBE, LBP and LBT option boards.

E1-E2 Printer normally prints buffered characters only on receipt of CR or 132 printable characters.

E2-E3 Option enabled provides for printing of buffered characters on receipt of CR, LF, FF, VT or 132 printable characters.

BRO OPTION

Functional on LBE and LBT option boards.

E4-E5 Provides for complementary operation with TMS 5501 on processor board to accept data at 110, 150, 300, 1200, 2400, 4800, 9600 baud.

E5-E6 Option enabled provides for complementary operation with TMS 5504 on processor board to accept data at 110, 200, 300, 1200, 2400, 600, 9600 baud. (Baud rates of 200 and 600 respectively are substituted for 150 and 4800.)

DCO OPTION

E17-E18 DC1/DC3 characters recognized for on line/off line control.

E17-E16 Disable DC1/DC3 control.

DNB OPTION

Functional on LBE option board only; same as DNB option on processor board.

E8-E9 Sets DTR = on line.

E7-E8 Option enabled provides for DTR = on line and not Busy.

IRC OPTION

Functional on LBE option board only; same as IRC function on processor board.

E10-E11 Sets reverse channel = Busy.

E11-E12 Option enabled provides for reverse channel = $\overline{\text{Busy}}$.

GDS OPTION

Functional on LBE, LBP and LBT option boards. (This option must be enabled if either HDP or GED are enabled.)

E19-E20 Provides for normal acceptance of at least five characters during a "Printer Busy" condition.

E20-E21 Option enabled ignores any characters received during a "Printer Busy" condition.

HDP OPTION

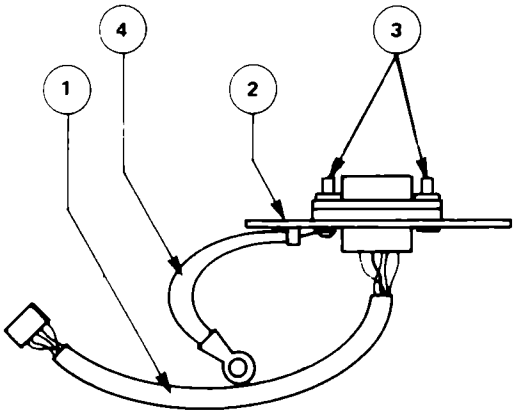
Functional on LBT option board only.

Rev C and earlier:	E27-E28 E29-E30	
Rev D:	E29-E30	Provides for operation in the normal four-wire full duplex mode
Rev E and later:	E29-E30 E32-E33	
All Revisions:	E13-E14 E25-E26 E20-E21	Option enabled provides for two-wire half duplex operation. Transmitter, receiver wired in series. (Positive current in TTY received data, pin 5, and returned through TTY transmitted data return, pin 2.)

GED OPTION

Functional on LBE option board Rev D and later only.

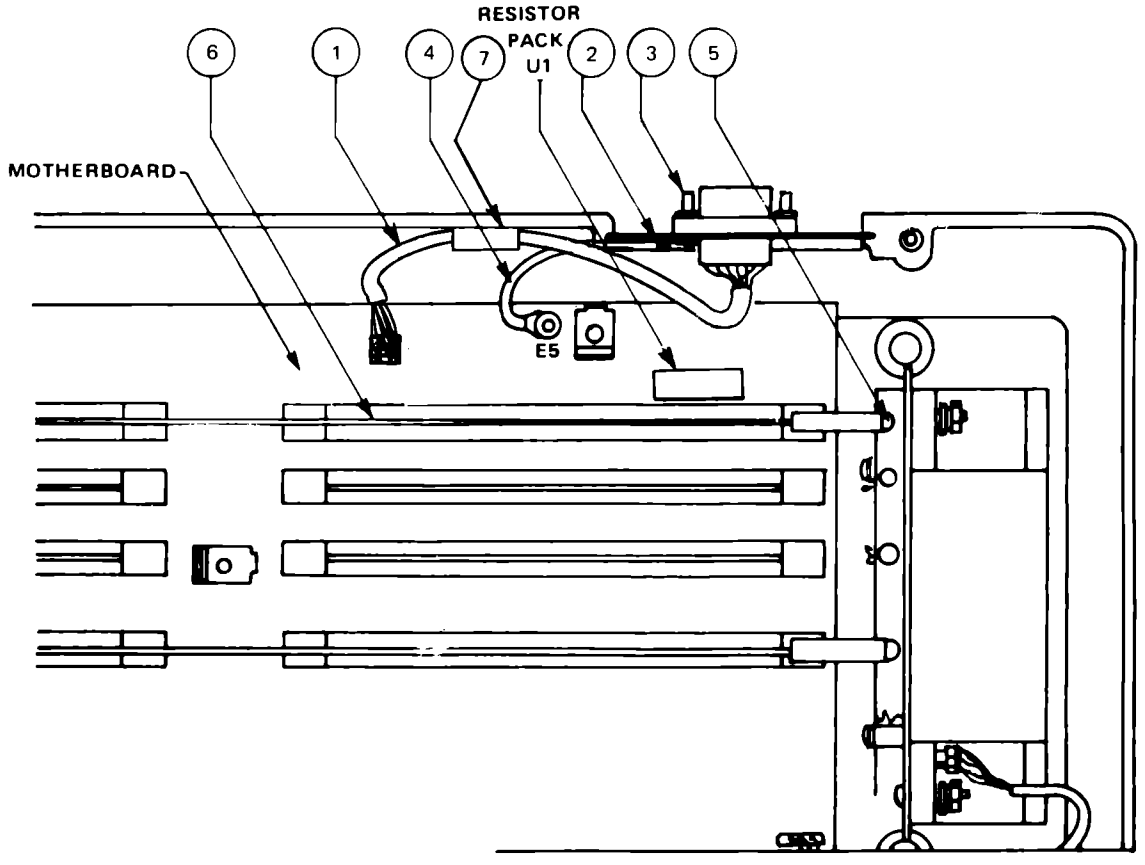
Rev D only	No jumper	Provides for normal acceptance of at least 5 characters during a "Printer Busy" condition.
Rev E and later:	E28-E31	
All Revisions	E27-E28	Option enabled ignores any characters received during a "Printer Busy" condition.
	E20-E21	



1. TTY I/F Cable Part Number 994361-1
2. Auxiliary Input Panel
3. Screw Lock Assemblies
4. Safety Ground Strap

994386-114

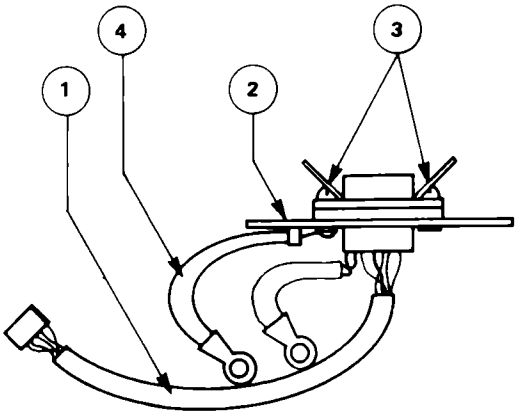
Figure 1. Detail of TTY Interface Cable and Safety Ground Strap to Auxiliary Input Panel.



1. TTY I/F Cable, Part Number 994361-1
2. Auxiliary Input Panel, Part Number 994333-3
3. Screw Lock Assemblies, Part Number 406769-1
4. Safety Ground Strap, Part Number 960967-3
5. Yellow Dot, Part Number 231729-4
6. LBT Assembly, Part Number 994503-2
7. Clip, Part Number 996729-1

994386-115

Figure 2. LBT I/F Kit Installation on Model 810 Printer.

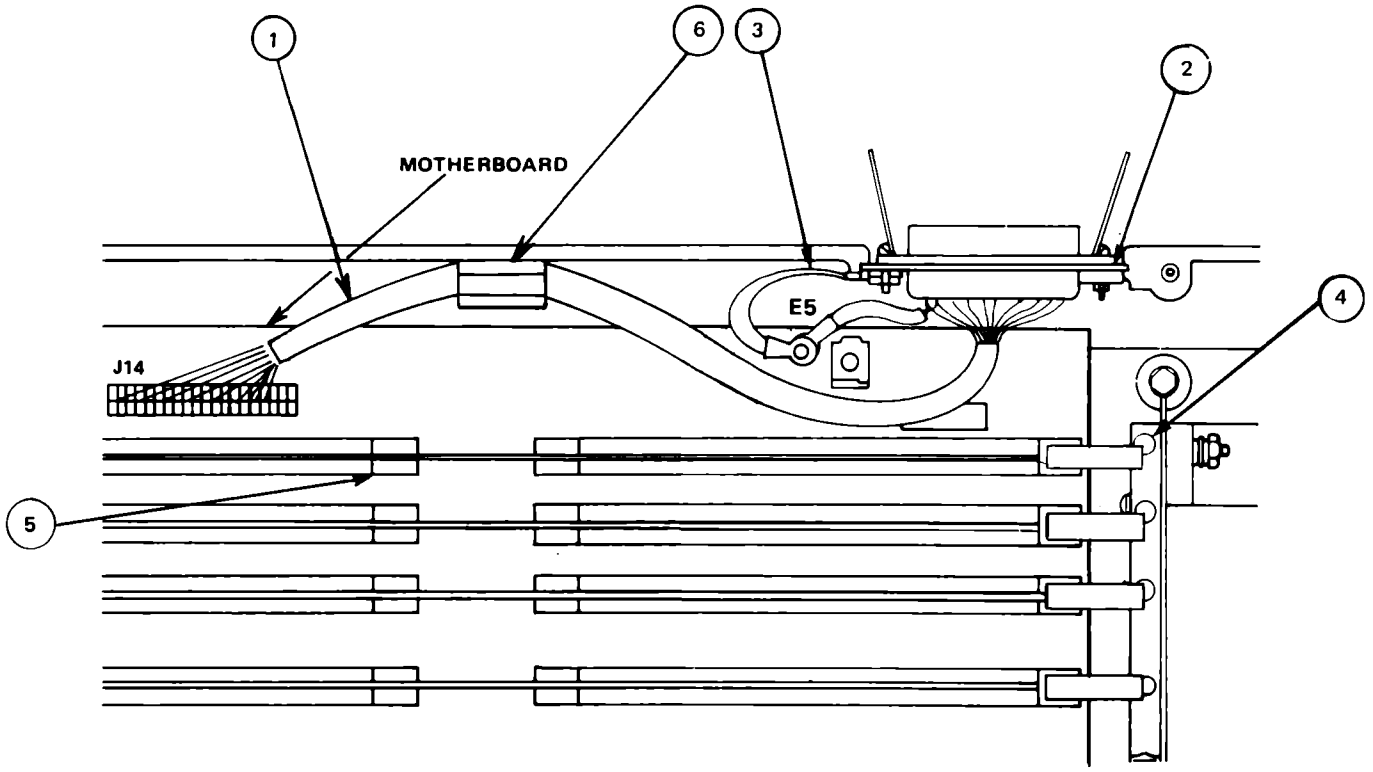


1. Parallel Interface Cable, Part Number 994359-2
2. Auxiliary Input Panel
3. Screw, and Lock Washers
4. Safety Ground Strap

994386-116

A000 1323

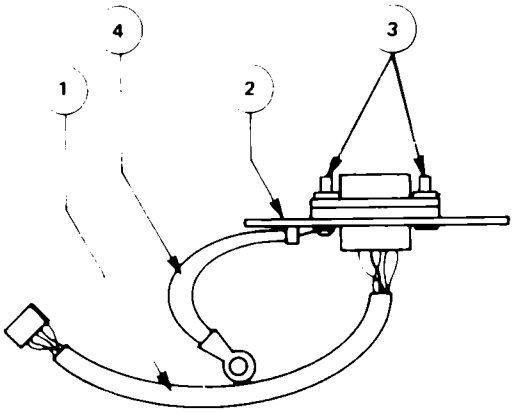
Figure 3. Detail of Parallel Interface Cable and Safety Ground Strap



1. Parallel Interface Cable, 994359-2
2. Auxiliary Input Panel, Part Number 994333-2
3. Safety Ground Strap, Part Number 960967-3
4. Yellow Dot, Part Number 231792-4
5. LBP Assembly, Part Number 994503-1
6. Clip, Part Number 996729-1

994386-117

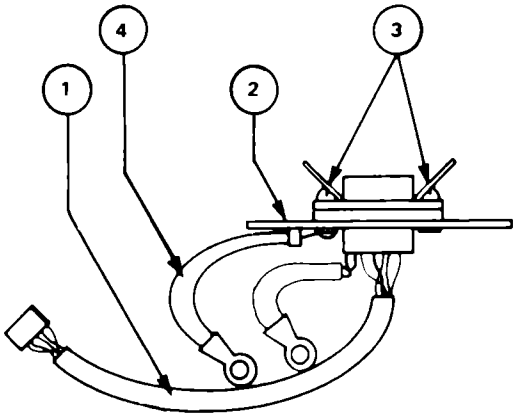
Figure 4. LBP Interface Installation on Model 810 Printer



1. TTY I F Cable Part Number 994361-1
2. Auxiliary Input Panel, Part Number 994333-3
3. Screw Lock Assemblies, Part Number 406769-1
4. Safety Ground Strap, Part Number 960967-3

994386-118

Figure 5. Assembly of TTY Interface Cable and Safety Ground Strap to Auxiliary Input Panel.



1. Parallel Interface Cable, Part Number 994359-2
2. Auxiliary Input Panel, Part Number 994333-2
3. Screw, and Lock Washers
4. Safety Ground Strap, Part Number 960967-3

994386-119

A000 1323

Figure 6. Assembly of Parallel Interface Cable and Safety Ground Strap to Auxiliary Input Panel.

TABLE F-1. SUMMARY OF LBE STRAPPABLE OPTIONS

NOTES

1. (n) indicates DESELECTED position.
2. Mandatory positions listed below MUST be set.

Suboption		LBE Revision Level		
		Rev. E And Later	**Rev. D**	**Rev. C And Earlier**
DSC	(Decode Carriage Return)	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]
BRO[2]	(Baud Rate Option)	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504
DNB[3]	(Data Terminal Not Busy)	E8-E9 (n) on line E7-E8 on line and not busy	E8-E9 (n) on line E7-E8 on line and not busy	E8-E9 (n) on line E7-E8 on line and not busy
IRC[3]	(Inverse Reverse Channel)	E10-E11 (n) Reverse Channel = Busy E11-E12 Reverse Channel = $\overline{\text{Busy}}$	E10-E11 (n) Reverse Channel = Busy E11-E12 Reverse Channel = $\overline{\text{Busy}}$	E10-E11 (n) Reverse Channel = Busy E11-E12 Reverse Channel = $\overline{\text{Busy}}$
GDS[4]	(Gated Data Strobe)	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe ungated E20-E21 Data Strobe gated
GED	(Gated EIA Data)	E28-E31 (n) EIA Data Ungated E27-E28, E20-E21 EIA Data Gated	No Jumper (n) EIA Data Ungated E27-E28, E20-E21 EIA Data Gated	Suboption Not Available
	Mandatory Position of Other LBE Jumpers	E29-E30 E26-E34	E29-E30	E27-E28 E29-E30

[1]Or 132 characters.
[2]This option must also be configured on the processor board.
[3]These options must be deselected on the processor board.
[4]E20-E21 when GED is selected.

TABLE F-2. SUMMARY OF LBT STRAPPABLE OPTIONS

NOTES

1. (n) indicates DESELECTED position.
2. Mandatory positions listed below MUST be set.

Suboption		LBT Revision Level		
		Rev. E And Later	**Rev. D**	**Rev. C And Earlier**
DSC	(Decode Carriage Return)	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]
BRO[2]	(Baud Rate Option)	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504
GDS[3]	(Gated Data Strobe)	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated
HDP	(Half Duplex Mode)	E29-E30 } (n) Full Duplex E32-E33 } E13-E14 } Half Duplex E25-E26 }	E29-E30 (n) Full Duplex E13-E14 } E20-E21 } Half Duplex E25-E26 }	E27-E28 } Full E29-E30 } (n) Duplex E13-E14 } E20-E21 } Half E25-E26 } Duplex
	Mandatory Position of Other LBT Jumpers	E8-E9 E10-E11 E28-E31	E8-E9 E10-E11	E8-E9 E10-E11

[1]Or 132 characters.
[2]This option must also be configured on the processor board.
[3]E20-E21 when HDP is selected.

TABLE F-3. SUMMARY OF LBP STRAPPABLE OPTIONS

NOTES

1. (n) indicates DESELECTED position.
2. Mandatory position listed below MUST be set.

Suboption		LBP Revision Level		
		Rev. E And Later	**Rev. D**	**Rev. C And Earlier**
DSC	(Decode Carriage Return)	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]
GDS	(Gated Data Strobe)	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated
	Mandatory Position of Other Jumpers on LBP Board	E4-E5 E8-E9 E10-E11 E29-E30 E32-E33 E28-E31	E4-E5 E8-E9 E10-E11 E29-E30	E4-E5 E8-E9 E10-E11 E27-E28 E29-E30

[1]Or 132 characters.

TI PUBLICATION 999940-9701
ISSUED 1 OCTOBER 1978
REVISION A

INSTALLATION INSTRUCTIONS
*OMNI 800** TERMINAL STAND PAPER BASKET

PART NO. 999839-0001

1. GENERAL

The Terminal Stand Paper Basket kit consists of the paper basket and static ground cable for attachment to the Texas Instruments *Omni 800** printer terminal stand.

2. INSTALLATION

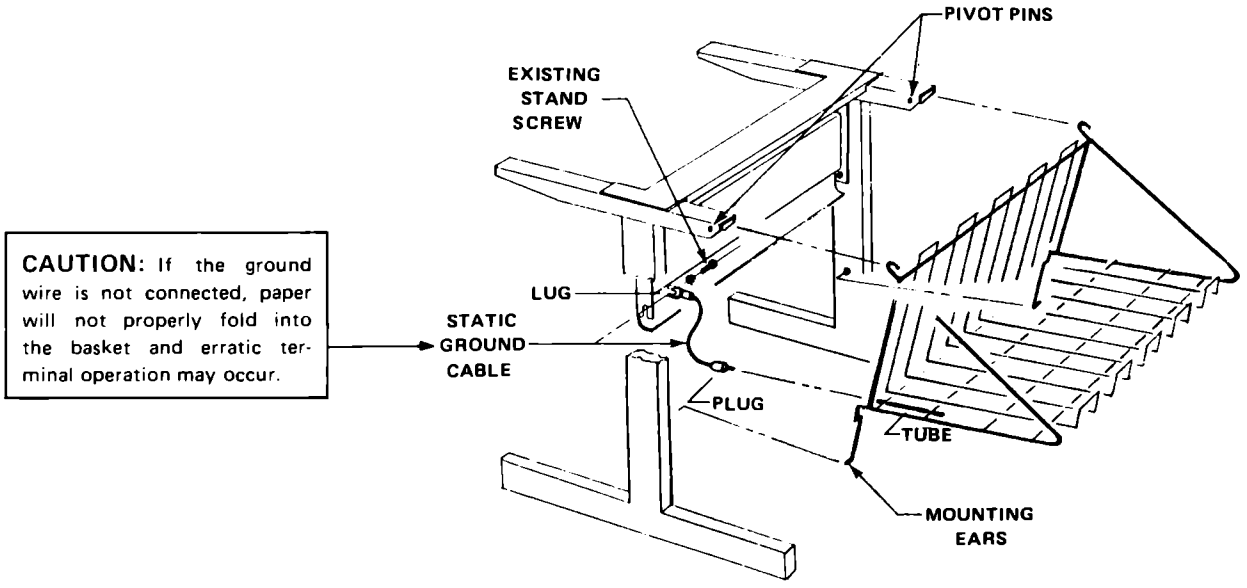
These instructions explain how to attach the paper basket to the terminal stand. Refer to the figure and proceed as follows:

a. Remove the existing stand screw from stand.

b. Attach the static ground cable lug to the stand using the existing stand screw removed in step a.

c. Attach the paper basket by hooking the basket onto the terminal stand pivot pins. Then rotate the basket downward, deflect basket mounting ears inward, and insert the ears into the holes in the terminal stand legs.

d. Connect the ground cable banana plug into the tube on the basket as shown in the figure.



*Omni 800** **Terminal Stand Paper Basket**

994386-119

*Trademark of Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED

*OMNI 800** **Model 810 Printer**
Terminal Paper Basket Kit (TI Part No. 994442-0001)
Installation Instructions

DESCRIPTION

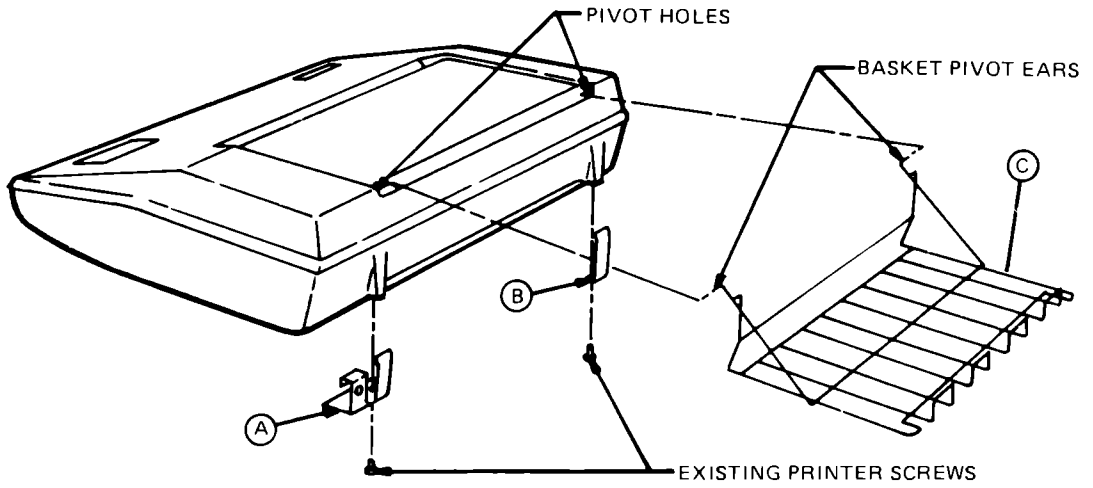
The Terminal Paper Basket Kit provides a paper basket for the Texas Instruments Model 810 Printer. The kit consists of the basket and all necessary hardware to attach the paper basket to the Model 810.

NOTE

Printers configured after February 15, 1981, have static ground brackets installed on the printer and can omit steps 2 and 3 of the PROCEDURE below. Customers who order a paper basket for printers configured before February 15, 1981, will be furnished static ground brackets free of charge on request. (The configured date is the date shown under "NOTES:" on the label marked "810 PRINTER CONFIGURATION" located on the underside of the front access door.)

PROCEDURE (Refer to the Figure)

1. Set the ON/OFF switch to the OFF position. Disconnect the power cord from the wall outlet.
2. Remove the two existing printer screws from the rear paper chute.
3. Attach the left (A) and right (B) static ground brackets to the printer using the existing screws removed in the previous step.
4. Attach the basket (C) by deflecting the top of basket pivot ears and inserting the ears into the pivot holes in the printer top cover.
5. Return the printer to operation.



994441-1

994386-120

A — Bracket, Left — Static Ground (TI Part No. 2360075-0001)
B — Bracket, Right — Static Ground (TI Part No. 994438-0002)
C — Paper Basket (TI Part No. 994176-0001)

*Trademark of Texas Instruments Incorporated.

TI Part No. 994441-9701 Rev. B

Appendix G

TMS 6011 Data Sheets

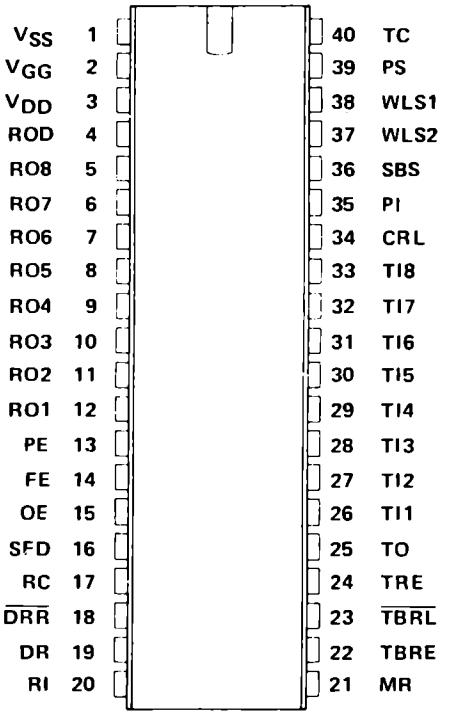
This section contains data sheets on TMS 6011.

TMS 6011 JC, NC
ASYNCHRONOUS DATA INTERFACE (UART)

BULLETIN NO. DL S 7512275, MAY 1975

- Transmits, Receives, and Formats Data
- Full-Duplex or Half-Duplex Operation
- Operation from DC to 200 kHz
- Static Logic
- Buffered Parallel Inputs and Outputs
- Programmable Word Lengths . . . 5, 6, 7, 8 Bits
- Programmable Information Rate
- Programmable Parity Generation/Verification
- Programmable Parity Inhibit
- Automatic Data Formatting
- Automatic Status Generation
- 3-State Push-Pull Buffers
- Low-Threshold Technology
- Standard Power Supplies . . . 5 V, −12 V
- Full TTL Compatibility . . . No External Components

40-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 6011 JC, NC is an MOS/LSI subsystem designed to provide the data interface between a serial communications link and data processing equipment such as a peripheral or a computer. The device is often referred to as an asynchronous data interface or as a universal asynchronous receiver/transmitter (UART).

The receiver section of the TMS 6011 will accept serial data from the transmission line and convert it to parallel data. The serial word will have start, data, and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking proper start, parity, and stop bits, and will convert the data to parallel.

The transmitter section will accept parallel data, convert it to serial form, and generate the start, parity, and stop bits.

The TMS 6011 is a fully programmable circuit allowing maximum flexibility of operation, defined as follows:

- The receiver and transmitter sections are separate and can operate either in full-duplex (simultaneous transmission and reception) or in half-duplex mode (alternate transmission and reception).
- The data word may be externally selected to be 5, 6, 7, or 8 bits long.
- Baud rate is externally selected by the clock frequency. Clock frequency can vary between 0 and 200 kHz.
- Parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification.
- The stop bit can be selected as either a single- or a double-bit stop.
- Static logic is used to maximize flexibility of operation and to simplify the task of the user. The data holding registers are static and will hold a data word until it is replaced by another word.
- Asynchronous operation allows the use of a single transmission line. The clock period has to be within ±4% of 1/16 of the time for one bit for the transmitter and/or receiver but no phase relationship is required.

description (continued)

To allow for a wide range of possible configurations, three-state push-pull buffers have been used on all outputs except **Transmitter Output (TO)** and **Transmitter Register Empty (TRE)**. They allow the wire-OR configuration.

The TMS 6011 can be used in a wide range of data handling equipment such as modems, peripherals, printers, data displays, and minicomputers. By taking full advantage of the latest MOS/LSI design and processing techniques, it has been possible to implement the entire transmit, receive, and format function necessary for digital data communication in a single package, avoiding the cumbersome circuitry previously necessary.

P-channel enhancement-type low-threshold technology permits the use of standard power supplies (5 V, −12 V) as well as direct TTL interface. No external components are needed.

The TMS 6011 is offered in both 40-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from −25°C to 85°C.

operation

The operation can be best understood by visualizing the TMS 6011 as three separate sections: 1) common control, 2) transmitter, and 3) receiver. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

common control section

The common control section will direct both the receiver and the transmitter sections.

The initialization of the TMS 6011 is performed through the **Master Reset (MR)** terminal. The **MR** terminal is strobed to a high level after power turn-on to reset all status and transmitter registers and to reset **Transmitter Output (TO)** to a high level. The **Receiver Outputs (RO1-RO8)** are not controlled by the **MR** terminal.

Status flags **Parity Error, Framing Error, Overrun Error, Data Ready,** and **Transmitter Buffer Register Empty** are disabled when the **Status Flags Disable (SFD)** is at a high level. When disabled, the status flags float (three-state buffers are in the high-impedance state). The **Transmitter Register Empty (TRE)** status flag is not a three-state output.

The number of bits per word is controlled by the **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)** inputs. The word length may be 5, 6, 7, or 8 bits. Selection is as follows:

WORD LENGTH	WLS1	WLS2
5	Low	Low
6	High	Low
7	Low	High
8	High	High

The parity to be checked by the receiver and generated by the transmitter is determined by the **Parity Select (PS)** input. A high level on the **PS** input selects even parity and a low level selects odd parity.

The parity will not be checked or generated if a high level is applied to **Parity Inhibit (PI)**; in this case the stop bit or bits will immediately follow the data bit.

When a high level is applied to **PI**, the **Parity Error (PE)** status flag is brought to a low level indicating a no-parity error because parity is disregarded in this mode.

To select either one or two stop bits, the **Stop Bit(s) Select (SBS)** terminal is used. A high level at this terminal will result in two stop bits while a low level will produce only one.

To load the control bits (**WLS1, WLS2, PS, PI,** and **SBS**) a high level is applied to the **Control Register Load (CRL)** terminal. This terminal may be strobed or hard wired to a high level.

operation (continued)

transmitter section

The transmitter section will accept data in parallel form, then serialize, format, and transmit the data in serial form.

Parallel input data is received through the **Transmitter Inputs (TI1-TI8)**.

Serial output data is transmitted from the **Transmitter Output (TO)** terminal.

Input data is stored in the transmitter-buffer register. A low level at the **Transmitter Buffer Register Load ($\overline{\text{TBRL}}$)** command terminal will load a word in the transmitter-buffer register. The length of this word is determined by **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)**. If a word of length greater than this appears at **TI8** through **TI1**, only the least significant bits are accepted. The word is justified into the least significant bit, **TI1**.

The data is transferred to the transmitter register when the **$\overline{\text{TBRL}}$** terminal goes from low to high. The loading of the transmitter register is delayed if the transmitter section is presently transmitting data. In this case the loading of the transmitter register is delayed until the transmission has been performed.

Output serial data (transmitted from the **TO** terminal) is clocked out by **Transmitter Clock (TC)**. The clock rate is 16 times faster than the data rate.

The data is formatted as follows: start bit, data, parity bit, stop bits (1 or 2). Start bits, parity bits, and stop bits are generated by the TMS 6011. When no data is transmitted the output **TO** remains at a high level.

The start of transmission is defined as the transition of **TO** from a high to a low logic level.

Two flags are provided. A high level at the **Transmitter Buffer Register Empty (TBRE)** flag indicates that a word has been transferred to the transmitter/receiver and that the transmitter buffer register is now ready to accept a new word. A high level at the **Transmitter Register Empty (TRE)** flag indicates that the transmitter section has completed the transmission of a complete word including stop bits. The **TRE** flag will remain at a high level until the start of transmission of a new word.

Both the transmitter buffer register and the transmitter register are static and will perform long-term storage of data.

receiver section

The data is received in serial form at the **Receiver Input (RI)**. The data from **RI** enters the receiver register at a point determined by the character length, the parity, and the number of stop bits. **RI** must be maintained high when no data is being received. The data is clocked by the **Receiver Clock (RC)**. The clock rate is 16 times faster than the data rate.

Data is transferred from the receiver register to the receiver buffer register. The output data is then presented in parallel form at the eight **Receiver Outputs (RO1** through **RO8)**. The MOS output buffers used for the eight **RO** terminals are three-state push-pull output buffers that permit the wire-OR configuration through use of the **Receiver Output Disable (ROD)** terminal. When a high level is applied to **ROD** the **RO** outputs are floating. If the word length is less than 8 bits, the most significant bits will be at a low level. The output word is right justified. **RO1** is the least significant bit and **RO8** is the most significant bit.

A low level applied to the **Data Ready Reset ($\overline{\text{DRR}}$)** terminal resets the **Data Ready (DR)** output to a low level.

Several flags are provided in the receiver section. There are three error flags (**Parity Error, Framing Error,** and **Overrun Error**) and a **DR** flag. These status flags may be disabled by a high level at the **Status Flags Disable (SFD)** terminal.

A high level at the **Parity Error (PE)** terminal indicates an error in parity.

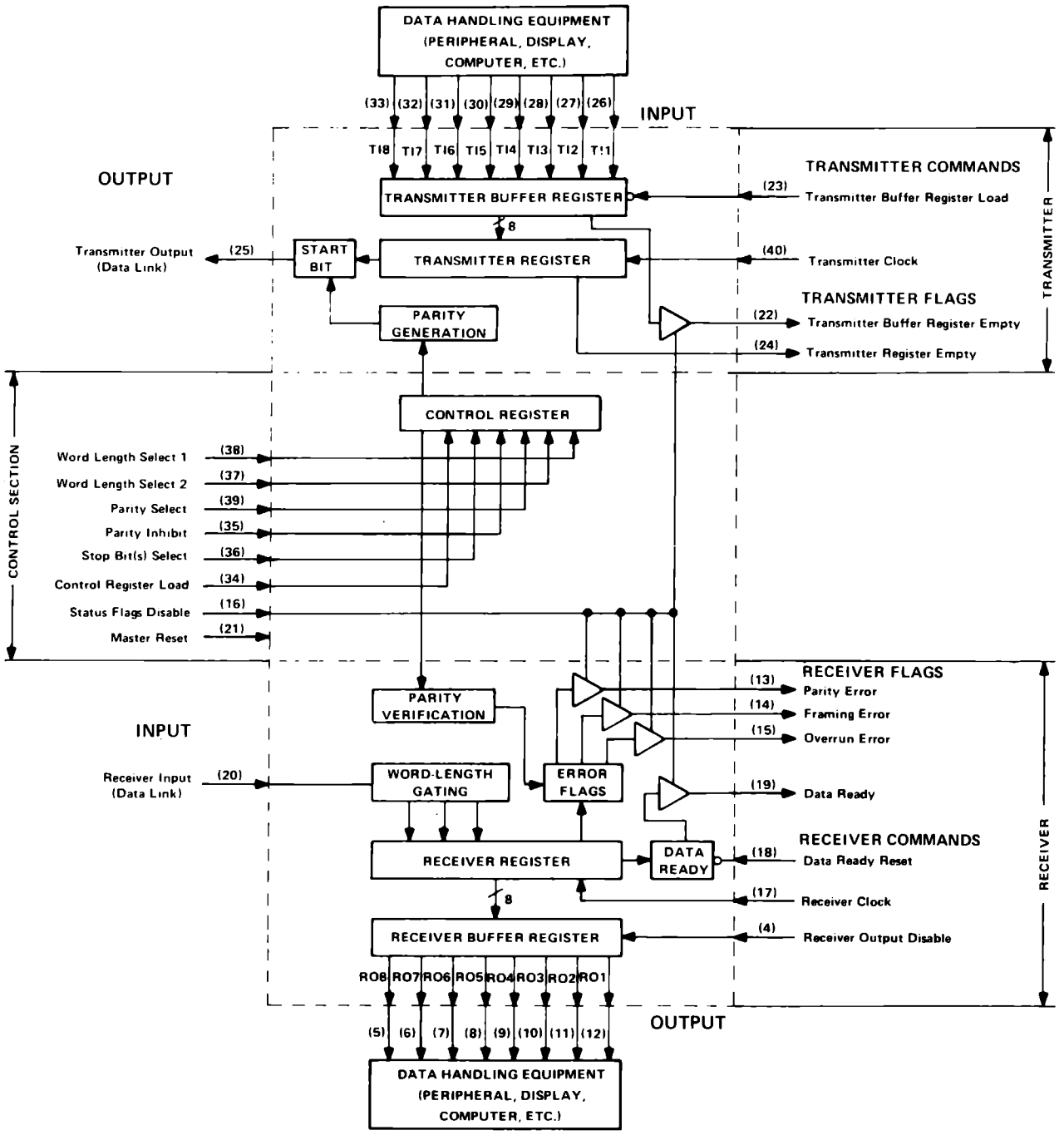
A high level at the **Framing Error (FE)** terminal indicates a framing error that is an invalid or nonexistent stop bit in the received word.

operation (continued)

A high level at the **Overrun Error (OE)** terminal indicates an overrun. An overrun occurs when the previous word has not been read, i.e., when the **DR** output has not been reset before the present data was transferred to the receiver buffer register.

A high level at the **DR** terminal indicates that a word has been received, stored in the receiver-buffer register and that the data is available at outputs **RO1** through **RO8**. The **DR** terminal can be reset through the $\overline{\textbf{DRR}}$ terminal.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Input voltage (any input) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			0		V
Supply voltage, V_{GG}		−11.5	−12	−12.5	V
Supply voltage, V_{SS}		4.75	5	5.25	V
High-level input voltage, all inputs, V_{IH} (see Notes 2 and 3)		V_{SS} −1.5		V_{SS} +0.3	V
Low-level input voltage, all inputs, V_{IL} (see Notes 2 and 3)		−12		0.8	V
Pulse width, t_w	Clock	2.5			μs
	Transmitter buffer register load	400			ns
	Control register load	250			ns
	Parity inhibit (see Notes 4 and 5)	400			ns
	Parity select (see Notes 4 and 5)	300			ns
	Word length select and stop bit select (see Notes 4 and 5)	300			ns
	Master reset	1.5			μs
	Data ready reset	250			ns
Data setup time, $t_{su(da)}$		10↓			ns
Data hold time, $t_{h(da)}$		20↑			ns
Clock frequency, f_ϕ (see Note 6)		0		200	kHz
Operating free-air temperature, T_A		−25		85	°C

NOTES: 2. All data, clock, and command inputs have internal pull-up resistors to allow direct clocking by any TTL circuit.
3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.
4. Inputs to PI, PS, WLS1, WLS2, and SBS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.
5. All control signal pulses should be centered with respect to CRL to ensure maximum setup and hold time.
6. Clock frequency is 16 times the baud rate.

↑↓The arrow indicates the edge of the $\overline{TBRL}$ pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.6	V
I_{IH}	High-level input current, all inputs	V_I = 5 V			10	μA
I_{IL}	Low-level input current, all inputs	V_I = 0 V			−1.6	mA
I_{GG}	Supply current from V_{GG}	All inputs at a high level		11	16	mA
I_{SS}	Supply current from V_{SS}	All inputs at a high level		20	35	mA
P_D	Power dissipation	All inputs at a high level		240	385	mW
C_i	Input capacitance, all inputs	V_I = V_{SS}, f = 1 MHz		10	20	pF

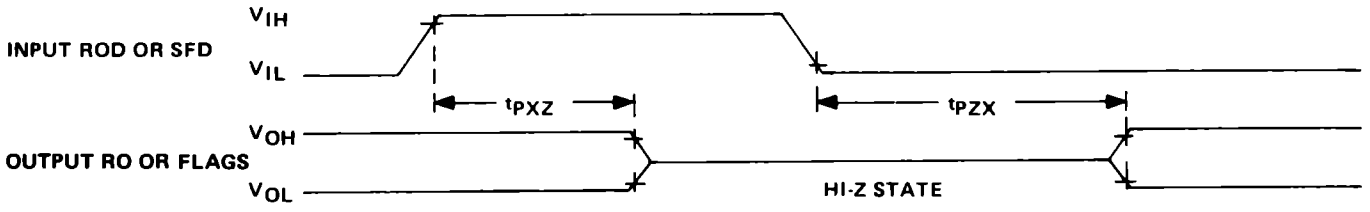
†All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

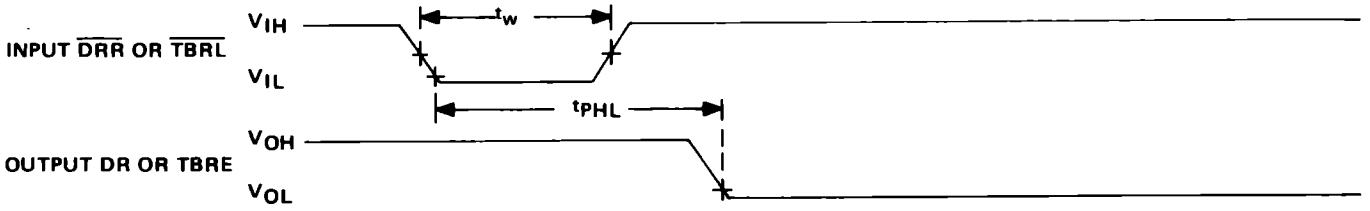
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level DR output from $\overline{DRR}$	1 Series 74 TTL load		800	1000	ns
t_{PHL}	Propagation delay time, high-to-low level TBRE output from $\overline{TBRL}$			800	1000	ns
t_{PZX}	Enable time, receiver output from ROD			300	500	ns
t_{PXZ}	Disable time, receiver output from ROD			300	500	ns
t_{PZX}	Enable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns
t_{PXZ}	Disable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns

†All typical values are at $T_A = 25°C$ and nominal voltages.

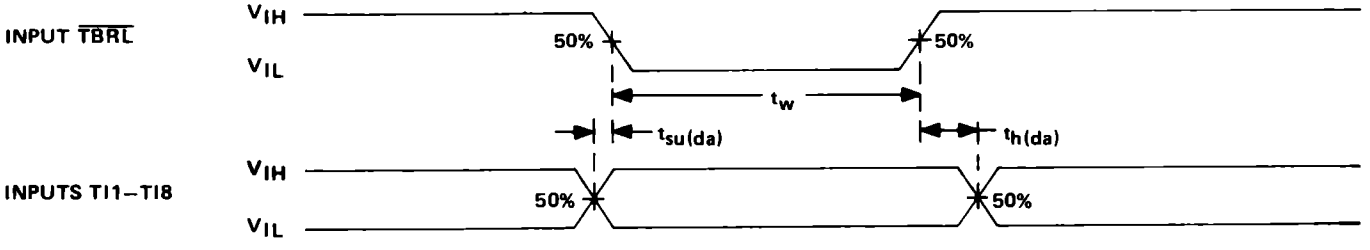
voltage waveforms



ENABLE AND DISABLE TIMES



PROPAGATION DELAY TIMES

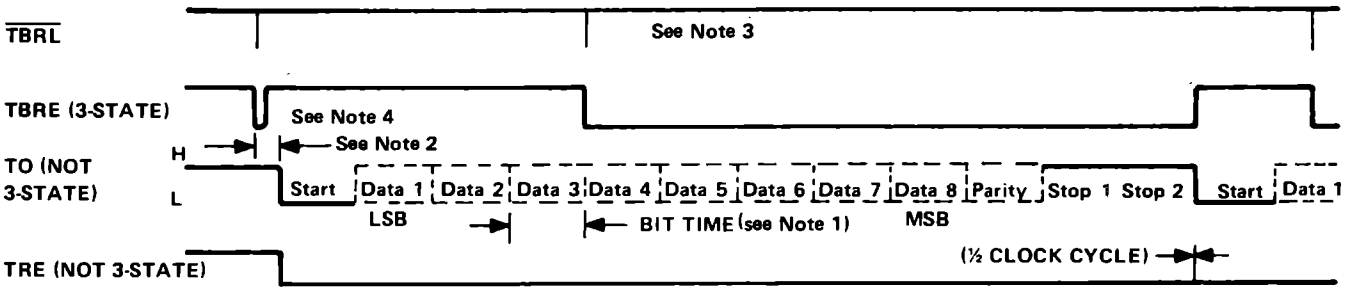


DATA SETUP AND HOLD TIMES

NOTE: All enable, disable, and propagation delay times are referenced to the 90% or 10% points. All pulse widths are referenced to the 50% points.

operation timing diagram

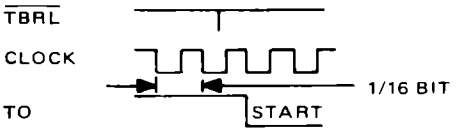
TRANSMITTER TIMING†



† Transmitter initially assumed inactive at start of diagram, shown for 8 level code and parity and 2 stops.

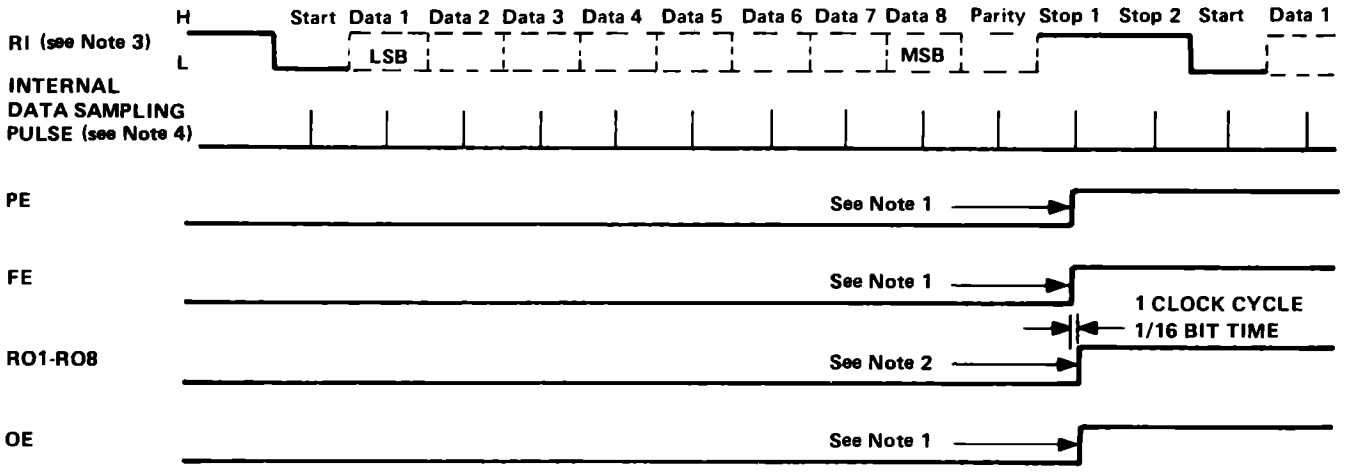
NOTES: 1. Bit time is 16 clock cycles.

2. If transmitter is inactive the start pulse will appear on line within one clock cycle of time data strobe occurs (see detail below).



3. Because transmitter is double buffered, another data strobe can occur anywhere during transmission of character 1.
4. TBRE goes to a low for a period of approximately one clock cycle following a $\overline{\text{TBRL}}$ pulse.

RECEIVER TIMING

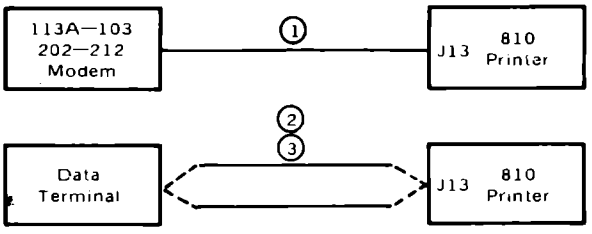


NOTES: 1. This is the point at which the error condition is detected, if error occurs.

2. A high-to-low transition on the DR pin indicates that the contents of the receiver register has been transferred to the receiver buffer register and that the three error-flag signals are valid. Output data remains valid until the next word is transferred into the receiver buffer register.
3. The RI waveform illustrates an eight-bit word with parity and two stop bits. If parity is inhibited, the stop bits immediately follow the last data bit. For all word lengths, the data in the buffer register must be right justified, i.e., RO1 (pin 12) is the least significant bit.
4. Data sampling occurs at the center of each data bit (8 clock cycles after the beginning of the bit).

Appendix H

Cables and Pin Assignments



810 Port Designations:
J13 = EIA Serial

Table H-1. Summary of Cable Options

Item	Part Number	Description	810 Connector Type	No. Wires	Device Connector Type	Length Meters	Length Feet
1	993205-0001	113A/103-202/212 Data Set Cable	25 Pin Male	12	25 Pin Male	1.8	6
2	993210-0001	Data Terminal Cable	25 Pin Male	12	25 Pin Female	1.8	6
3	993239-0001	770 Terminal Cable	25 Pin Male	12	25 Pin Male	1.8	6

Table H-2. 113A/103, 202/212 Data Set Cable (TI Part Number 993205-0001)

810 Pin P6-P7	202/212 Pin	RS-232-C Circuit	Function
1	1	AA	Protective Ground
2	2	BA	Transmitted Data
3	3	BB	Received Data
4	4	CA	Request to Send
5	5	CB	Clear to Send
6	6	CC	Data Set Ready
7	7	AB	Signal Ground
8	8	CF	Received Line Signal Detector
11	11	SCA	Secondary Request to Send (Reverse Channel Transmit)
12	12	SCF	Secondary Received Line Signal Detector (Reverse Channel Receive)
20	20	CD	Data Terminal Ready
22	22	CE	Ring Indicator

Appendix I

US ASCII/Katakana Dual Character Set

This Appendix defines the requirements for and operation of Model 810 printers with dual character set options and, specifically, the US ASCII/Katakana option.

Selection of Character Set
Selection of the normal (US ASCII) or alternate character set is governed by the settings of pencil switches 4 and 5 on the control panel, by the SI (shift-in) and SO (shift-out) control characters, and by the level of bit 8 of the eight-bit code structure. These conditions are summarized in Table I-1 and below.

When pencil switches 4 and 5 are both in the OFF position, parity is not checked and bit 8 is used to select the character set (bit 8 = 0 selects the normal set; bit 8 = 1 selects the alternate set). The control characters SI and SO are ignored.

When pencil switch 4 is OFF and switch 5 is ON, parity is not checked and bit 8 of the eight-bit code is ignored. The control characters SI and SO may be used to select between character sets. If SI was received last, the Model 810 printer uses the normal or US ASCII character set; if SO was received last, the alternate character set is used.

When pencil switch 4 is ON and switch 5 is OFF, bit 8 is considered the parity bit, and each character is checked for even parity. The SI and SO control codes may be used to select normal and alternate character sets, respectively.

When pencil switches 4 and 5 are both in the ON position, each character is checked for odd parity. The SI and SO may be used to select character sets.

Parity Errors
Detection of a parity error results in printing a special symbol whether the normal or alternate character set is used.

Self-Test
The character pattern generated for the self-test is the normal character set if pencil switch 4 is ON and the alternate character set if switch 4 is OFF.

Limitations
The horizontal tab capability is not available in Model 810 printers equipped with the dual character set option. The HT (horizontal tab) and ESC3 (set horizontal tabs) control codes are ignored.

Character Sets

Normal Character Set
The normal character set consists of the standard 64 characters plus the optional 31 printable characters.

Alternate Character Set
The alternate character set consists of the 64 Katakana characters and 31 US ASCII characters.

Special Alternate Character Set
A special Katakana character set is available which substitutes the six characters in Figure I-1 for those elicited by ASCII codes 61 through 66 in the usual Katakana character set.

Table I-1. Parity/Character Set Selection

Switch*					
S4	S5	Bit 8	SI/SO	Parity	Characters
OFF	OFF	0	Ignore	Don't Care	Normal
OFF	OFF	1	Ignore	Don't Care	Alternate
OFF	ON	Ignore	SI	Don't Care	Normal
OFF	ON	Ignore	SO	Don't Care	Alternate
ON	OFF	Parity	SI	Even	Normal
ON	OFF	Parity	SO	Even	Alternate
ON	ON	Parity	SI	OFF	Normal
ON	ON	Parity	SO	Odd	Alternate

*Switches 4 and 5 are located on the control panel.

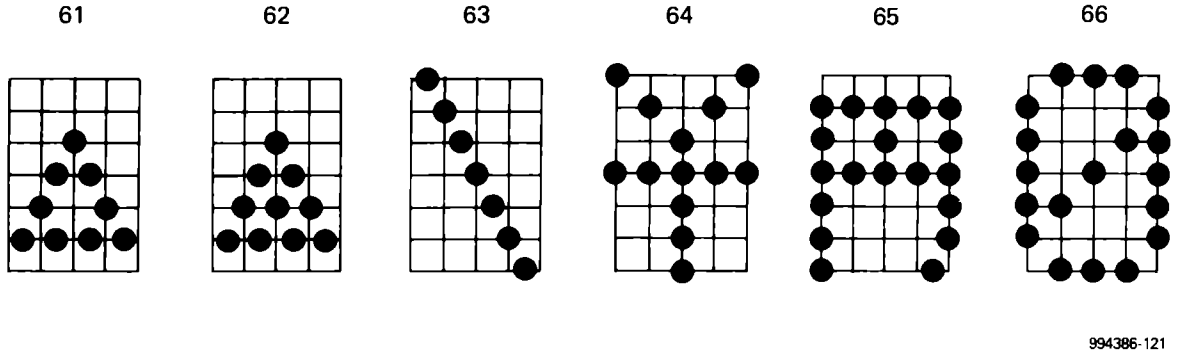


Figure I-1. Special Katakana Character Set (TI Part No. 994434-0016)

Appendix J

Strappable Options for Processor and Line Buffer Boards

Table J-1. Processor PC Board Strappable Options

Function	EIA	PLT	TTY	Position
NDE (No Delete)	X	X	X	E2-E3 (n) Delete E1-E2 No Delete
DNB (Data Terminal Not Busy)	X			E4-E5 (n) DTR = ONLINE E5-E6 DTR = ONLINE and NOT BUSY
IRC (Inverted Reverse Channel)	X			E8-E9 (n) Reverse Channel = BUSY E7-E8 Reverse Channel = BUSY–
DCO (Disable Recognition of DC1 and DC3 Characters)	X	X	X	E17-E18 (n) Enable DC1-DC3 E16-E17 Disable DC1-DC3
LB (Line Buffer Board)	X	X	X	E10-E11 Standard EIA, PLT or TTY E13-E14 Interfaces E11-E12 Line Buffer Option E13-E15 LBE, LBP or LBT Interface
Mandatory Jumper Positions	X	X	X	E25-E26, E28-E29
Unused Jumper Positions (Do Not Connect)	X	X	X	E19, E20, E21, E22, E23, E24

NOTES
"X" indicates that function is selectable for installed option.
(n) indicates position of jumper when assembly is shipped from factory.
A blank space indicates that function does not apply to designated interface.

ADDITIONAL MODIFICATION OPTIONS

To disable the bell, disconnect R99 located on the driver board (TI Part No. 994533)

Table J-2. EIA Line Buffer PC Board (LBE) Strappable Options

Suboption		LBE Revision Level		
		Rev. E and Later	Rev. D	Rev. C and Earlier
DSC	(Decode Carriage Return)	E1-E2 (n) Print on CR[1] E2-E3 Print on CR, LF, FF, VT[1]	E1-E2 (n) Print on CR[1] E2-E3 Print on CR, LF, FF, VT[1]	E1-E2 (n) Print on CR[1] E2-E3 print on CR, LF FF, VT[1]
BRO[2]	(Baud Rate Option)	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504
DNB[3]	(Data Terminal Not Busy)	E8-E9 (n) ONLINE E7-E8 ONLINE and NOT BUSY	E8-E9 (n) ONLINE E7-E8 ONLINE and NOT BUSY	E8-E9 (n) ONLINE E7-E8 ONLINE and NOT BUSY
IRC[3]	(Inverse Reverse Channel)	E10-E11 (n) Reverse Channel = BUSY E11-E12 Reverse Channel = BUSY—	E10-E11 (n) Reverse Channel = BUSY E11-E12 Reverse Channel = BUSY—	E10-E11 (n) Reverse Channel = BUSY E11-E12 Reverse Channel = BUSY—
GDS[4]	(Gated Data Strobe)	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated W20-E21 Data Strobe Gated	W19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated
		E28-E31 (n) EIA Data Ungated	No Jumper (n) EIA Data Data Ungated	
GED	(Dated EIA Data)	E27-E28, E20-E21 } EIA Data Gated	E27-E28, E20-E21 } EIA Data Gated	Suboption Not Available
	Mandatory Position of Other LBE Jumpers	E29-E30 E26-E34	E29-E30	E27-E28 E29-E30

NOTES:

[1]Or 132 characters.

[2]This option must also be configured on the processor board.

[3]These options must be deselected on the processor board.

[4]E20-E21 when GED is selected.

(n) indicates DESELECTED position.

Mandatory positions listed MUST BE SET.

Jumpers E11-E12 and E13-E15 located on the processor board must be strapped for processor boards Rev P and later.

Table J-3. TTY Current Loop Line Buffer PC Board (LBT) Strappable Options

Suboption		Current Loop Board (LBT) Revision Level		
		Rev. E and Later	Rev. D	Rev. C and Earlier
DSC	(Decode Carriage Return)	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]
BRO[2]	(Baud Rate Option)	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504	E4-E5 (n) 5501 E5-E6 5504
GDS[3]	(Gated Data Strobe)	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated
HDP	(Half Duplex Mode)	E29-E30, E32-E33 (n) Full Duplex E13-E14, E20-E21, E25-E26 Half Duplex	E29-E30, E13-E14, E25-E26 (n) Full Duplex E20-E21 Half Duplex	E27-E28, E29-E30 Full (n) Duplex E13-E14, E20-E21, E25-E26 Half Duplex
	Mandatory Position of Other LBT Jumpers	E8-E9 E10-E11 E28-E31	E8-E9 E10-E11	E8-E9 E10-E11

NOTES:
[1]Or 132 characters.
[2]This option must also be configured on the Processor PC board.
[3]E20-E21 when HDP is selected.
(n) indicates DESELECTED position.
Mandatory positions listed MUST BE SET.
Jumpers E11-E12 and E13-E15 located on the processor board must be strapped for processor boards Rev P and later.

Table J-4. Parallel Interface Line Buffer PC Board (LBP) Strappable Options

Suboption		Parallel Board (LBP) Revision Level		
		Rev. E and Later	Rev. D	Rev. C and Earlier
DSC	(Decode Carriage Return)	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]	E1-E2 (n) print on CR[1] E2-E3 print on CR, LF, FF, VT[1]
GDS	(Gated Data Strobe)	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated	E19-E20 (n) Data Strobe Ungated E20-E21 Data Strobe Gated
	Mandatory Position of Other Jumpers on LBP Board	E4-E5 E8-E9 E10-E11 E29-E30 E32-E33 E28-E31	E4-E5 E8-E9 E10-E11 E29-E30	E4-E5 E8-E9 E10-E11 E27-E28 E29-E30

NOTES:
[1]Or 132 characters.
(n) indicates DESELECTED position.
Mandatory positions listed MUST BE SET.
Jumpers E11-E12 and E13-E15 located on the processor board must be strapped for processor boards Rev. P and later.

Appendix K

Theory of Operation for Driver Board (TI Part No. 994322) and Power Supply (TI Part No. 994394)

K.1 INTRODUCTION

This covers the theory of operation for the driver boards which appear in some Model 810 printers. Technicians should inspect the printer to see which driver board is used.

The theory of operation covered in Section 7 provides detailed explanations for the other printer mechanisms.

K.1.2 Driver Board

The driver board (TI Part No. 994322) contains power circuits for driving the printhead, the carriage motor, and the paper feed stepper motor (refer to Figure K-1). All drivers are constant current switching regulators. Power for the carriage driver motor and paper feed motor is derived from the +30 Vdc supply. Power for the printhead solenoids is derived from the −75 Vdc supply.

K.1.2.1 Printhead Driver Circuits. The function of the printhead driver circuits is to provide a current pulse of proper magnitude for the excitation of the seven print wire solenoids. The sequence and duration of the current pulses are defined by the microprocessor, which provides the active low logic level input signals SF1− and SF7− to the printhead circuitry (see Figure K-1).

Each of the seven solenoid drivers can be described as a free running 1.5A current mode switching regulator. Processor board outputs SF1− through SF7− are NORed with the current sensing comparator circuit output, which enables the regulator power circuit to generate the current pulse profile illustrated in Figure K-2. Current flow in the power circuit (relative to the current profile of Figure K-2) is shown in Figure K-3, which illustrates one of the seven printhead drive circuits (all seven circuits are identical). (Refer to logic driver diagram number 994320 in Section 10 for detailed circuit information.) The rising portions of the current profile (section 1 of Figure K-2) occur while Q2 is on (Figure K-3). The solenoid current path is from ground through R11 (A1-A7), the printhead solenoid, through Q2 (A1-A7) and CR2, CR3, CR4 (stage A8) to the −75 Vdc supply. When the voltage across R11 is more negative than VREF (−0.3 V), the comparator (U1) turns Q2 off, and the current decays through R11, CR2 (A1-A7) and Q1 (stage A8) (section 2 of Figure K-2). The hysteresis of the comparator (U1) then allows the current to fall approximately 0.25A before the comparator turns Q2 on again. The circuit oscillates in this mode for the duration of the input pulse. The oscillation frequency is variable over the 24-100 kHz range. When the input pulse returns high, Q2 (A1-A7) and Q1 (A8) turn off, leaving the solenoid clamped to +30 Vdc through supply CR1.

This causes the solenoid current to decay rapidly (section 3 of Figure K-2) and returns the energy stored in the solenoid to the 30 Vdc supply for greater system efficiency.

The 8 SW line is used to derive the base drive from Q2 (stage A1-A7) allowing the power circuit to be enabled or disabled remotely by the Power-Good signal. (Enabling of the 8 SW is described in paragraph K.1.3.4.) CR2, CR3, and CR4 are used to develop the necessary negative bias for turning off Q2 and are common to all seven drivers. CR5 is used to derive the −0.3 V reference for all seven comparators. The printhead driver circuits are logically disabled when either S1 (A8) (located in

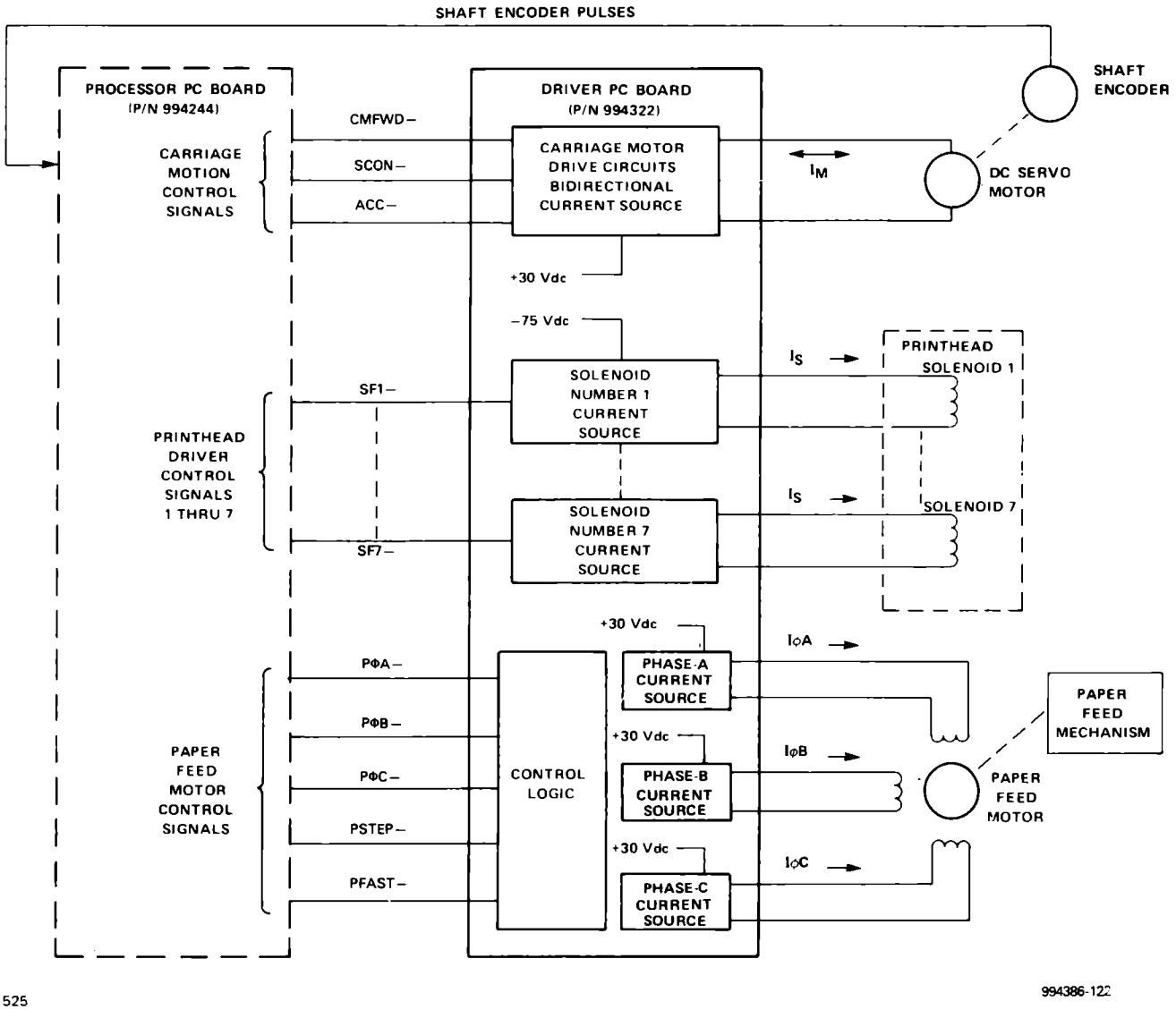


Figure K-1. Driver PC Board Block Diagram

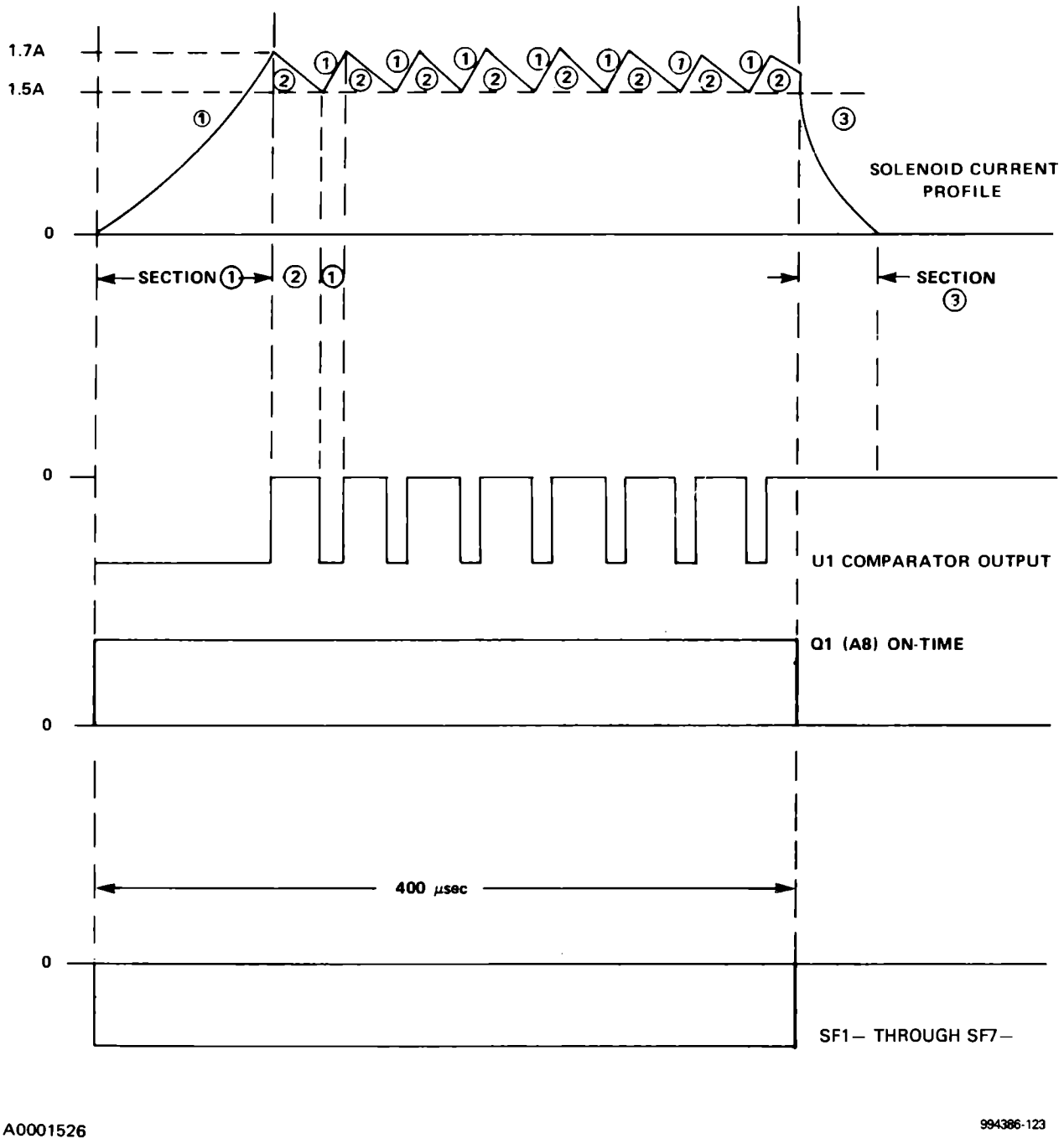


Figure K-2. Printhead Solenoid Current Pulse Profile

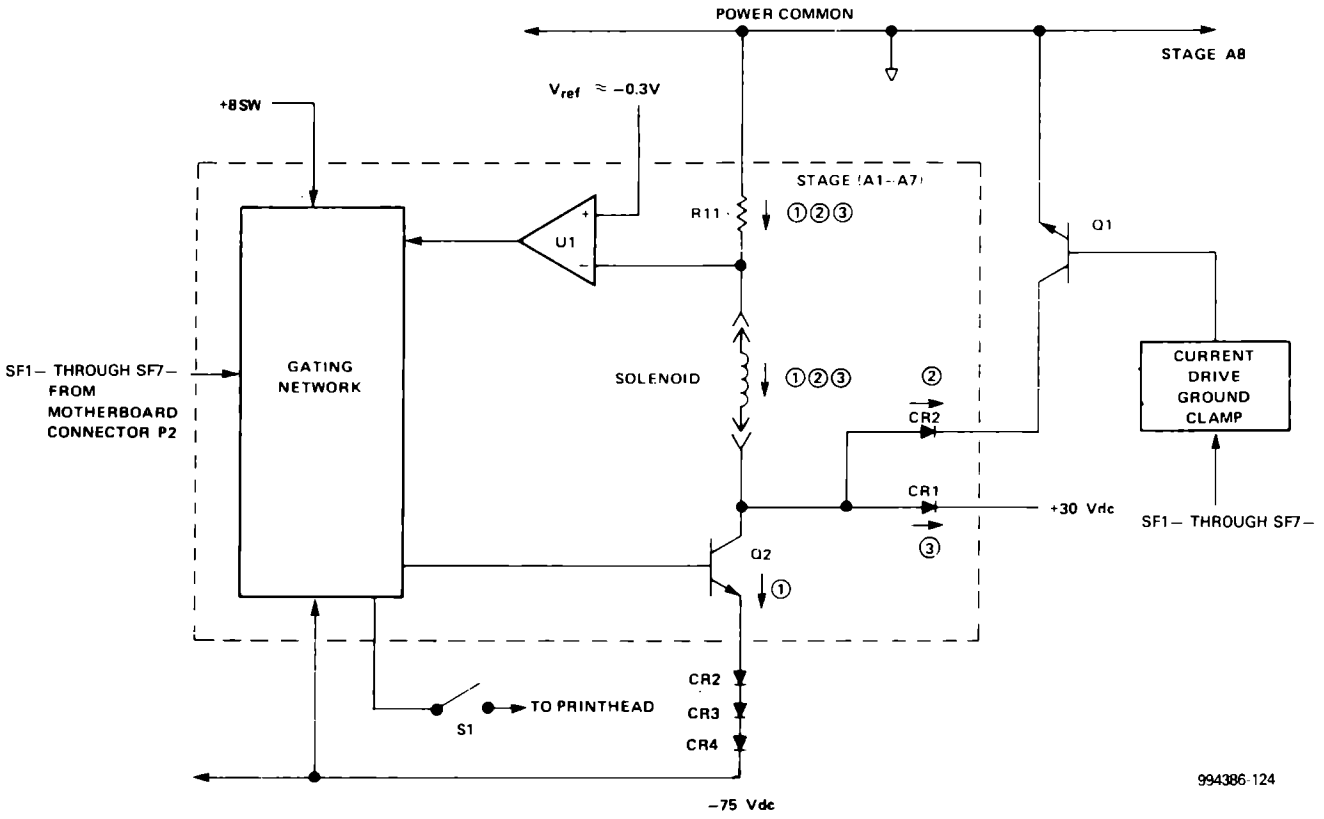


Figure K-3. Printhead Power Driver Simplified Schematic

the upper left area of the driver board) is in the OFF position, and/or when the printhead is disconnected.

K.1.2.2 Carriage Motor Driver Circuit. The carriage motor driver circuit is a bidirectional, two-level, regulated current source. "Bidirectional" describes the ability to reverse the direction of the motor current to drive the carriage in either direction. The high-level current setting is used during periods in which high acceleration or deceleration rates are required; these include starting from rest, accelerating from print speed to slew speed, decelerating from slew to print speeds, or stopping from print speeds. The low current setting is used during the print speed or slew speed regulating mode to minimize velocity variations during these phases of operation. With constant current motor drive, carriage acceleration is constant.

Nominal acceleration values for the two levels of current are:

	Motor Current Amperes	Acceleration In./Sec²	Deceleration In./Sec²
Hi (ACC = 1)	2.85 ± 5%	1000	1500
Lo (ACC = 0)	1.43 ± 5%	500	1000

These acceleration values allow the carriage to reach print speed (15 inches per second) in 15 msec. or slew speed in 35 msec.

The carriage motor drive control signals from the processor board (Figure K-1) are:

CMFWD— An active low on this line sets direction of current flow in the carriage motor to produce forward carriage motion (left to right).

SCON— An active low on this line turns on the motor current.

ACC— An active low on this line sets the motor current to the high acceleration value (2.85A nominal).

The basic circuit of the carriage motor driver is a switching mode current regulator which operates from the unregulated +30 Vdc bus. The main components of this circuit are illustrated in simplified form in Figure K-4. The four power transistors, Q1 through Q4, operate in pairs (Q1, Q4 and Q2, Q3) to establish current flow through the motor in the + to − or − to + direction, respectively. Motor current always flows through the sense resistor R9 in the same direction.

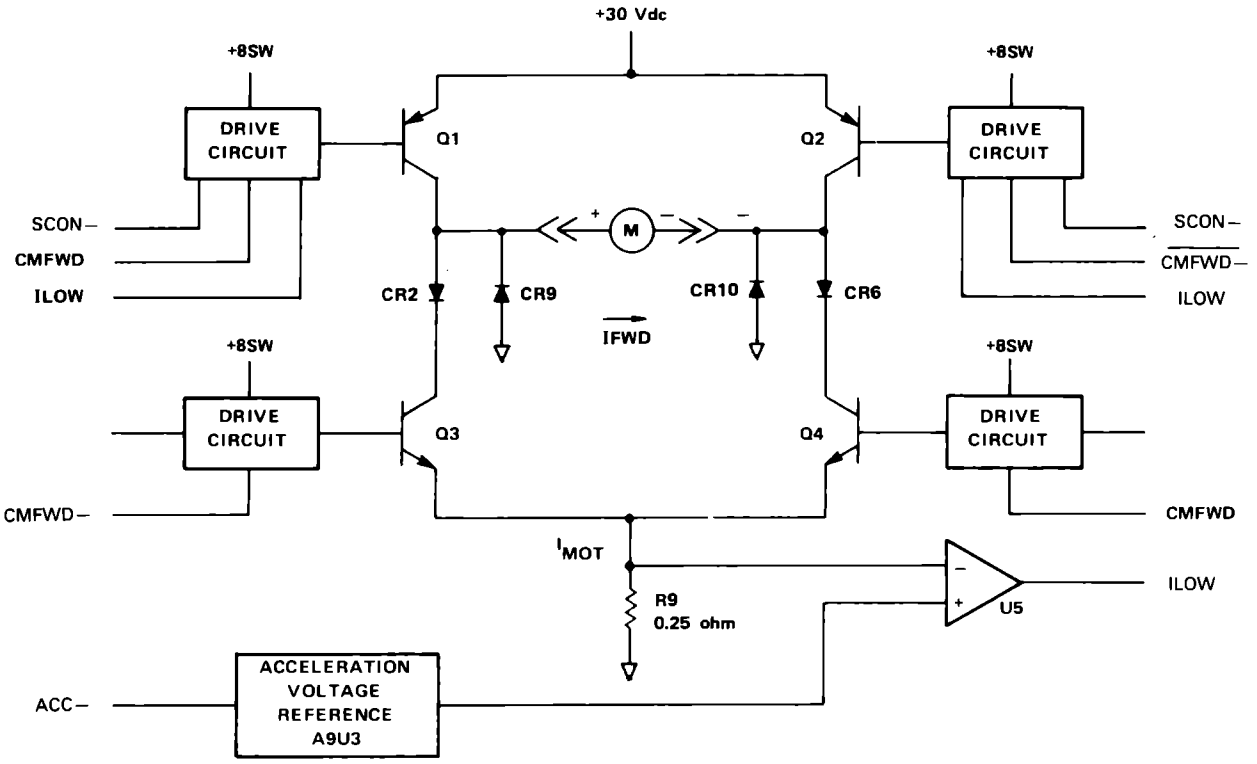


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Figure K-4. Printhead Carriage Driver Simplified Schematic

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Figure K-5 illustrates current flow for a forward command from the processor board. The CMFWD signal is applied through the driver circuits to turn on Q4. Q4 remains on as long as the processor is commanding forward motion. CMFWD prevents Q3, Q2 from conducting. (See Figure K-4.) The operation of the carriage motor circuit can be analyzed using the conduction paths illustrated in Figure K-5 for forward motion. Conduction in transistor Q1 is controlled by three signals: CMFWD, SCON–, and ILOW. CMFWD and SCON– are generated by the process board and are assumed to be true for this part of the circuit analysis. ILOW is a logic level signal generated on the driver board by comparator U5, which compares a voltage drop across R9 to one of two dc reference voltages. The voltage drop across R9 is proportional to the motor current. The dc reference voltage is selected by an FET switch (A9U3) by the ACC– command from the processor board. The output of comparator U5 is at a logic one level if the voltage drop across R9 is less than the selected dc reference voltage. Thus, ILOW is high if the motor current is below the reference selected, or low when the motor current is greater than the reference. Assuming the processor has selected forward motion by setting CMFWD and SCON– true, ILOW will determine if Q1 is conducting. When Q1 is turned on, current I_1 (Figure K-5) exponentially increases towards a target value set by the unregulated supply voltage, the back emf generated by the motor, and the circuit resistance. The time constant of this exponential rise is set by the motor inductance and the circuit resistance. Figure K-6 illustrates a typical motor current waveform from turn-on through the first few regulating cycles. When the motor current reaches the comparator upper trip point, ILOW goes low, turning Q1 off. The current path shown as I_1, therefore, is interrupted. Motor current cannot change instantaneously, however, due to the motor inductance. The collapsing magnetic field in the motor tries to maintain the motor current. Figure K-5 illustrates this current path (I_2).

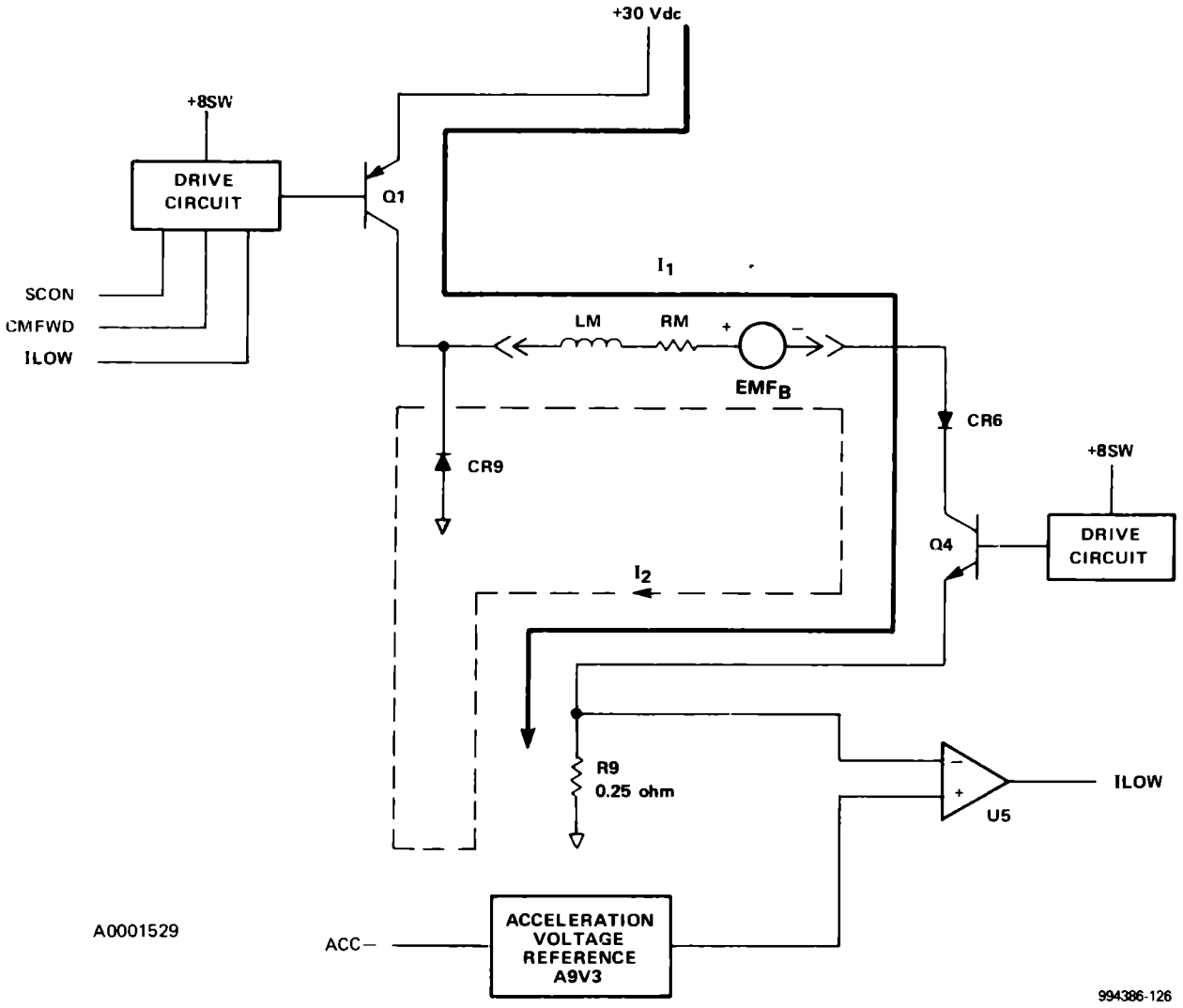


Figure K-5. Printhead Carriage Driver Circuit Forward Command

Figure K-6 illustrates the exponential decay of motor current I_2. The motor inductance and circuit resistance determine the time constant or decay rate for the motor current.

The comparator circuit has a designed-in hysteresis which causes the lower trip point to be approximately 150 mA lower than the upper trip point. When 12 decays to this lower trip point, ILOW goes high again (Figure K-5). This action turns Q1 on again and current is established again along current path I_1. Q1 is turned on and off at a frequency determined by the current rise (I_1) and fall times (I_2) and the amount of comparator hysteresis. The nominal frequency is 10 kHz, although this value can vary widely with variations in motors and the +30 Vdc unregulated supply voltage. As long as SCON− and CMFWD remain true, this switching action continues and produces a constant average current in the motor windings. This average motor current is between the upper and lower comparator trip points as shown in Figure K-6. Average motor current is also determined by the dc reference voltage applied to the comparator positive input terminal. When ACC is true, the average motor current is 2.86A (nominal). When ACC− is false, the average motor current is 1.43A (nominal).

Bidirectional printhead drive capability is achieved by reversing the current flow in the motor. The processor changes the circuit configuration by changing CMFWD from true to false (refer to Figure K-4). In the reverse direction, Q1 and Q4 are turned off, Q2 and Q3 are turned on. Current regulation in the reverse direction is similar to the forward current cycle except that the current flows through Q2, Q3, CR2, R9, and CR10.

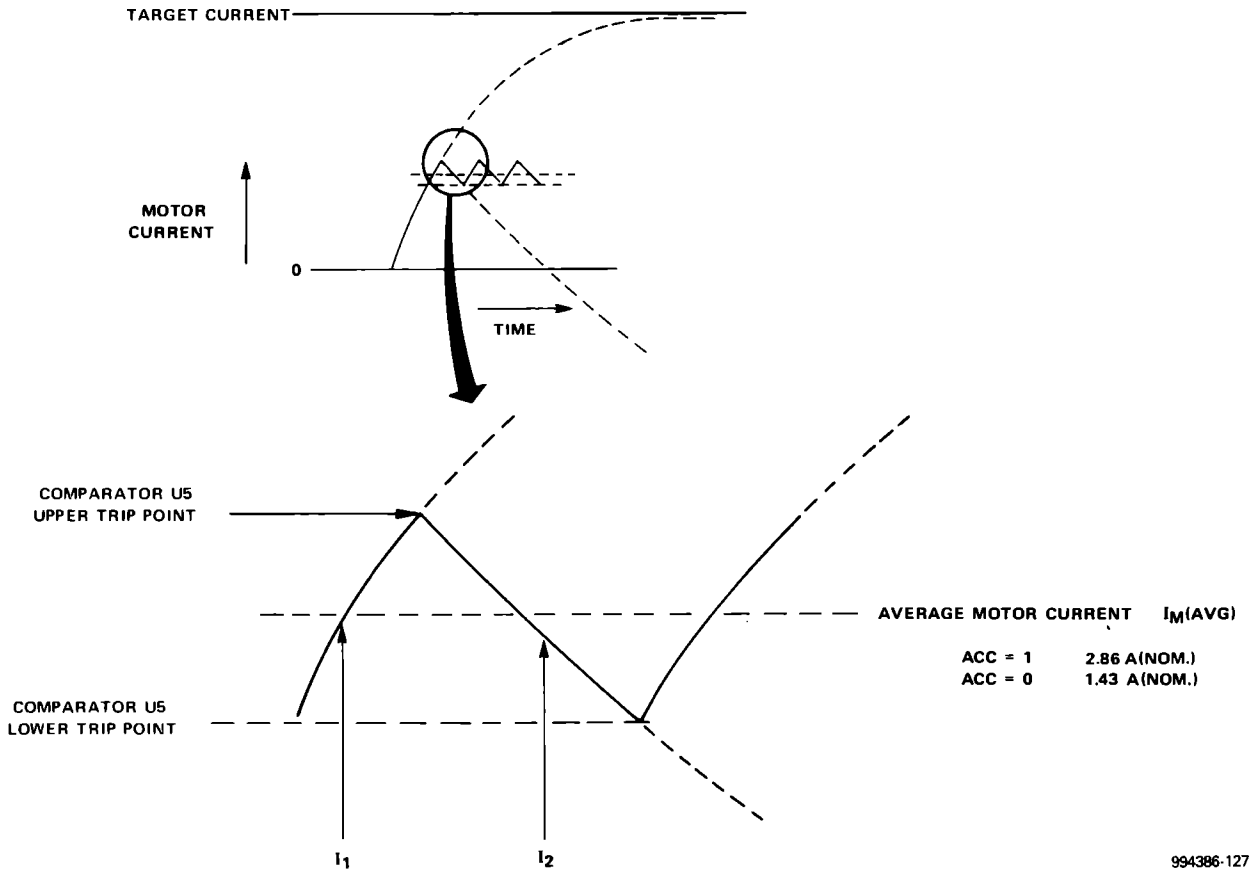


Figure K-6. Printhead Carriage Motor Current Waveforms

When ACC is true, the average motor current is 2.86A (nominal). When ACC– is false, the average motor current is 1.43A (nominal).

Refer to Logic Driver (diagram number 994320, sheet 2, Section 10) for a detailed schematic of the carriage motor power circuits. The basic circuit components are Q1 through Q4, CR9, CR10, and U5. Transistors Q5, Q6, and U1 form the drive circuit and logic functions for Q1. Transistors Q7, Q8 and section 2 of U1 form the drive and logic functions for Q2.

Q3 and Q4 are high gain Darlington power transistors requiring minimal base drive current through R16 and R32, respectively. Diodes CR2 and CR6 prevent inverted mode operation of Q3 and Q4 during the motor current decay phase (I_2, Figure K-6).

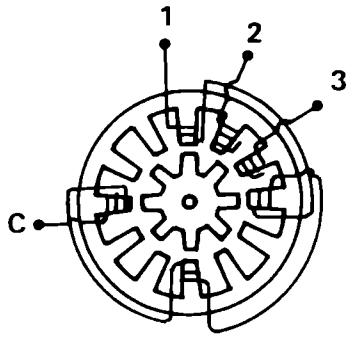
CR1 is a one percent, 5.1V zener reference which is used to set the 2.86A current level for high acceleration. This same 5.1V reference source is divided down by R22 and R23 to set the 1.43A reference for U5. U3 is a quad FET switch used to select the required reference. The reference voltage set by CR1 is also used by the paper feed motor drive circuit.

U5 is an inverting comparator with the hysteresis level set by the 425 k ohm feedback resistor R12. Resistor R40 and CR5 bias the output stage of U5 to 0.6V below ground to provide additional noise margins when coupling to TTL circuits grounded on the Motherboard.

The +8 SW supply voltage controls base drive to Q3 and Q4 directly and to Q1 and Q2 indirectly. Thus, the +8 SW supply forms a positive motor drive inhibit function independent of logic supplies. This prevents application of power to the carriage motor during power-up sequences or marginal power conditions since the +8 SW is only turned on when Power-Good is true. (See paragraph K.1.3.8 for a Power-Good circuit description.)

K.1.2.3 Paper Feed Motor Driver Circuits. The stepper motor driver circuit provides driving current to the three-phase variable reluctance (VR) stepper motor, based on commands from the microprocessor. Logic signals from the microprocessor control the sequence, direction, and magnitude of current through each of the three windings in the stepper motor as needed to start, brake, and reverse the motion of the paper (forms). Paper direction is controlled by pulsing the stepper motor A, B, and C windings in the proper order (A, B, C; A, B, C ... etc. for forward; or C, B, A; C, B, A ... etc. for reverse).

The VR stepper motor stator consists of various wire-wound poles (Figure K-7). The rotor consists of a cylindrical, toothed member. The number of teeth determines the step angle required (15° for the Model 810 printer). When current flows through the selected set of motor windings, a torque is developed to rotate the rotor to a position of minimum path reluctance.



15° VR Stepper (3-phase), complete winding shown for one phase only. 994386-47

Figure K-7. Variable Reluctance, Paper Feed Stepper Motor

This position is statically stable; i.e., external torque is required to move the rotor from its present position. This position is not an "absolute" position since there are many stable positions of the motor.

When a different set of windings is energized, the minimum reluctance occurs at a different set of poles and rotor teeth, causing the rotor to move to a new position. These stable positions can be made to rotate smoothly around the stator poles by energizing selected sets of windings. This action produces rotational speed and torque which is coupled to the paper driver tractors through a 7.5-to-1 gear set. When the phase rotation sequence stops, the rotor position becomes fixed. The rotor has a "detent" torque due to the holding current which locks the tractors and paper into position for printing.

When the energizing sequence is stopped, the rotor continues to move because of motor and load inertias. The motor overshoots until sufficient reverse torque is developed to pull the rotor back to the detent position. Special timing is used in the drive sequence to minimize overshoot when the motor is stopped.

The stepper motor drive circuits form a switching mode, constant current regulator, which operates from the unregulated +30 Vdc bus. Figure K-8 illustrates the major component parts of the switching regulator drive current for all three motor phases. The switching action (which regulates the current in a selected phase) can be analyzed using the simplified single phase schematic illustrated in Figure K-9.

The PNP transistor labeled Q2/Q3 is a quasi-PNP circuit formed from an NPN output stage and a PNP driver. Q2/Q3 is turned on by a combination of signal PØA from the processor board and the output of comparator U3.

The stepper motor is operated in two modes, hold and stepping. In the hold mode the stepper is not moving but is providing a detenting torque to prevent paper movement while printing. In the stepping mode, the motor moves the paper 0.014 inch for each 15° step the motor is advanced.

The power circuits are controlled by the processor board through the following logic signals:

PØA—
PØB—
PØC— An active low on one of these signal lines determines which of the three motor phases will be energized. One phase is energized at all times (the signals are exclusive).

PSTEP— An active low on this line will set the motor phase current to 3.0A nominal. A high level sets the motor phase current to 1.0A.

PFAST— An active low on this line will change the time constant of the current decay circuits from slow to fast.

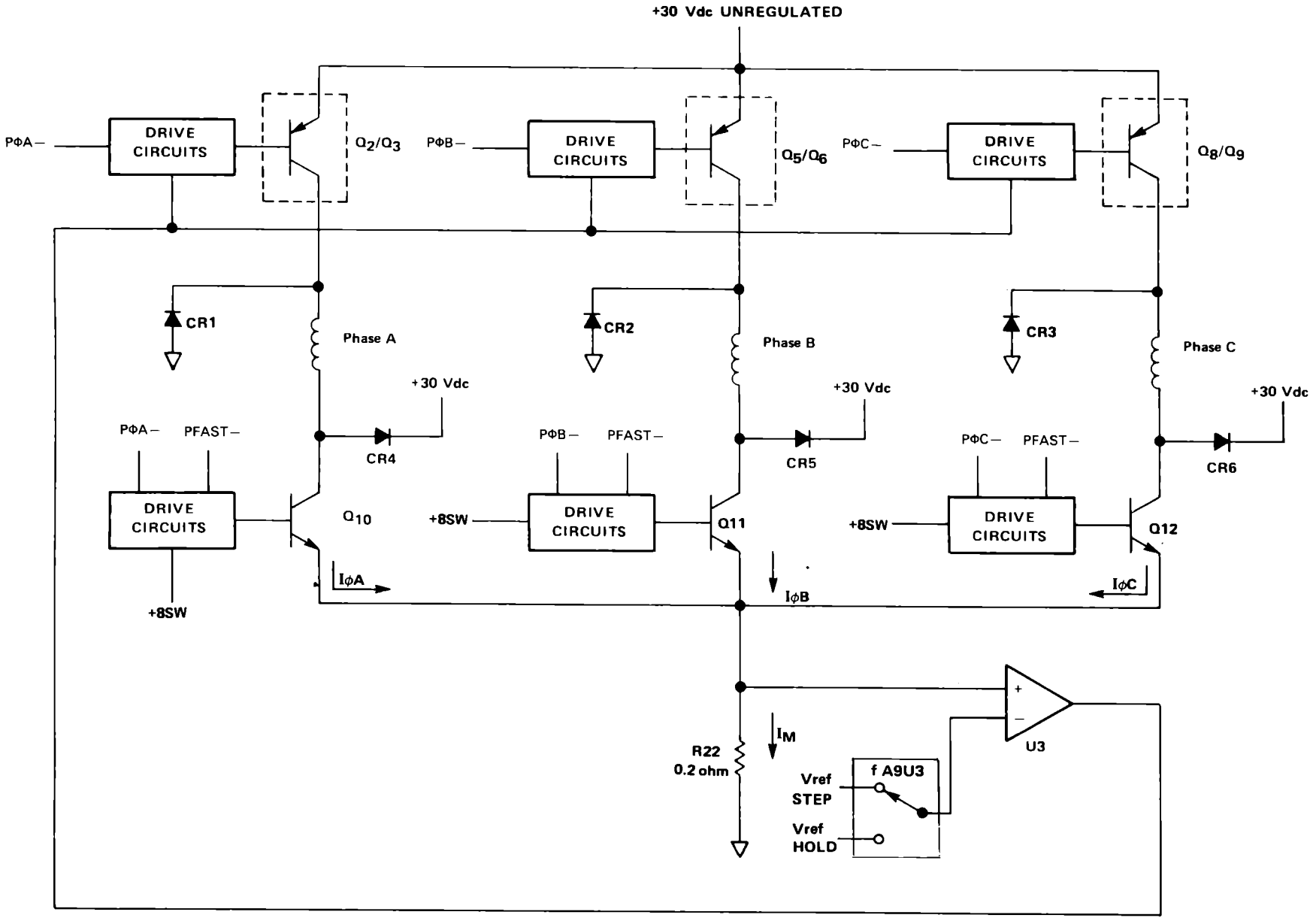


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Figure K-8. Stepper Motor Drive Circuit, Simplified Diagram

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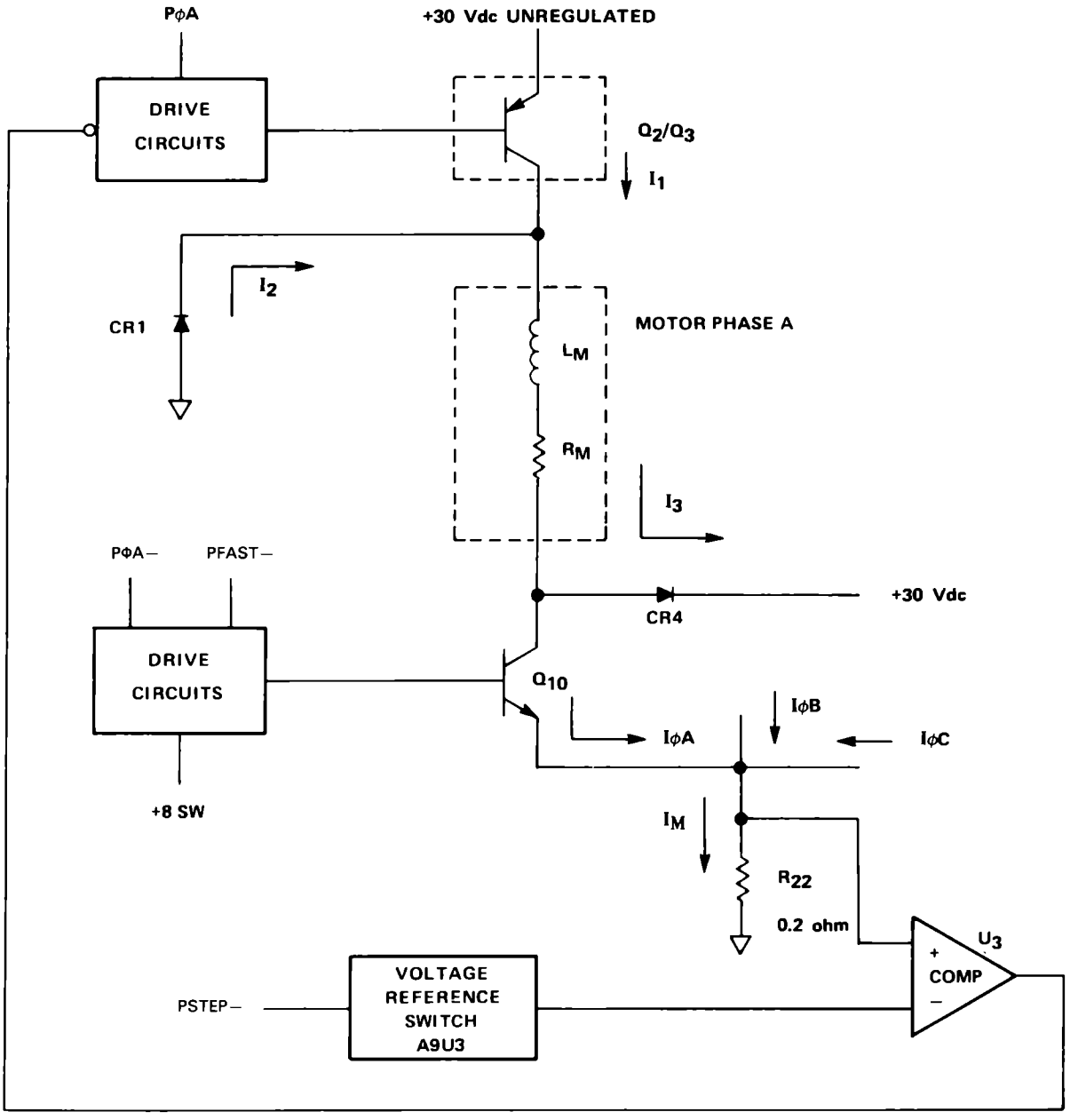


Figure K-9. Stepper Motor Drive Circuit, Phase A

1. *Hold Mode Operation.* The hold mode energizes the selected phase of the stepper motor with a low level (1.0A) constant current which is used to provide a detent or holding torque. Since the hold mode involves only one phase, it is the most straightforward mode to analyze. The processor board selects the hold mode voltage reference and applies it to the inverting terminal of U3 (refer to Figure K-9). The comparator U3 output is at a logic low for motor current (I_M) less than the reference current. The PFAST command from the processor board changes the time constant of the motor current decay circuit. In the normal regulating mode, this command is false. Starting with zero motor current and PΦA— true,

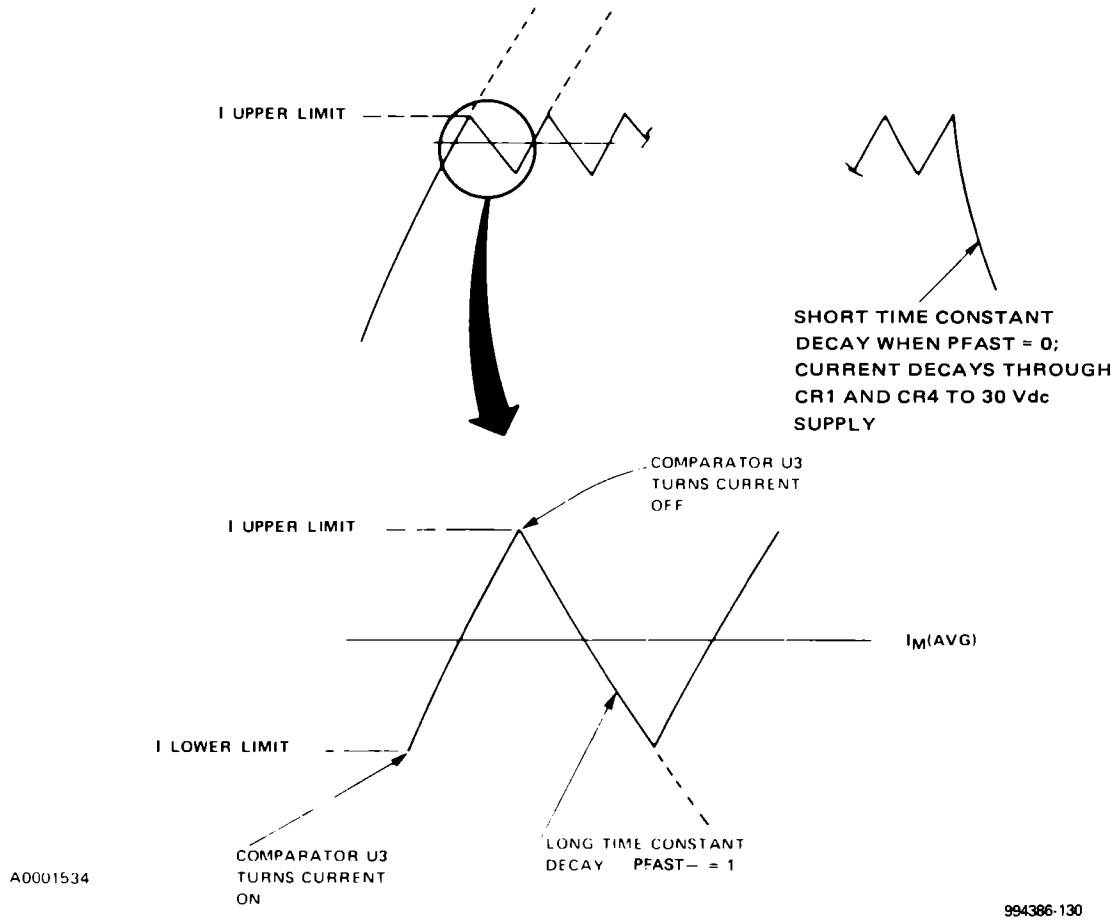


Figure K-10. Stepper Motor Circuit Waveforms

transistor switches Q2/Q3 and Q10 are turned on. Motor current I_1 starts to rise at a rate set by the supply voltage and the circuit time constant determined by the motor inductance and resistance. At this instant I_1, IØA, and I_M (see Figure K-9) represent the motor phase current. The motor current continues to increase towards a target value set by the supply voltage and circuit resistance. Figure K-10 illustrates the switching waveforms. When the current reaches the upper comparator limit, the voltage drops across R22 equal the hold current reference voltage and comparator U3 switches to a high state. This, in turn, switches off transistor Q2/Q3.

Since the motor is inductive, motor current cannot change instantly (see Figure K-9). The path for the decay current is through Q10 (IØA), R22 (I_M) and CR1 (I_2). The time constant for this decay path is determined by the motor and circuit resistances and is relatively long. The current continues to decay until the lower current limit is reached. The lower limit is set by the hold current reference voltage and the comparator (U3) hysteresis. At the lower limit, Q2/Q3 are turned on again and the switching cycle is repeated. The holding current is the average of the switched current waveform.

2. *Stepping Mode Operation.* The regulation action of the stepper motor driver circuit is similar to the analysis presented for the hold current mode. However, there are exceptions.

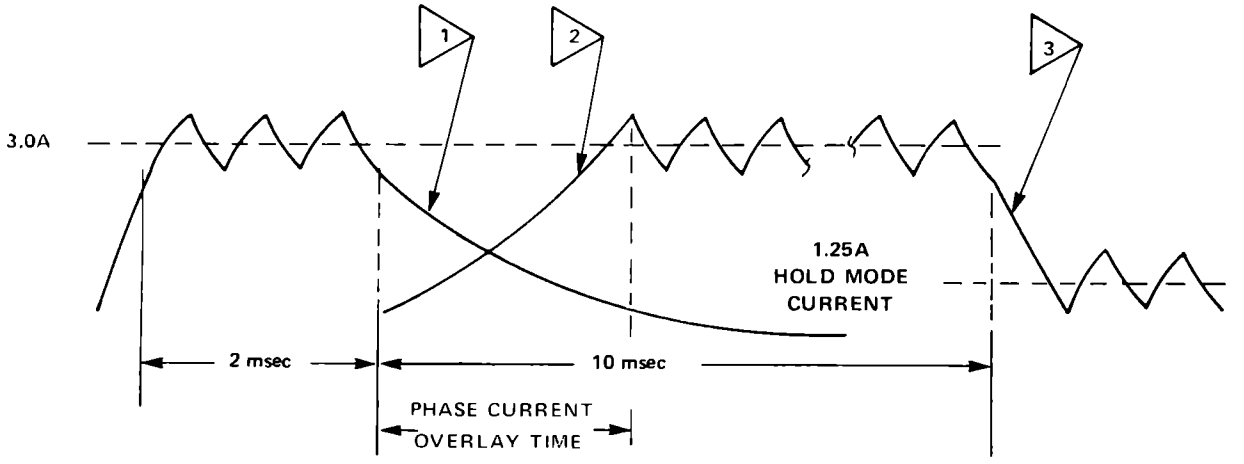
   - Magnitude: The average current level is maintained at a 3.0A (nominal) level by the PSTEP– command.

- End-of-step time delay: When switching current from one phase to another during the stepping mode, a decrease in the time constant is required for the current decay in the phase being turned off. This is accomplished by turning off Q10 with the PFAST— signal from the processor. The decay current then flows through diode CR4 and CR1 as shown by I_3 and I_2 in Figure K-9. The energy stored in the magnetic field of the motor windings is returned to the +30 volt supply, and the current decays very rapidly as illustrated in Figure K-10.

3. *Motor Braking Mode.* Referring again to Figure K-8, note that the three phase currents IØA, IØB, and IØC are summed to form the total motor current I_M. Therefore, when viewed as a complete driver circuit, the total regulated current is 3A in the stepping mode. This summing effect is important during the overlap time between the decay current in the preceding phase and the buildup of current in the phase being turned on.

Figure K-11 illustrates the current distribution in the stepper motor when making a transition to the last or detent phase. Normal stepping time, or the time each phase is energized in the stepping mode, is 2 msec. At the end of each step the time constant is changed to fast (PFAST— = 0), which causes a rapid decay of phase current. At t_{12} (Figure K-11) the normal sequence is changed to leave the decay time constant in the slow mode (PFAST— = 1). The phase signals are advanced as in a normal step. The slowly decaying current (note 1, Figure K-11) retards the normally fast current buildup of the next phase (note 2, Figure K-11). This is necessary since the sum of the phase currents must be equal to the programmed motor current.

The mechanical position of the rotor at time t_{12} is leading the energized winding. The slow decay of current, therefore, becomes a retarding force. In addition slow buildup of current in the detent windings provides only a relatively weak accelerating force on the rotor. The net effect is to slow the rotor just prior to detenting to the final position. This action minimizes the overshoot of the rotor and brings the paper advance mechanism to a smooth stop.



1 SLOW DECAY OF CURRENT IN NEXT TO LAST PHASE; PFAST— = 1, PSTEP— = 0 (t_{12})

2 SLOW BUILDUP OF CURRENT IN THE LAST PHASE (DETENT POSITION)

3 CHANGE FROM 3.0 AMP STEPPING CURRENT TO 1.25 AMP HOLDING CURRENT.

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Figure K-11. Paper Feed Stepper Motor Currents

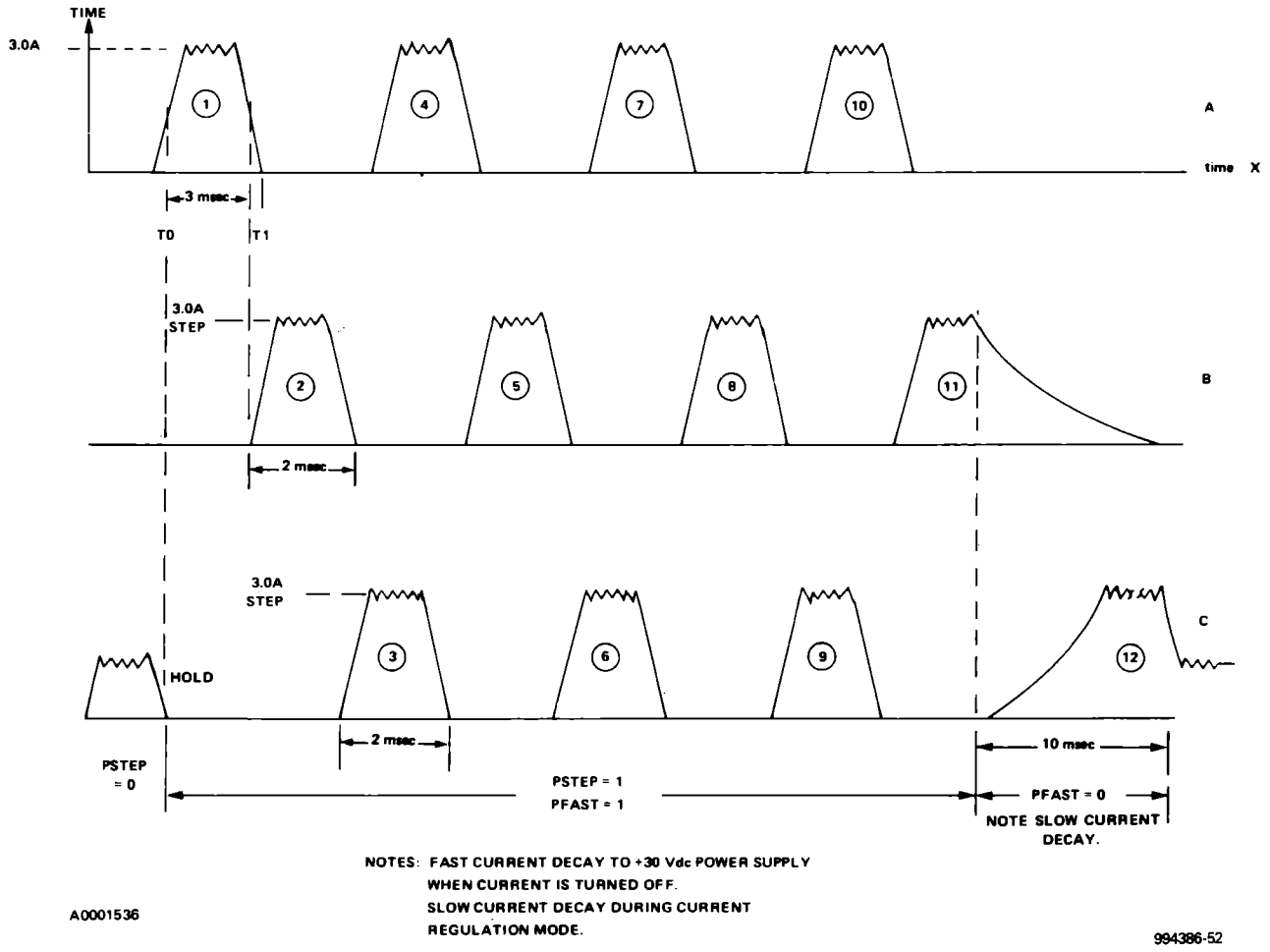

Figure K-12. Stepper Motor Line Feed Cycle

4. *Line Feed Cycle.* Figure K-12 illustrates the current waveforms in the phase A, B, and C windings of the motor for a complete 12-step line feed. The diagram assumes the motor is in the hold mode with phase C energized at the start of the sequence.

K.1.3 Power Supply

The power supply consists of the ac power module and the power supply board (which plugs into the Motherboard). The power supply provides the necessary voltage and current requirements for all Model 810 printer operations. It also generates Power-Good (PWRGOOD) and Reset (RST) signals for initializing the microprocessor system when power is turned on. Figure K-13 provides a detailed block diagram of the power supply. (The sheet numbers listed on Figure K-13 refer to drawing number 994392 in Section 10 of this manual.)

K.1.3.1 AC Power Module. As shown in Figure K-13, the ac power module (Part No. 994461) consists of an EMI filter, an **ON/OFF** power switch, line fuse, power transformer, a bridge rectifier, and a power input selection mechanism which allows selection of four primary line voltages: 100, 120, 220, or 240 Vac. The power supply module produces 75 Vac, 40 Vac (center tapped to produce two 20-Vac lines), 30 Vdc unfiltered, and 29 Vac to operate the inked ribbon drive and the cooling fan.

Line voltage selection (described in Section 2, paragraph 2.4.1) is accomplished by changing the orientation of a small printed circuit board at the rear of the printer which rearranges the power transformer primary taps. The primary taps ar-

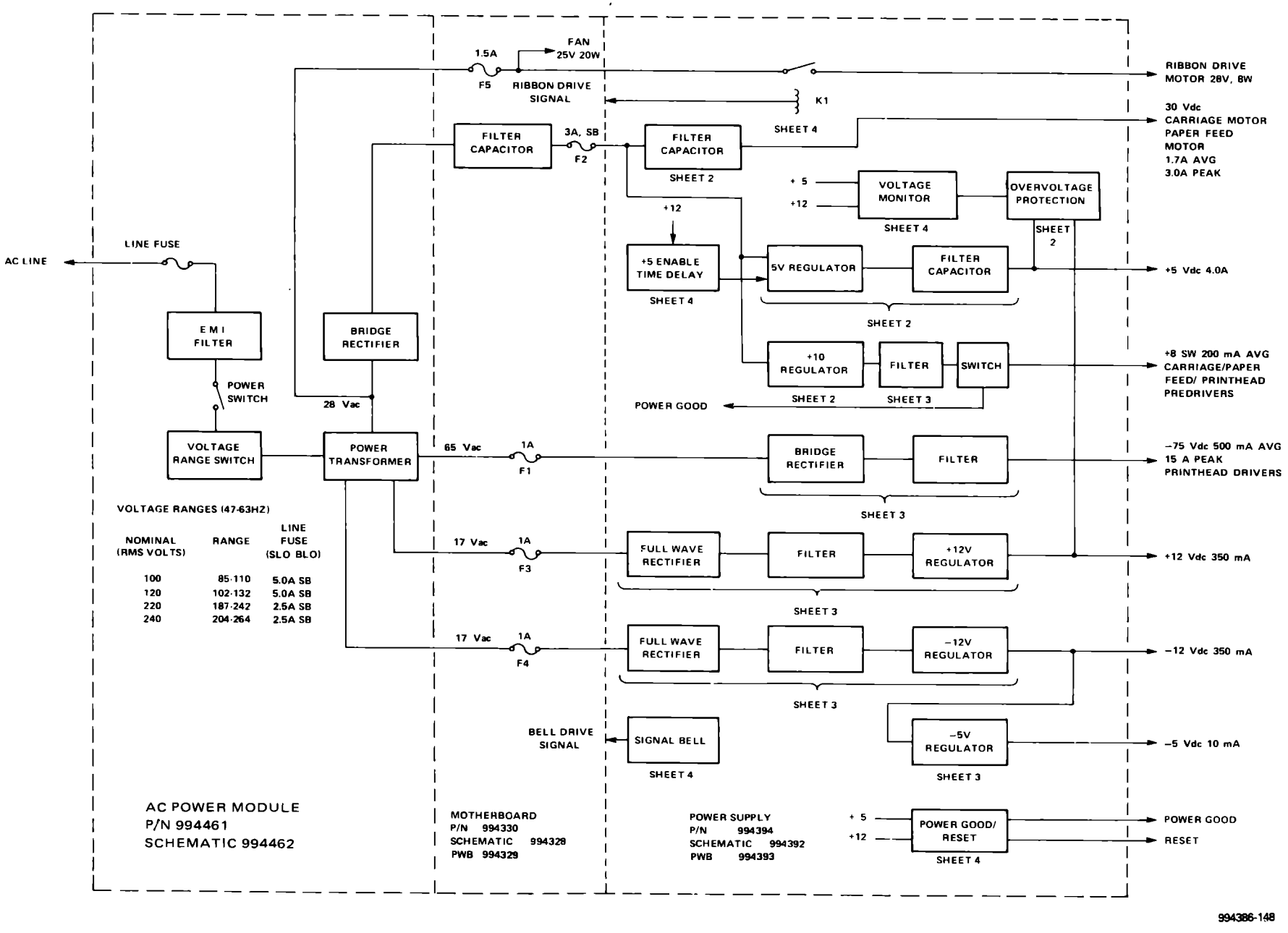

Figure K-13. Power Supply Functional Block Diagram

rangements are illustrated in Figure K-14. Refer to drawing number 994462 in Section 10 for a detailed schematic of the ac power module.

The EMI filter prevents printer switching regulator noise from being conducted into the ac power line. The ac line (primary side of power transformer) is fused with either a 2.5A or 5.0A fuse, depending on line voltage selection (refer to paragraph 2.4.1 for line voltage selection). A 5.0A fuse is required for 100 or 120 Vac selection (Figure K-13) and a 2.5A fuse is required for 220 to 240 Vac selection. The secondary side of the power transformer is fused with five fuses located on the Motherboard. Refer to drawing number 994392, sheet 1, in Section 10 for location of these fuses in the power supply circuits.

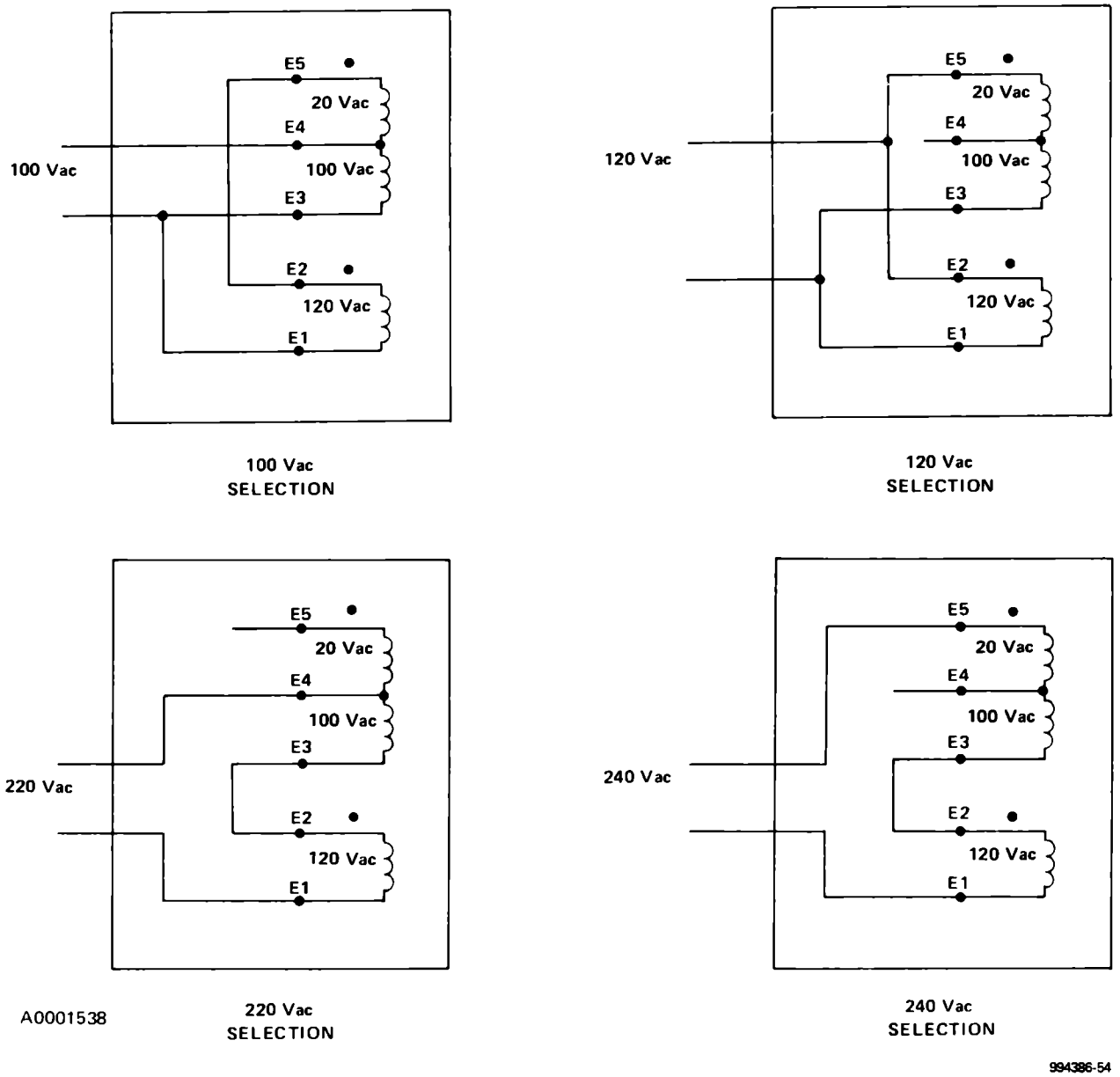

Figure K-14. Power Transformer Primary Tap Arrangements

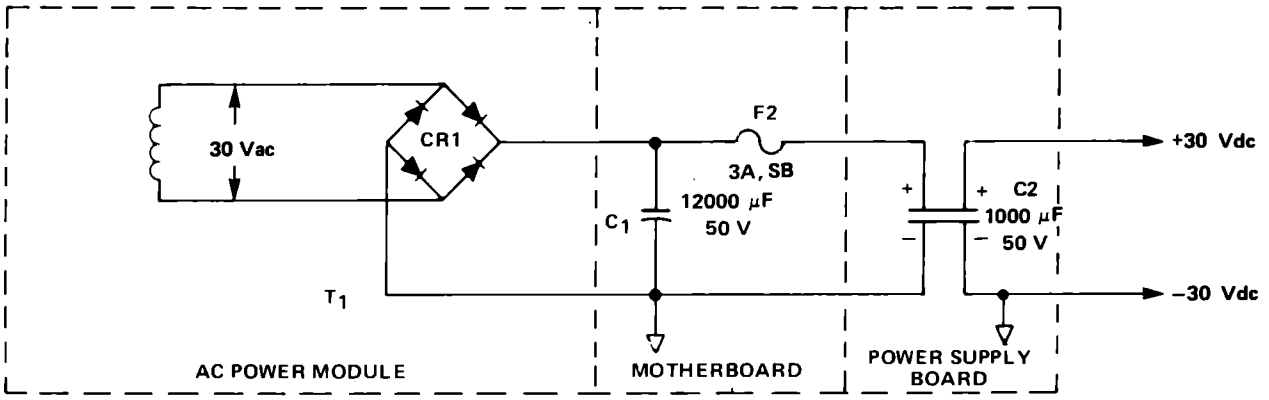

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Figure K-15. 30 Vdc Supply

994386-55

K.1.3.2 +30 Vdc Supply. The +30 Vdc supply consists of a transformer, bridge rectifier, and filter capacitor configuration as illustrated in Figure K-15.

The transformer and bridge rectifier are contained in the ac module. Filter capacitor C1 is located on the Motherboard and filter capacitor C2 is located on the power supply board. C1 is a low frequency electrolytic capacitor which filters the raw dc voltage from the ac module; and C2 is a high frequency electrolytic capacitor used to decouple the high frequency load imposed by the numerous switching regulators in the printer.

The +30V line supplies power for the carriage motor, paper feed motor, +4 Vdc regulator, and the +8 SW regulator (Figure K-13).

K.1.3.3 +5 Vdc Regulator. The +5 Vdc regulator, located on the power supply board (Figure K-13), supplies power for all processor, driver board, and option board circuits. The +5V regulator can be defined as a constant ΔI voltage switching regulator. The basic configuration of the circuit is illustrated in Figure K-16. The +30 Vdc supply provides input power for the +5 Vdc regulator.

The +5 Vdc regulator output is maintained at +5 ±0.10 Vdc with a load current from 0.5 to 4.0A. The output is regulated by the power switch Q4 duty cycle and the control circuitry (which monitors the ac and dc voltage across R10 and the 5 Vdc output voltage). L1, C7, C8, and C9 are the energy storage elements of the regulator. CR4 serves as a commutating diode during the off time of Q4. The enable circuit provides a means of enabling or disabling the entire regulator (i.e., when +5 ENA is high, the regulator is turned on).

Refer to drawing number 994392, sheet 2, in Section 10 for the following discussion of the +5 Vdc regulator operation.

Transistors Q3 and Q4 form a power switch which is turned on or off by the circuit which controls transistor Q2. Q2 acts as a voltage isolating element to prevent the +30 Vdc on the base of Q3 from increasing the driving point (pin 2 of AR1) more than 0.6V above the AR1 supply voltage (derived from CR39). Transistor Q1 enables the 24 mA constant current source which supplies current to CR39 and AR1. A voltage proportional to the ripple current in R10 is fed back to AR1 through C4 and C6. This voltage defines the filter

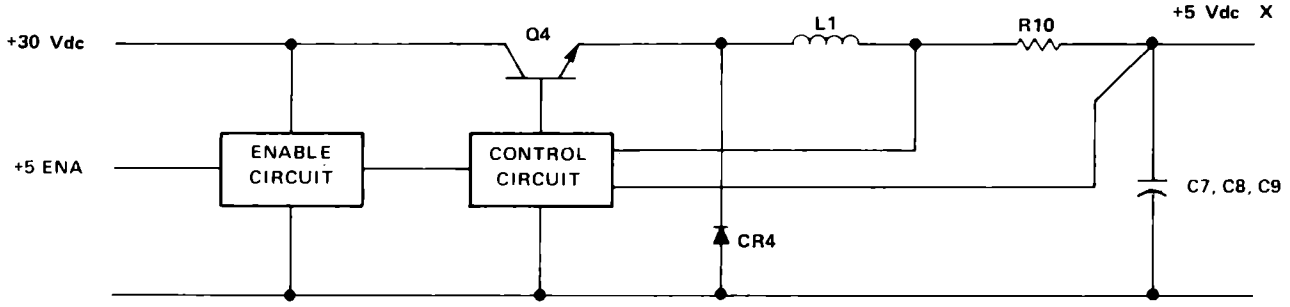

Figure K-16. +5 Vdc Regulator

994386-56

capacitor ripple current and, thereby, the ripple voltage at the output. The dc output voltage is remotely sensed as indicated, and the voltage at pin 2 or R13 is compared to an internal reference in AR1 to produce the desired output. Adjustment of R13 will vary the output dc level from 4.2 Vdc to 5.5 Vdc. If the regulator output is overloaded, Q6 senses an overvoltage across R10 and increases the off time of Q4 to current limit the regulator at 5A. This lowers the frequency of operation from 25 kHz to 8 kHz which produces an audible indication that the regulator is overloaded or shorted.

K.1.3.4 +8 SW. Refer to Figure K-13. The +8 SW line is required to enable the power circuitry on the driver board after the +12V and +5V regulators in the power supply exceed their respective minimum values for proper machine operation (see paragraph K.1.3.8, Power-Good/Reset circuit description). This prevents carriage and paper motion and/or printing to occur during the power-up and power-down sequence of the machine. Basic implementation of the circuit is illustrated in Figure K-17. The +8 Vdc output is derived from the +30 Vdc line. The reference voltage for the regulator is derived from the +12 monitor line. This regulated voltage is then communicated to the load through power switch 1 which is turned on or off by the PWRGOOD signal.

Refer to drawing number 994392, sheets 2 and 3 in Section 10 for the following detailed discussion of the +8 SW circuit.

Diode CR7 is a programmable shunt regulator which provides a constant emitter voltage (10.45 V) on transistor Q9 (Darlington), thereby producing the regulated output voltage. Transistor Q10 is used as a current limiter by sensing the voltage across R28. As the voltage across R28 exceeds ≈ .6V, Q10 turns on and sinks a portion of the base drive for Q9, causing it to turn off, limiting the output current to ≈ .3A. This regulated voltage is connected to the load through the power switch comprised of transistor Q8 (Darlington) and its driver transistor Q7. Q7 is turned on when the Power-Good line goes high. CR41 and CR42 ensure that Q7 is off when Power-Good is low. The collector-emitter drop across Q8 lowers the output to approximately +8 Vdc.

K.1.3.5 ±12 Vdc and −5 Vdc Regulators. The ±12 Vdc regulators are two 3-terminal regulators. The −5 Vdc output is regulated by zener diode CR16 from the −12 Vdc bus. Figure K-18 illustrates ±12 Vdc and −5 Vdc regulator configuration. The input to the ±12 Vdc regulators is from a conventional center-tapped transformer, bridge rectifier, and capacitor configuration.

The +12 Vdc output supplies the MOS device on the processor board and the various comparators on the driver board. The −12 Vdc line supplies comparators on the driver board and MOS circuit devices on the processor board. The −5 Vdc line is used as a substrate bias for the 8080A microprocessor.

K.1.3.6 −75 Vdc Supply. The −75 Vdc source is derived from a conventional transformer, bridge rectifier, and capacitor configuration as illustrated in Figure K-19.

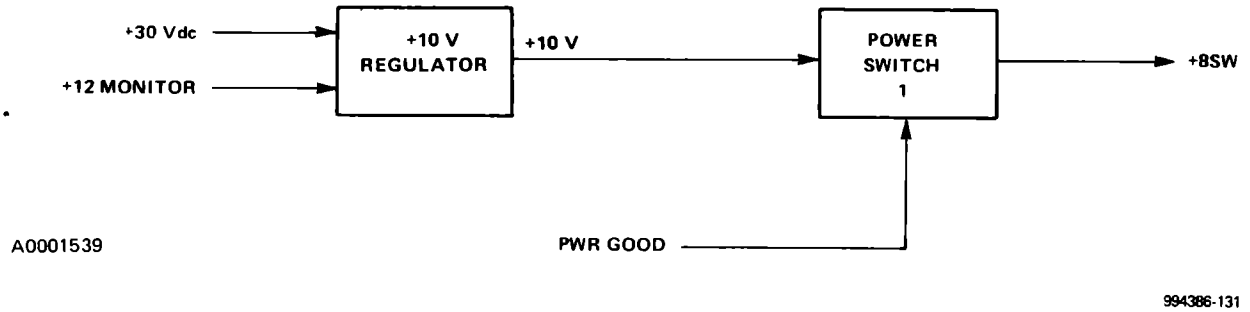

Figure K-17. +8 SW Line

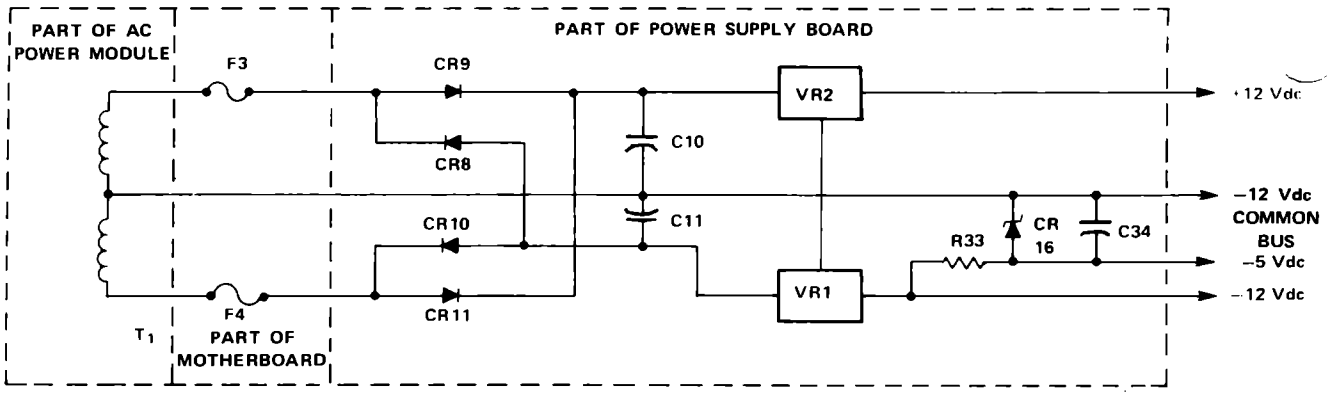

Figure K-18. ±12 Vdc and −5 Vdc Regulators

The −75 Vdc supply is only used for supplying power to the printhead driver circuits. This high potential is necessary to produce fast rising current pulses in the printhead solenoids.

K.1.3.7 Overvoltage Protection Circuit. The overvoltage protection (OVP) circuit is used to disable the printer, under a condition of overvoltage on the +5 Vdc or +12 Vdc line. The circuit operates in two modes, destructive and nondestructive. In the destructive mode, the OVP should fire as a result of an actual power supply malfunction when the +5 Vdc and/or +12 Vdc regulator exceed their preset upper voltage limit. In this mode, the +30 Vdc and/or the +20 Vdc fuses will blow and disable the printer. In the nondestructive mode, the OVP will fire under conditions of overvoltage on the +5 Vdc or +12 Vdc as a result of other malfunctions not associated with the power supply. In this mode the +12 Vdc and +5 Vdc power supply outputs are grounded through SCR1. Both the +12 Vdc and +5 Vdc supplies immediately go into current limit. With the +12 Vdc output at ground, the +5 Vdc regulator operating in dissipation limit until power is recycled.

Refer to drawing number 994392, sheets 2 and 4, in Section 10 (sheet 4 illustrates the SCR trigger pulse generator). The output is derived from +5 and +12 Vdc monitors. Sheet 2 illustrates the SCR and the manner in which it grounds the +5 Vdc and +12 Vdc outputs. The +5 Vdc and +12 Vdc trigger pulse generators are essentially the same. The voltage detection devices include diodes CR32 and CR34 (which are TL430 programmable shunt regulators).

Since the +5 Vdc and +12 Vdc detection circuits are similar, only the +5 Vdc circuit is described. When the voltage at the emitter of transmitter Q19 rises above the programmed voltage of CR32 (which is set by voltage divider R83 and R84), CR32 begins to sink current from the base of Q19. This action turns Q19 on, sourcing current

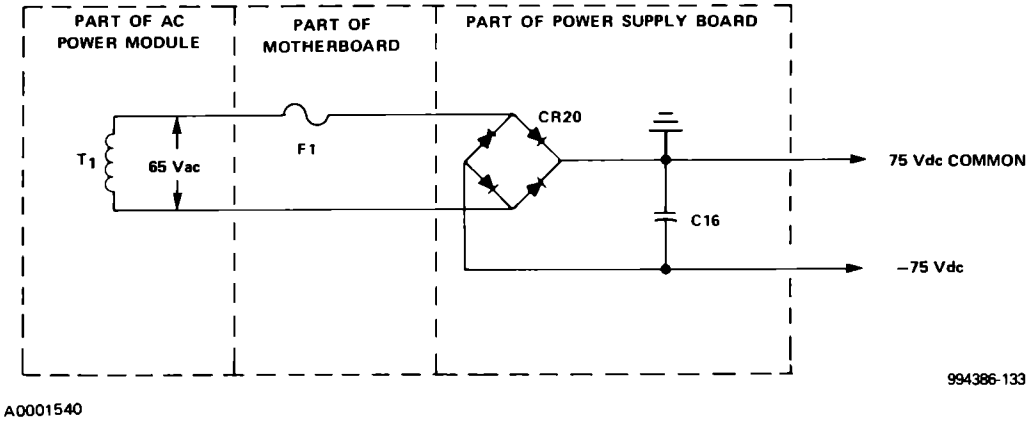

Figure K-19. −75 Vdc Supply

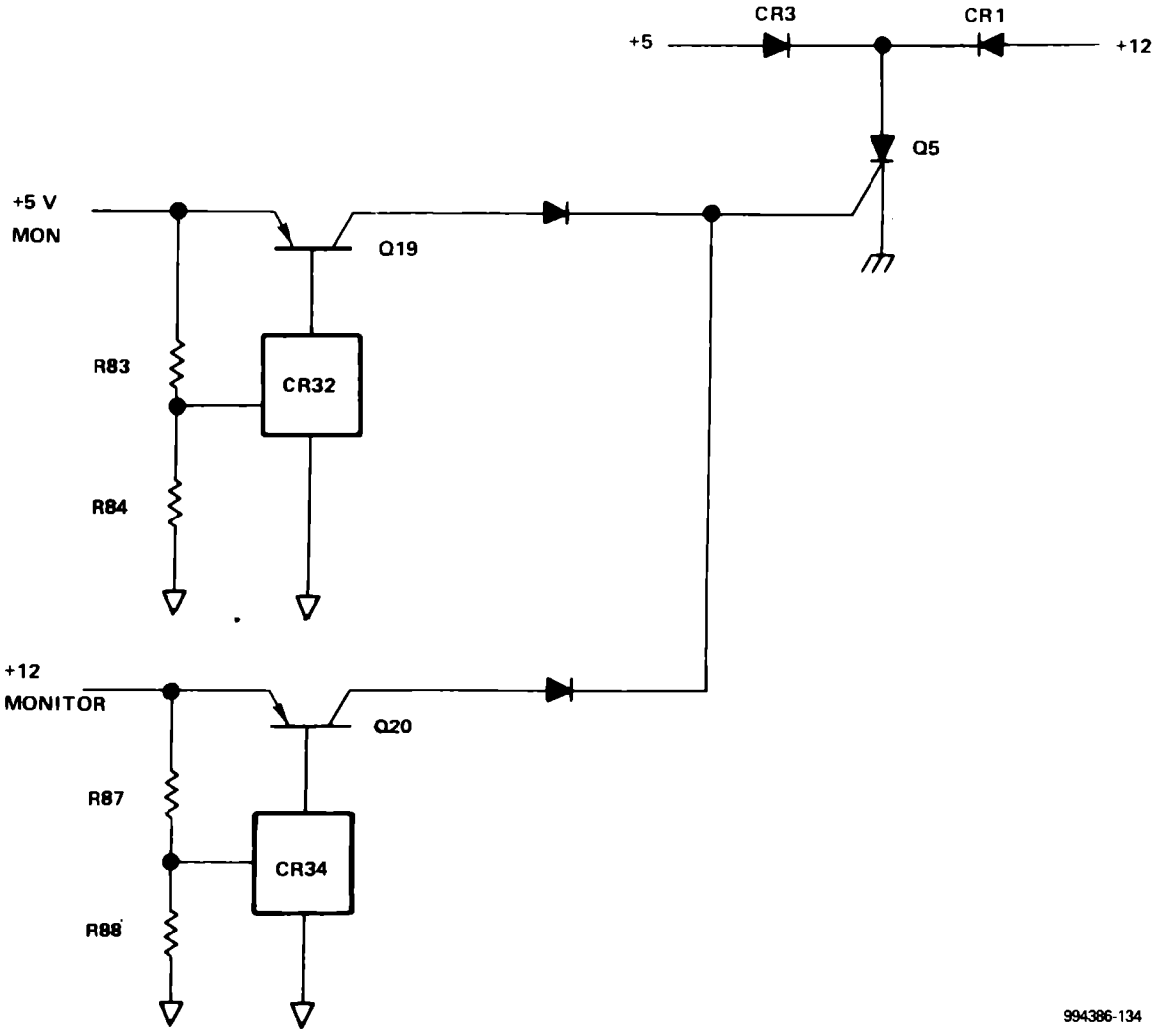

Figure K-20. Overvoltage Protection Circuit

operation. These signals are used to reset the 8080A, as an enable for the 8 SW circuit (which remotely enables the power circuits on the driver board), and to clear the control latches on the processor board. A functional block diagram of the Power-Good/Reset circuit is illustrated in Figure K-22.

The 5 Vdc enable (ENA) provides a timed delay which allows the +12 Vdc regulator to be at least in coarse regulation before the +5 Vdc line is allowed to come up. This ensures that the Power-Good/Reset circuit itself has adequate power for its own operation. The storage element in this block (C18) provides enough energy for this circuit to remain in operation during power-down or circuit malfunction (for an orderly power-down sequence). The +5 Vdc and +12 Vdc comparator circuits compare the +12 Vdc monitor and the +5 Vdc monitor lines to a voltage generated by the reference regulator block. The outputs of these comparator circuits are wire ANDed such that the +5 Vdc line and the +12 Vdc line exceed their respective minimum values for proper printer through CR33 and into the gate of Q5 (SCR). This causes Q5 to fire, grounding the +5 Vdc output and the +12 Vdc output. Q5 remains on until ac power is recycled. Figure K-20 provides a diagram of the overvoltage protection circuit.

K.1.3.8 Power-Good/Reset. The purpose of the Power-Good/Reset circuit is to provide signals to the processor board which indicate that the +5 Vdc and +12 Vdc supplies are above the minimum required levels for proper circuit operation. The Power-Good signal also controls the +8 SW power to the driver board. Figure K-21 illustrates the Power-Good and Reset signal pro-

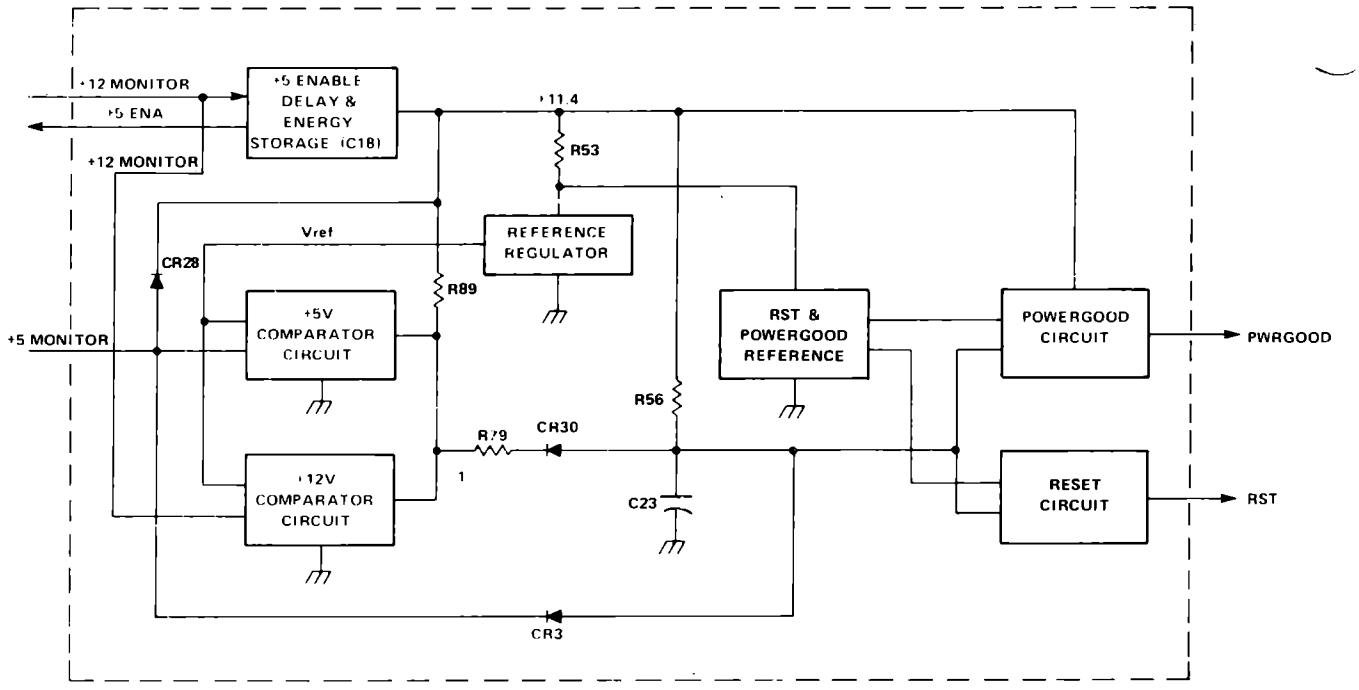

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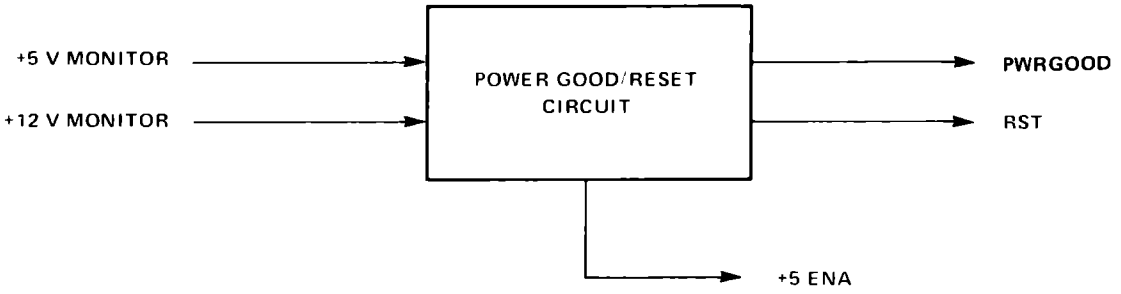
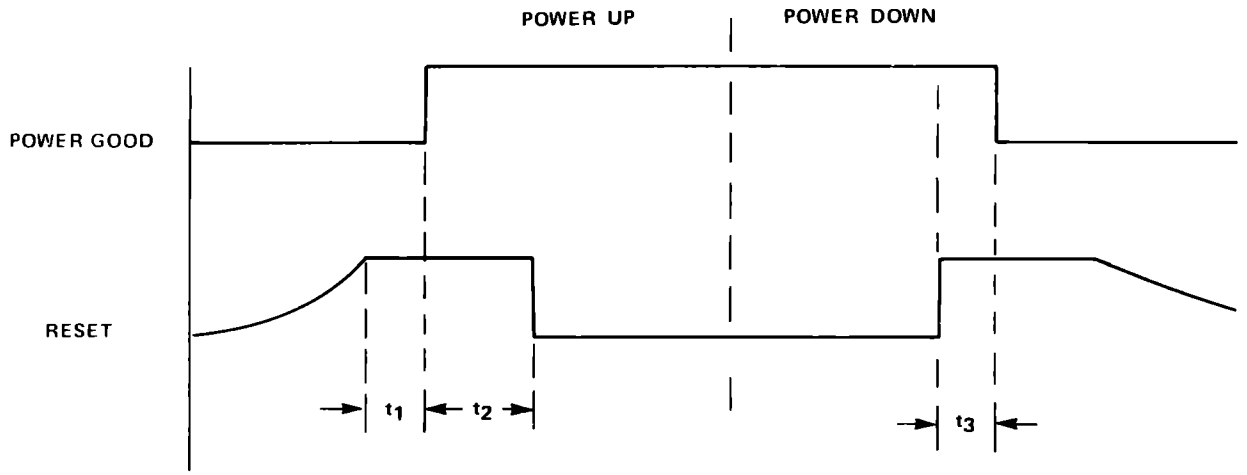
Figure K-21. Power-Good/Reset Signal Profiles





A0001531

Figure K-22. Power-Good/Reset Circuit Block Diagram

994386-61

files during power-up and power-down. The low to high transition of the Power-Good line indicates that when the +5 Vdc and +12 Vdc regulators are both within limits, and both detection circuit outputs are high, C23 begins charging through R56. The voltage ramp developed across C23 is compared to a low level reference in the Power-Good circuit comparator and a higher level reference in the reset circuit comparator. If either of the detector comparators goes low because either the +5 Vdc or the +12 Vdc line falls below its reference values, C23 discharges through R79, generating a power-down sequence. For a detailed circuit diagram of the Power-Good/Reset circuit, refer to diagram number 994392, sheet 4, Section 10.

The storage for the Power-Good/Reset circuit is provided by C18. CR26 prevents C18 from being discharged by the grounding or crowbar of the +12 Vdc monitor line. Q14 or Q15 act as an inverted Schmitt trigger. Q15 remains saturated during power-up while C19 is charging. This keeps the base of Q15 below the base of Q14 for approximately 200 msec, which provides enough time for the +12 Vdc regulator to come into regulation under normal conditions. If the +12 Vdc supply does not come up, the +5 ENA signal remains low, and the +5 Vdc regulator is not enabled. If the +11.4 Vdc line is grounded, C19 is discharged through CR27 and the +5 ENA line immediately goes low, disabling the +5 Vdc regulator.

CR29 and R53 provide the constant reference voltage for use by all of the comparator circuits. This ramp is applied to the inputs of the Power-Good and Reset comparator circuits, which are also configured as voltage comparators with hysteresis. The output of the Power-Good comparator (AR2) is buffered by Q17 and Q18 to provide the necessary current sink capability. The output of the Reset comparator goes directly to the microprocessor. CR31 provides immediate discharge of C23 in the event of a system overvoltage.

K-22

NOTES: UNLESS OTHERWISE SPECIFIED

1. MAX. LEAD LENGTH TO BE .062 FROM CONDUCTOR SIDE OF BOARD.
2. DO NOT SOLDER ON COMPONENT SIDE.
3. ~~INSTALL EJECTORS (ITEMS 123&124) AFTER PROCESS 2.~~
4. MASK ALL CONN FINGERS ON BOTH SIDES OF BOARD WHEN SOLDERING TO PREVENT SOLDER FROM WICKING DOWN CONN FINGERS.
5. MARK ASSEMBLY SITE/DATE CODE IN LOCATION SHOWN. PER PROCESS 1 AND ITEM 139 PARAGRAPH 4.0
6. MARK APPROPRIATE REVISION LETTER IN LOCATION SHOWN PER PROCESS 1 AND REVISION LEVEL BLOCK
7. HEATSINK MUST BE SQUARELY ON LOCATION AND MUST NOT TOUCH AND SHORT OUT ADJACENT COMPONENT LEADS OR CONDUCTOR RUNS
8. MOUNT DISC (ITEM 24) TO SUPPORT ITEM (ITEM 119) USING SILICONE (RTV) (ITEM 101). 3 POSTS ON SUPPORT USED TO CENTER DISC. DISC SHOULD NOT TOUCH POSTS ON SUPPORT.
9. TORQUE TO 5±1 INCH-POUNDS
10. TORQUE TO 28±2 INCH-POUNDS
11. R97 IS OPTIONAL, NOT INSTALLED
12. TORQUE TO 3.5±.5 INCH-POUND MAX
13. ~~TORQUE TO 8 IN/LBS MAX~~
14. APPROXIMATELY 1/8" LENGTH OF TUBING ON EACH LEAD
15. ITEM 150 CONSISTS OF COMPONENTS WHICH ARE AUTO INSERTED AND ARE CONTAINED IN THE -5000 SERIES LM.

DWG NO	SH
994394	1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
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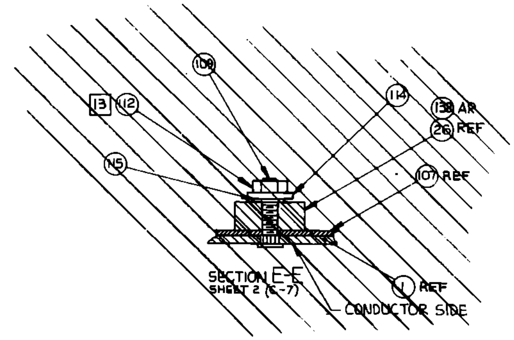
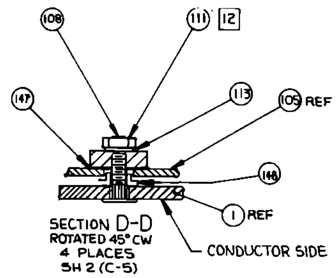
(I)	LM AND ZD-2 DELE ITEM 133 [illegible]	[illegible]	[illegible]



SECTION E-E
SHEET 2 (C-7)



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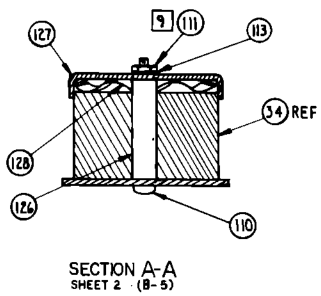
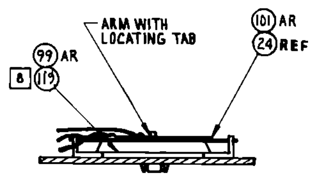
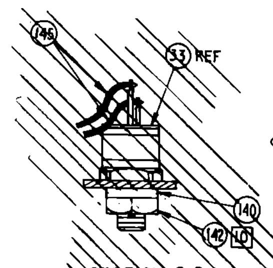
4 PLACES
SH 2 (C-5)



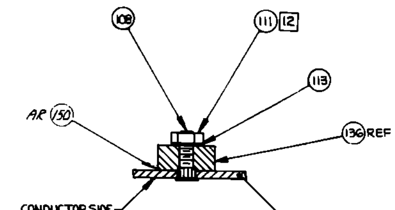
SECTION A-A
SHEET 2 (B-5)



VIEW B-B
ROTATED 90° CW
SHEET 2 (C-2)
16



SECTION C-C
ROTATED 90° CW
SHEET 2 (B-3)



SECTION F-F
ROTATED 90° CCW
SH 2 (B-6)

15

PART NUMBER	DESCRIPTION
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994394-0001	POWER SUPPLY

REV STATUS OF SHEETS				
REV	V			
SH	1	2		

SEQ NO	IDENT	F-SPEC	NO	ADDITIONAL
3	SLDR	127-01	00	
2	SLDR	124-02	00	
1	MARK	100-02	21	HEIGHT: .06; COLOR: BLACK
	PROCESS		CLASSIFICATION	

PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS SEE TI DRAWING 729467

REVISION LEVEL

DIAGRAM	D	D	E	E	Y
ASSEMBLY	P	S	T	U	V

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

NEXT ASSY	USED ON
994293	8733
994292	8733

APPLICATION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES: ANGLES ±1°; 3 PLACE DECIMALS ±.010; 2 PLACE DECIMALS ±.02
- INTERPRET DRAWING PER MIL-D-1000
- REMOVE ALL BURRS AND SHARP EDGES
- CONCENTRICITY MACHINED DIAMETERS .010 FIM
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

HOLE TOLERANCE

.013 THRU .125: .004 / .001	.126 THRU .250: .005 / .001	.251 THRU .500: .006 / .001		
.501 THRU .750: .008 / .001	.751 THRU 1.000: .010 / .001	1.001 THRU 2.000: .012 / .001		

	DATE
[illegible]	12-29-76
[illegible]	1/21/77
[illegible]	1/4/77
[illegible]	1/4/77
[illegible]	1-24-77
[illegible]	1/11/77
[illegible]	1/26/77

TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

POWER SUPPLY

SIZE	FSCM NO	DRAWING NO
D	96214	994394

SCALE 2/1 — SHEET 1 OF 2

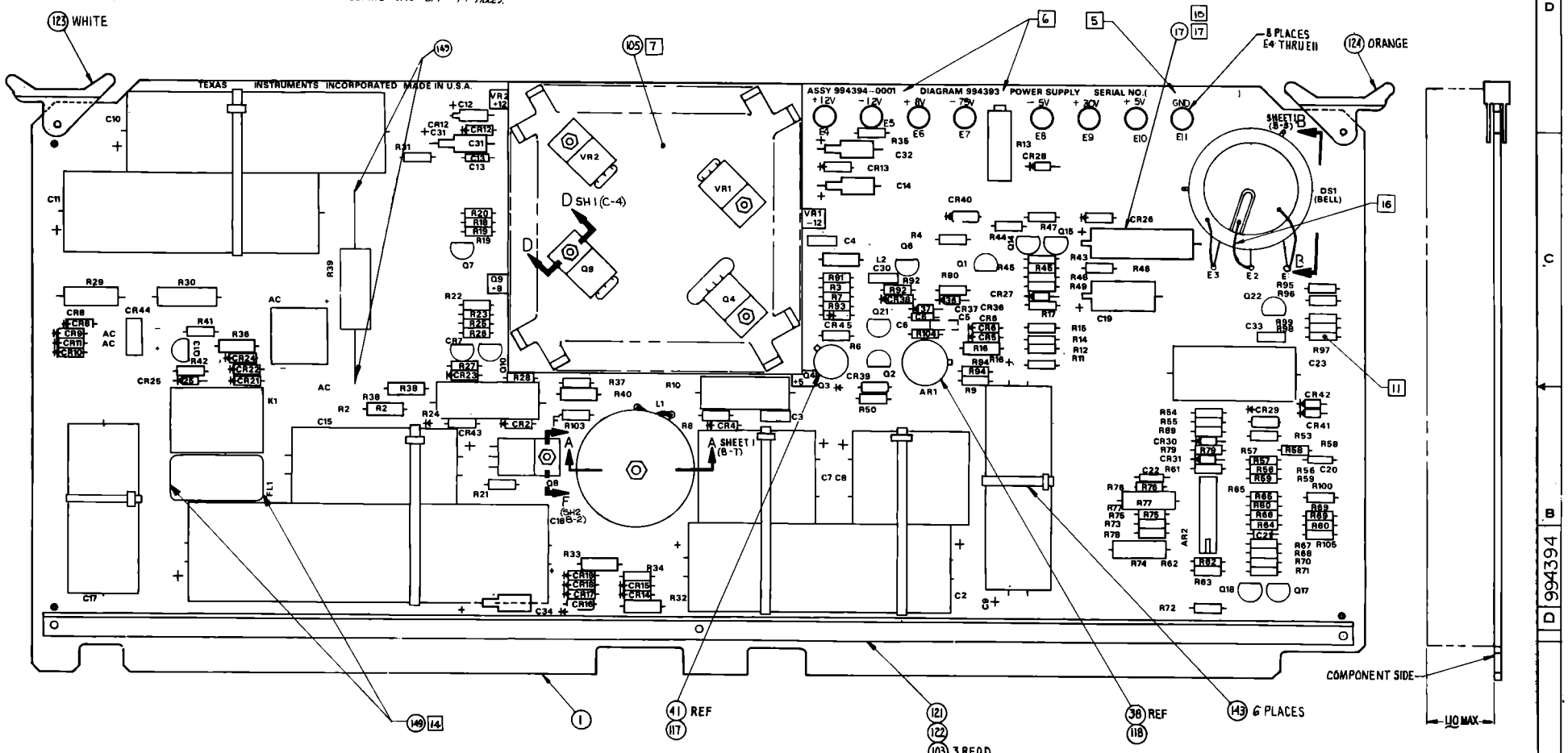
LM

16 TO INSTALL BELL, LINE UP CENTER PRONGS WITH LARGE HOLE IN PC. BOARD AND LINE UP LOCATING TAB WITH SMALL HOLE, THEN PRESS CENTER OF BELL TILL PRONGS HAVE SEATED IN HOLE. SOLDER THE FOLLOWING WIRES; YELLOW OUTSIDE SECTION TO E3, SMALL WHITE INSIDE SECTION TO E2, LARGE WHITE INSIDE SECTION TO E1. NEATLY R.T.V. (ITEM 101) EXTRA WIRE LENGTH TO BOARD KEEPING R.T.V. OFF PT HOLES.

17 MOUNT CAPACITOR FLUSH TO BOARD AND NOT TOUCHING BELL

18 SOLDER 4/32" OF NEGATIVE LEAD TO GROUND PLANE USEING ACCEPTABLE WORKMANSHIP STANDARDS

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED



SIZE	CODE IDENT NO	DRAWING NO	REV
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SCALE 2/1		SHEET 2	

D 994394

LIST OF MATERIALS

AUGUST 27, 1980

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ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION.....	UM
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0003	REF	0983412-9901	REVISION LEVEL STATUS,MC810/ATS	EA
0004	00001.000	0972965-0004	CAP FIX CERAMIC 2200 PF 10% 200V	EA
			QPL - CK06BX222K	
0004A			C33	
			QPL - CK06BX222K	
0005	00001.000	0972663-0001	NETWORK,LM339N	EA
0005A			AR2	
0007	00002.000	0972929-0385	CAP FIX CERAMIC 220 PF 10% 200V	EA
			SEE - TI DRAWING	
0007A			C5,C30	
			SEE - TI DRAWING	
0008	00001.000	0972965-0012	CAP FIX CERAMIC .010 MF 10% 200V	EA
			QPL - CK06BX103K	
0008A			C3	
			QPL - CK06BX103K	
0010	00001.000	0972965-0024	CAP FIX CERAMIC .100 MF 10% 100V	EA
			QPL - CK06BX104K	
0010A			C4	
			QPL - CK06BX104K	
0012	00001.000	0419051-0474	CAP FIX FILM FOIL .470 UF 5% 200VDC	EA
			TRW - 663UW	
0012A			C23	
			TRW - 663UW	
0015	00001.000	0996335-0001	CAP FIXED 12.0MF 100V	EA
0015A			C17	
0016	00001.000	0972924-0011	CAP FIX TANT SOLID 68 MFD 10 % 15 VOLT	EA
			QPL -M39003/1-2274	
0016A			C19	
			QPL -M39003/1-2274	
0017	00001.000	0996681-0002	CAP,AL-ELECTROLYTIC,15V,1000MFD,.38 OHMS	EA
			090201-SEE DRAWING	
0017A			C18	
			QPL -M39003/1-2277	
0018	00001.000	0996479-0001	CAP,FIXED 850MF 125V	EA
			052689-604D186	
0018A			C16	
			052689-604D186	
0019	00001.000	0972931-0093	CAP FIXED 1000 UF 50VDC -10/OR+75%	EA
			SPR - 604D102G050HP	
0019A			C2	
			SPR - 604D102G050HP	
0020	00002.000	0507315-0033	CAP 1500 UF 40V 45%	EA
			-39D158G040HP5	
0020A			C10 C11	
			-39D158G040HP5	
0021	00001.000	0972931-0025	CAP FIXED 1700 10V ALUM LOW IMPEDANCE	EA
0021A			C15	
0022	00002.000	0996326-0001	CAPACITOR 2200UF 12 DCWV ELECTROLYTIC	EA
			001939-6730228H012JE5	
0022A			C7,C8	
			001939-6730228H012JE5	
0023	00001.000	0972931-0016	CAPACITOR 4400UF-10/+75% 7.5V	EA
			SEE - TI DRAWING	

LIST OF MATERIALS

AUGUST 27, 1980

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0024	00001.000	0972461-0001	DISC,SOUND-PIEZO-ELECT 3200 +/- 600 HZ	EA
			SEE - TI DRAWING	
0024A			DS1	
			SEE - TI DRAWING	
0025	00001.000	0996329-0001	IC,TL430CLP PROGRAMMABLE SHUNT,REGULATOR	EA
			SEE TI- DRAWING	
0025A			CR7	
			SEE TI- DRAWING	
0026	00001.000	0996318-0001	BRIDGE RECTIFIER,2AMP FULL-WAVE	EA
			027777-VS248	
0026A			CR20	
			027777-VS248	
0029	00001.000	0996281-0006	RECTIFIER,SS3892/UES1307,V(R)100V I(O)6A	EA
			014099-SS3892	
0029A			CR4	
			014099-SS3892	
0034	00001.000	0996322-0001	INDUCTOR FIXED 205UH	EA
			GFS - 76205-1	
0034A			L1	
			GFS - 76205-1	
0035	00003.000	0972057-0001	TRANSISTOR-A5T2222 NPN SILICON	EA
			1640-2132-000	
0035A			Q6 Q18 Q22	
			1640-2132-000	
0036	00004.000	0996337-0001	XST A5T2243	EA
			TI -A5T2243	
0036A			Q1 Q2 Q7 Q10	
			TI -A5T2243	
0037	00005.000	0800523-0001	TRANSISTOR A5T2907 PNP SILICON	EA
			TI- -A5T2907	
0037A			Q13 Q14 Q15 Q17 Q21	
			TI- -A5T2907	
0038	00001.000	0222224-0305	NETWORK LM305H OPERATIONAL AMP	EA
			-LM305H	
0038A			AR1	
			-LM305H	
0039	00001.000	0972499-0002	NETWORK,VOLG REG,NEG,3 TERM-(-12V)	EA
0039A			VR1	
0040	00001.000	0996438-0002	IC,UA78M12UC VOL REG THREE TERMINAL	EA
			009404-2UA78M12UC	
0040A			VR2	
			009404-2UA78M12UC	
0041	00001.000	0996298-0001	TRANSISTOR,SGD2162 PNP SWITCHING	EA
			TI -SGD2162	
0041A			Q3	
			TI -SGD2162	
0042	00001.000	0972962-0002	TRANSISTOR TIP41C POWER AMP & HIGH-SPEED	EA
			TI -TIP41C	
0042A			Q4	
			TI -TIP41C	
0043	00001.000	0972572-0003	TRANSISTOR,TIP122 SILICON NPN DARLINGTON	EA
			TI -TIP122	
0043A			Q9	
			TI -TIP122	
0044	00001.000	0996383-0011	DIODE UZ8818 ZENER,1 WATT	EA
			012969-UZ8818	
0044A			CR39	
			012969-UZ8818	

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PART NUMBER	REV	DESCRIPTION
0994394-0001	V	POWER SUPPLY

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0069	00001.000	0996274-0002	RES 2.00 OHM .25 W 1% FIXED W/W PWR	EA
			001686-T-1/2A	
0069A			R28	
			001686-T-1/2A	
0070	00001.000	0539373-0323	RESISTOR, 226 OHMS 1% 3/8W FX,FILMED	EA
			024546-NA60 1/	
0070A			R53	
			024546-NA60 1/	
0071	00001.000	0996272-0003	RES 0.12 OHM 5 W 1% FIXED W/W PWR	EA
			001686-NT-5-74	
0071A			R10	
			001686-NT-5-74	
0097	00001.000	0972947-0089	RES FIX 10 K OHM 5% .5 W CARBON FILM	EA
			ROH - R-50	
0097A			R2	
			ROH - R-50	
0098	00002.000	0972978-0103	RES FIXED COMP 1.2K 1 WATT 5%	EA
			QPL - RCR32G122JS	
0098A			R29 R30	
			QPL - RCR32G122JS	
0099	AR	0417200-0004	PRIMER,SILICONE RUBBER-RED	PT
			COR - 1203	
0100	00001.000	0972832-0273	RES FIX 68.1 OHMS 1% 7W	EA
0100A			R24	
0101	AR	0417559-0001	SILICONE RUBBER (RTV) DOW 3140	TU
			SEE - TI DRAWING	
0102	00001.000	0972942-0026	RES FIX 4.70 K OHMS 5% 5 WATT WIREWOUND	EA
			OHM - 995-4641	
0102A			R39	
			RCL - T-10-78	
0103	00003.000	0972684-0002	SCREW,THD FRMG,HEX WSHR HD,2-56X1/4 LG	EA
0104	00001.000	0539795-0007	RES VAR CERMET 1.0 K OHMS 10 % .75 WATT	EA
			BOU -3069P-1-102	
0104A			R13	
			BOU -3069P-1-102	
0105	00001.000	0996332-0003	HEATSINK MULTIPLE DVC TO-66 CASE 12318-3	EA
			THR - 12318-3	
0106	00001.000	0996331-0001	RELAY,SPNO 3 AMP 12 VDC	EA
			082415-27A21D12	
0106A			K1	
			082415-27A21D12	
0108	00005.000	0972355-0003	STUD,CLINCH,.375 LONG,BRONZE	EA
			046384-KFH-440-6	
0110	00001.000	0972988-0121	SCREW 4-40 X.1.12 PAN HEAD CRES	EA
0111	00006.000	0411115-0044	NUT,4-40 HEXAGON CRES STEEL	EA
			MS -35649-244	
0113	00006.000	0411101-0057	LOCKWASHER # 4 EXTERNAL TOOTH CRES	EA
			QPL - MS35335-57	
0117	00001.000	0184262-0001	PAD,MOUNTING,TO-5, 4 LEAD,RED	EA
			THR - 7717-5	
0118	00001.000	0537402-0001	X INSULATOR DISK,8 LEAD,STANDOFF	EA
			THR - 7717-122N	
0119	00001.000	0983910-0001	SUPPORT,TONE GENERATOR	EA
			1224-3910-019	
0121	00001.000	0945239-0001	BRACKET-STIFFENER, PWB, 14IN	EA
			1215-0239-035	
0122	00001.000	0966486-0001	INSULATOR PWB STIFFENER	EA
			1215-0486-035	

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PART NUMBER	REV	DESCRIPTION
0994394-0001	V	POWER SUPPLY

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0123	00001.000	0413277-0001	EJECTOR,PCB,NON-LOCKING,WHITE	EA
			SCA -S-200(NATURAL)	
0124	00001.000	0413277-0004	EJECTOR,PCB,NON-LOCKING,ORANGE	EA
			SCA -S-200(ORANGE)	
0125	00001.000	0996330-0001	NETWORK 22 OHMS 10% #22 AWG SOLID LEADS	EA
0125A			FL1	
0126	00001.000	0416925-0411	SPACER #4 3/16 X .028 SCREW & BOLT	EA
0127	00001.000	0972306-0002	COVER ROUND	EA
0128	00001.000	0972621-0002	SPRING RING	EA
			5360-2000-000	
0132	00001.000	0972946-0061	RES FIX 680 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0132A			R20	
			ROH - R-25	
0136	00001.000	0996450-0001	TRANSISTOR TIP115,P-N-P DARLINGTON	EA
			001295-TIP115	
0136A			Q8	
			001295-TIP115	
0137	00000.000	0972806-0003	DIODE VM18 BRIDGE,DUAL-IN-LINE,1 AMP	EA
			-VM18	
0137A			ITEM 137 (QTY 1) CR44 MAY	
			-VM18	
0137B			BE USED AS AN ALTERNATE	
			-VM18	
0137C			FOR ITEM 30 (QTY 4) CR8,	
			-VM18	
0137D			CR9,CR10,AND CR11 ONLY	
			-VM18	
0139	REF	0994396-9901	PROCEDURE,SITE & DATE CODE SERIALIZATION	EA
0140	00001.000	0411101-0061	LOCKWASHER 1/4 EXTERNAL TOOTH CRES	EA
			QPL - MS35335-61	
0143	00006.000	0972632-0005	STRAP,TIE DOWN,CABLE-NON-STANDARD	EA
			PND - 5ST3I	
0147	00004.000	0996521-0010	INSULATOR, .147DIA .750LG .500W	EA
			055285-7403-09FR-54	
0148	00004.000	0972628-0019	WASHER, #4 ID .118 OD .250	EA
			091201-5607-50	
0149	AR	0410499-0011	INSULATION SLEEVING,TEFLON #12 NATURAL	FT
0150	00001.000	0994394-5001	AUTO-INSERTED PARTS LIST FOR 994394-1	EA
			1225-5394-098	
0151	AR	0415886-0003	GREASE,SILICONE,HEAT COND.	TU
			COR - DC 340	
9998	00001.000	0239999-9998	COST, AS REQUIRED	EA
9999	00002.000	0239999-9999	COST, SHRINKAGE	EA

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PART NUMBER	REV	DESCRIPTION
0994394-5001	V	AUTO-INSERTED PARTS LIST FOR 994394-1

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0001	00001.000	0994393-0001	PWB,POWER SUPPLY	EA
0002	00002.000	0972460-0006	DIODE E7918,SILICON,ZENER-1%	EA
			075222-E7918	
0002A			CR16 CR29	
			075222-E7918	
0003	00009.000	0972932-0001	DIODE 1N914B	EA
			SEE TI- DRAWING	
0003A			CR25 CR27 CR30 CR31 CR36	
			SEE TI- DRAWING	
0003B			CR37 CR38 CR41 CR42	
			SEE TI- DRAWING	
0004	00021.000	0539468-0002	DIODE,1N4002 1AMP 100PIV RECTIFIER	EA
			TI - IN4002	
0004A			CR2 CR5 CR6 CR8 CR9	
			TI - IN4002	
0004B			CR10 THRU CR15 CR17 CR18	
			TI - IN4002	
0004C			CR19 CR21 CR22 CR23 CR26	
			TI - IN4002	
0004D			CR28 CR43 CR45	
			TI - IN4002	
0005	00001.000	0539812-0050	RES,FIXED 239 OHMS .1% MF 1/8W	EA
			TI -MC55C	
0005A			R55	
			TI -MC55C	
0006	00001.000	0539812-0049	RES,FIXED 761 OHMS .1% MF 1/8W	EA
			TI -MC55C	
0006A			R54	
			TI -MC55C	
0007	00001.000	0539812-0052	RES FIXED 1.19K OHMS .1%	EA
			TI -MC55C	
0007A			R78	
			TI -MC55C	
0008	00001.000	0539812-0051	RES FIXED 3.42K OHMS .1%	EA
			TI -MC55C	
0008A			R75	
			TI -MC55C	
0009	00002.000	0539812-0057	RES FIXED 10K OHMS .1%	EA
			TI -MC55C	
0009A			R73 R76	
			TI -MC55C	
0010	00001.000	0539370-0346	RES FIX FILM 392 OHM 1% .25 WATT	EA
			COR - NA55	
0010A			R59	
			COR - NA55	
0011	00001.000	0539370-0364	RES FIX FILM 604 OHM 1% .25 WATT	EA
			COR - NA55	
0011A			R60	
			COR - NA55	
0012	00001.000	0539370-0369	RES FIX FILM 681 OHM 1% .25 WATT	EA
			COR - NA55	
0012A			R46	
			COR - NA55	
0013	00002.000	0539370-0385	RES FIX FILM 1.00K OHM 1% .25 WATT	EA
			COR - NA55	
0013A			R27 R57	
			COR - NA55	
0014	00001.000	0539370-0434	RES FIX FILM 3.24K OHM 1% .25 WATT	EA
			COR - NA55	
0014A			R14	
			COR - NA55	

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PART NUMBER REV DESCRIPTION.....
0994394-5001 V AUTO-INSERTED PARTS LIST FOR 994394-1

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION.....	UM
0015	00001.000	0539370-0450	RES FIX FILM 4.75K OHM 1% .25 WATT	EA
			COR - NA55	
0015A			R43	
			COR - NA55	
0016	00001.000	0539370-0462	RES FIX FILM 6.34K OHM 1% .25 WATT	EA
			COR - NA55	
0016A			R12	
			COR - NA55	
0017	00001.000	0539370-0481	RES FIX FILM 10.0K OHM 1% .25 WATT	EA
			COR -NA55D-100PPM/C	
0017A			R45	
			COR -NA55D-100PPM/C	
0018	00001.000	0539370-0577	RES FIX FILM 100 K OHM 1% .25 WATT	EA
			COR - NA55	
0018A			R56	
			COR - NA55	
0019	00002.000	0972936-0414	RES 1.00 M-OHM .125W 1% FIXED FILM	EA
			81349R-NC55H1004FM	
0019A			R62 R66	
			81349R-NC55H1004FM	
0020	00002.000	0972937-0419	RES 1.13 M-OHM .25 W 1% FIXED FILM	EA
			81349R-NC60H1134FM	
0020A			R74 R77	
			81349R-NC60H1134FM	
0021	00002.000	0972946-0017	RES FIX 10.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0021A			R7 R99	
			ROH - R-25	
0022	00003.000	0972946-0027	RES FIX 27.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0022A			R11 R15 R23	
			ROH - R-25	
0023	00001.000	0972946-0034	RES FIX 51.0 OHM 5 % .25 W.CARBON FILM	EA
			ROH - R-25	
0023A			R93	
			ROH - R-25	
0024	00007.000	0972946-0041	RES FIX 100 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0024A			R50 R58 R69 R79 R100 R104	
			ROH - R-25	
0024B			R105	
			ROH - R-25	
0025	00001.000	0972946-0048	RES FIX 200 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0025A			R47	
			ROH - R-25	
0026	00003.000	0972946-0057	RES FIX 470 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0026A			R68 R71 R72	
			ROH - R-25	
0027	00011.000	0972946-0065	RES FIX 1.0K OHM 5% .25 W CARBON FILM	EA
			ROH - R-25	
0027A			R4 R17 R19 R21 R25 R31 R34	
			ROH - R-25	
0027B			R35 R37 R42 R103	
			ROH - R-25	
0028	00001.000	0972946-0058	RES FIX 510 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0028A			R96	
			ROH - R-25	
0029	00004.000	0972946-0072	RES FIX 2.0K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	

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PART NUMBER REV DESCRIPTION.....
0994394-5001 V AUTO-INSERTED PARTS LIST FOR 994394-1

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION.....	UM
0029A			R49 R63 R89 R92	
			ROH - R-25	
0030	00003.000	0972946-0073	RES FIX 2.2K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0030A			R67 R70 R41	
			ROH - R-25	
0031	00001.000	0972946-0082	RES FIX 5.1K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0031A			R90	
			ROH - R-25	
0032	00006.000	0972946-0089	RES FIX 10K OHM 5% .25 W CARBON FILM	EA
			1640-2132-000	
0032A			R3 R48 R61 R64 R65 R80	
			1640-2132-000	
0033	00001.000	0972946-0117	RES FIX 150K OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0033A			R95	
			ROH - R-25	
0034	00001.000	0972946-0031	RES FIX 39.0 OHM 5 % .25 W.CARBON FILM	EA
			POH - R-25	
0034A			R98	
			ROH - R-25	
0035	00003.000	0972947-0017	RES FIX 10 OHM 5 % .5 W CARBON FILM	EA
			ROH - R-50	
0035A			R16 R32 R36	
			ROH - R-50	
0036	00001.000	0972946-0053	RES FIX 330 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0036A			R44	
			ROH - R-25	
0037	00001.000	0972934-0012	DIODE,1N757A 9.1 V 5% SIL VOLT REG	EA
			QPL - 1N757A	
0037A			CR40	
			QPL - 1N757A	
0038	00004.000	0972763-0025	CAPACITOR,.10UF 50V FX,CERAMIC DIEL	EA
			COR CA-C03Z5U104Z050A	
0038A			C13 C20 C21 C22	
			COR CA-C03Z5U104Z050A	
0039	00001.000	0538429-0020	COIL RF 220 UH 7.5 OHM 103 MA LT10K	EA
			QPL - MS90538-20	
0039A			L2	
			QPL - MS90538-20	
0040	00001.000	0418356-2344	CAP FIX 0.22 MF 50V 10% TANTALUM SOLID	EA
			SEE TI- DRAWING	
0040A			C12	
			SEE TI- DRAWING	
0041	00004.000	0972924-0018	CAP FIX TANT SOLID 6.8 MFD 10 % 35 VOLT	EA
			QPL -M39003/1-2304	
0041A			C14,C31,C32,C34	
			QPL -M39003/1-2304	
0042	00001.000	0972763-0013	CAP,FIXED .010UF 50 VOLTS	EA
			004222-MC105E103Z	
0042A			C6	
			004222-MC105E103Z	
0044	00001.000	0539668-0003	DIODE,1N4003 1AMP 200PIV RECTIFIER	EA
			TI - IN4003	
0044A			CR24	
			TI - IN4003	
0045	00001.000	0972946-0015	RES FIX 8.2 OHM 5% .25W CARBON FILM	EA
			ROH - R-25	
0045A			R9	
			ROH - R-25	

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PART NUMBER	REV	DESCRIPTION
0994394-5001	V	AUTO-INSERTED PARTS LIST FOR 994394-1

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0047	00001.000	0539370-0428	RES FIX FILM 2.80K OHM 1% .25 WATT	EA
			COR - NA55	
0047A			R26	
			COR - NA55	
0049	00001.000	0972946-0005	RES FIX 3.30 OHM 5 % .25 W CARBON FILM	EA
0049A			R94	
0050	00001.000	0972946-0043	RES FIX 120 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0050A			R6	
			ROH - R-25	
0051	00001.000	0972946-0063	RES FIX 820 OHM 5% .25 W CARBON FILM	EA
			ROH - R-25	
0051A			R22	
			ROH - R-25	
0052	00001.000	0972946-0139	RES FIX 1.2M OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0052A			R91	
			ROH - R-25	
0053	00001.000	0972947-0050	RES FIX 240 OHM 5% .5 W CARBON FILM	EA
			ROH - R-50	
0053A			R33	
			ROH - R-50	
0054	00001.000	0972947-0053	RES FIX 330 OHM 5% .5 W CARBON FILM	EA
			ROH - R-50	
0054A			R8	
			ROH - R-50	
0055	00001.000	0972947-0057	RES FIX 470 OHM 5% .5 W CARBON FILM	EA
			ROH - R-50	
0055A			R38	
			ROH - R-50	
0056	00001.000	0972947-0100	RES FIX 30 K OHM 5% .5 W CARBON FILM	EA
			ROH - R-50	
0056A			R40	
			ROH - R-50	
0057	00001.000	0972946-0062	RES FIX 750 OHM 5 % .25 W CARBON FILM	EA
			ROH - R-25	
0057A			R18	
			ROH - R-25	

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PART NUMBER	REV	DESCRIPTION
0994394-8001	V	POWER SUPPLY

ITEM.	QUANTITY.	COMPONENT..	DESCRIPTION	UM
0001	00001.000	0994394-0001	POWER SUPPLY 1225-1394-098	EA

Appendix L

First-Generation Front Panels and Carriage Motor Assembly

L.1 REMOVAL AND REPLACEMENT PROCEDURES

The removal and replacement procedures for older models of the control panel, the auxiliary control panel, and the carriage drive motor are presented below.

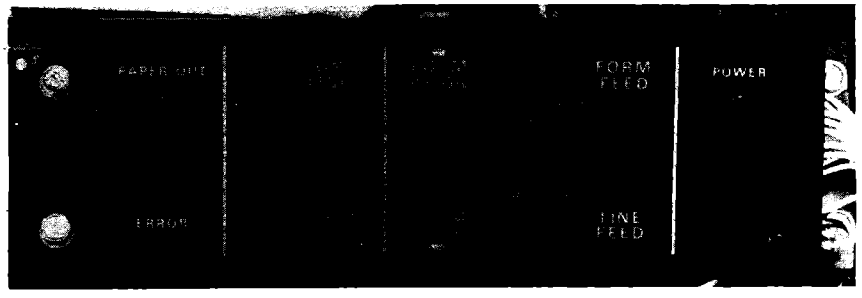
L.1.1 Control Panel Assembly

To remove the control panel assembly (TI Part No. 994251), refer to Figure L-1 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the covers (see paragraph 8.7.1).
2. Disconnect connector J6 from the Motherboard.
3. Remove the four screws securing the control panel assembly to the base.
4. Remove the control panel assembly.
5. To replace the control panel assembly, reverse the removal steps.



994386-136

Figure L-1. Control Panel Assembly

L.1.2 Auxiliary Control Panel Assembly

To remove the auxiliary control panel assembly (TI Part No. 994257), refer to Figure L-2 and proceed as follows.

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the cover (see paragraph 8.7.1).
2. Remove connector J2 from the Motherboard.
3. Remove the three screws securing the auxiliary control panel assembly to the base.
4. Remove the auxiliary control panel assembly.
5. To replace the auxiliary control panel assembly, reverse the removal steps.

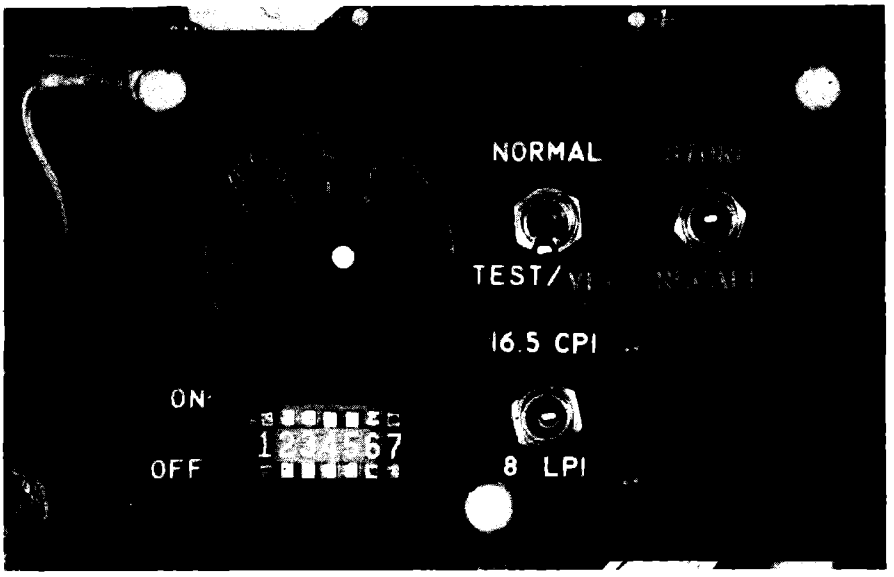


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Figure L-2. Auxiliary Control Panel

L.1.3 Carriage Drive Motor Assembly

To remove the carriage drive motor assembly (TI Part No. 994238), refer to Figures L-3 and L-4 and proceed as follows:

WARNING

Disconnect the power cord to prevent possible electrical shock.

1. Remove the cover (see paragraph 8.7.1).
2. Disconnect the two motor power leads from the motor. (NOTE: observe wire color location to ensure correct replacement).
3. Disconnect the encoder sensor cable from the Motherboard (connects to J8).

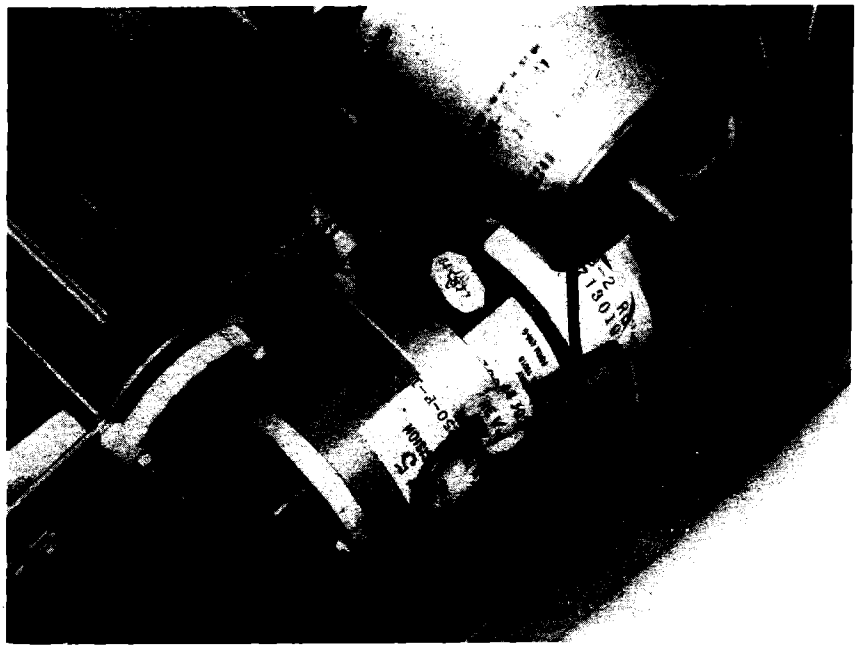

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Figure L-3. Carriage Drive Motor

4. Push the idler pulley support girder to the right allowing the detent in the bottom of the girder to latch on the right sideplate.*

5. Remove the wire rope from the capstan by disengaging the end of the wire rope from either end of the capstan and unwrapping the wire rope.

6. Loosen the motor strap retaining screw (two or three turns). Use a long screwdriver (6-8 inches).

7. Press down on top of the motor strap to disengage the motor strap from the right sideplate.

8. Remove the screw securing the carriage drive motor assembly to the cradle and remove the carriage drive motor assembly.

9. Remove the screw securing the ground wire to the motor.

10. To replace the carriage drive motor assembly, reverse the removal steps.

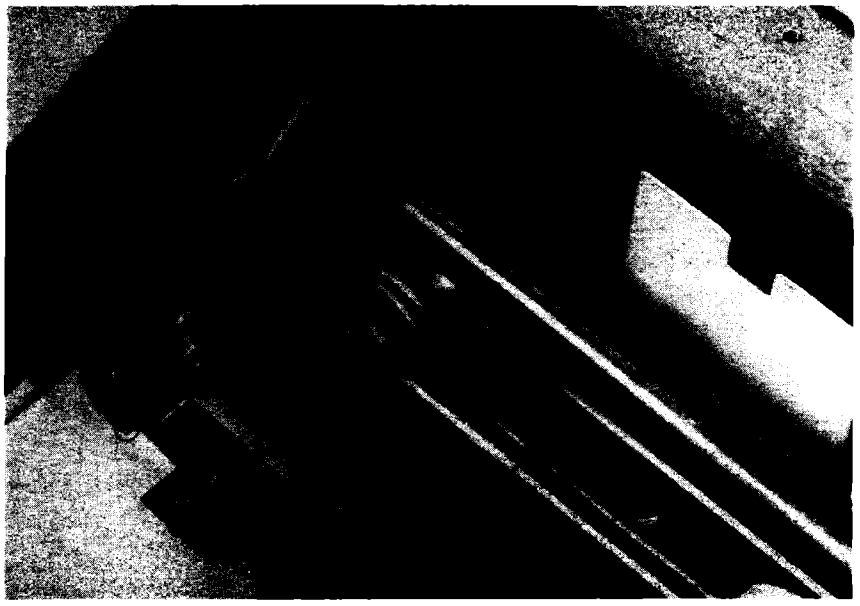

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Figure L-4. Idler Pulley

* This girder, to which the idler pulley is attached, is located at the bottom front of the printer and extends from the left sideplate to the right sideplate. Because it is held in place by a long spiral spring, it requires a definite effort to move it the required ¼ inch to the right.

Additional instructions for rewinding the wire rope follow.

1. Move the carriage to the left stop.

2. Bring the wire rope from the left side of the carriage around the idler pulley and back through the lower slot in the right sideplate.

3. Bring the wire rope from the right side of the carriage through the upper slot in the right sideplate, and (with the innermost capstan slot in the up position), place the end of the wire rope in the slot.

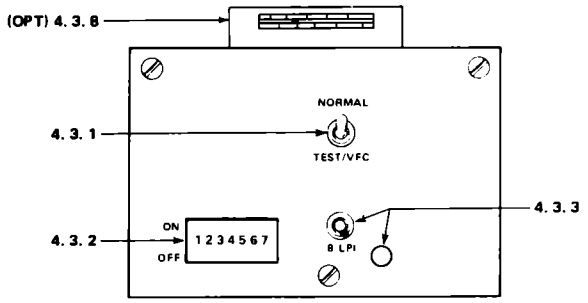
4. Wrap the wire rope counterclockwise (or allow wire rope to follow capstan groove while turning capstan clockwise) 6½ turns. The outermost capstan slot should be in the up position.

5. Bring the lower portion of the wire rope counterclockwise around the capstan 1½ turns with the rope end in the outermost capstan slot.

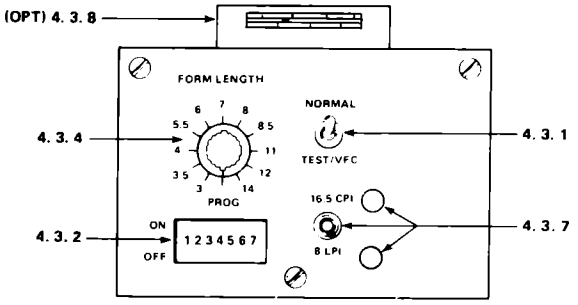
6. Carefully release the idler pulley support from the detent.

7. Manually move the carriage from stop to stop to remove the wire rope slack in the capstan.

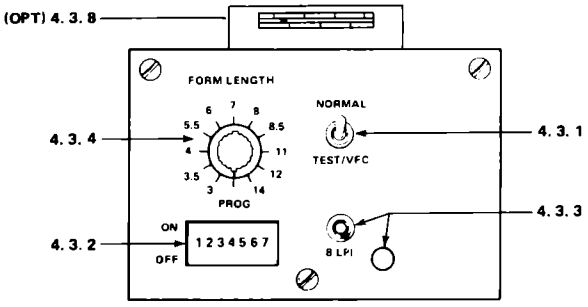
L.2 AUXILIARY CONTROL PANEL OPTIONS



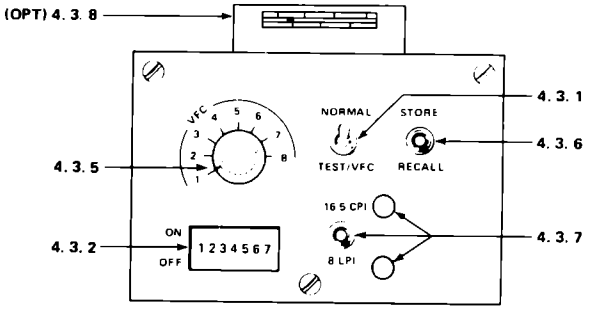
BASIC (994292–0001) BSC



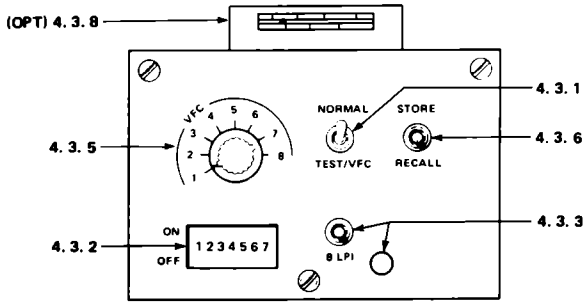
FORMS LENGTH AND COMPRESSED PRINT (994293–0001) FCO



FORMS LENGTH (994292–0002) FLO



VERTICAL FORMAT CONTROL AND COMPRESSED PRINT (994293–0002) VCO



VERTICAL FORMAT CONTROL (994292–0003) VFC

NOTE:

1. AUXILIARY CONTROL PANELS ARE IDENTIFIED BY TYPE OF OPTION, PRINTER PART NUMBER AND CONFIGURATION CODE.
2. REFER TO PARAGRAPHS CALLED OUT BY PARAGRAPH NUMBER FOR CONTROL FUNCTION EXPLANATION.

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994386-140

Figure L-5. Auxiliary Control Panel Options

① **NORMAL/TEST/VFC Switch.** In NORMAL position this switch enables the printer to receive data. With this switch in TEST/VFC position and serial interface mode selected, pressing the ONLINE switch causes a cyclical character test pattern (barberpole). With this switch in the TEST/VFC position and the printer OFFLINE, the alternate function switches TAB, TAB SET, TAB CLEAR, SET TOP OF FORM and LINE FEED on the control panel are enabled for vertical format control programming.

② **PENCIL Switches.** Switches 1, 2, and 3 select baud rates (see Section 3) or the optional parallel input (PLT and LBP printer). Switches 4 and 5 select odd, even or ignore parity (see Section 3). Switch 6 activates the automatic line feed override feature. Switch 7 activates the automatic top-of-form perforation skip override feature; automatic perforation skip causes the printer to skip three lines before the top of the next form. **Changes in pencil switch settings do not take effect until the printer goes OFFLINE.**

③ **8 LPI Switch/Indicator.** In the 8 LPI position this momentary, three-position, center-off switch selects either eight or six lines per inch. Lines per inch are also software programmable through the communications line (see Section 4). The indicator lights when the printer is in the 8 LPI mode.

④ **FORM LENGTH Rotary Switch.** This 12-position rotary switch permits selection of any one of the following 11 fixed form lengths: 3, 3.5, 4, 5.5, 6, 7, 8, 8.5, 11, 12, and 14 inches. In the PROG position this switch permits programming form lengths from the control panel (from 4 to 112 lines). **The program (nonstorable) is lost when power to the printer is removed.**

⑤ **VFC Switch.** This eight-position rotary switch selects one of eight, stored, vertical format programs. These eight channels are also software-programmable (see Section 4).

⑥ **STORE/RECALL Switch.** In the STORE position this momentary, three-position, center-off switch stores manually programmed vertical tabs, form length, and lines-per-inch spacing in the selected VFC channel. In the RECALL position the format program stored in the selected VFC channel is recalled into working memory. STORE and RECALL are active only when the NORMAL/TEST/VFC switch is set to TEST/VFC. Both are software programmable through the communications interface (see Section 4).

⑦ **16.5 CPI/8 LPI Switch and Indicators.** In the 16.5 CPI position this momentary, three-position, center-off switch selects the 16.5 characters-per-inch, compressed print mode. The 16.5 CPI indicator lights when the printer is in the compressed print mode. Setting this switch to the 16.5 CPI position a second time returns the printer to the standard 10-characters-per-inch print mode. The printhead returns to the left margin each time a change is made in characters-per-inch. In the 8 LPI position, this switch selects the eight or six-lines-per-inch mode alternately. The 8 LPI indicator lights when the printer is in the eight-lines-per-inch mode. All modes are software programmable through the communications interface (see Section 4).

SOFTWARE COMMANDS*

Command	ASCII Code Characters Received	Printer Action Taken
Carriage Return	CR	This command causes data if any in the line buffer to be printed Because of the bidirectional printing capability of the printer a carriage return is not executed Instead the carriage stops upon completion of printing a line When the next line is received the carriage is positioned to print forward or backward whichever requires the least carriage movement
Delete	DEL	This command clears the line buffer If the NDE (no delete) option has been enabled, this command will be ignored
Deselect	DC3 (See Note 3)	This command deselects the printer causing it to ignore all incoming data and control characters except DC1 (select) after printing out the contents of the line buffer
Form Feed	FF	This command causes data if any in the line buffer to be printed and advances the paper to the top of the next form
Form Length Set	ESC+2+n (See Note 1)	This command sets the form length used by the Form Feed (FF) command to n lines (4 to 112 lines)
Horizontal Tab	HT	This command causes spaces to be entered in the line buffer up to the next horizontal tab location where printing will begin
Horizontal Tab Set	ESC+3+n_1 +n_2 +n_k+ NUL (See Note 1)	This command clears all existing horizontal tabs and sets new tabs at columns n_1 n_2 and n_k (column 1 through 126)
Line Feed	LF	This command causes data if any in the line buffer to be printed and advances the paper one line space
Line Width Set	ESC+ +n (See Note 1)	This command causes the printer to print lines n columns wide (Line width is automatically set to 132 columns at power up)
Line Width 132	ESC+	This command causes the printer to print lines 132 columns wide (Line width is automatically set to 132 columns at power up)
Null	NUL	This command terminates the tab setting sequence for both horizontal and vertical tabs otherwise it is ignored

NOTE 1 The number n as used in the DC2 DC4 ESC 1 and ESC 2 ESC 3 and ESC commands represents a seven bit binary number See table below for the ASCII character code which will transmit the desired binary number

SOFTWARE COMMANDS* (Concluded)

Command	ASCII Code Characters Received	Printer Action Taken
Recall	ESC+9+N (See Note 2)	This command recalls the stored vertical format information in the optional VFC channel N memory to the working memory If the VFC option is not installed this command is ignored
Select	DC1 (See Note 3)	When power is applied to the printer this command selects the printer enabling it to receive data
Store	ESC+8+N (See Note 2)	This command stores vertical format information from the working memory in the optional VFC channel N memory If the VFC option is not installed this command is ignored
Tab To Address	DC4+n (See Note 1)	This command causes spaces to be entered in the line buffer from the present column up to a column n n must be greater than the present column If n is less than the present column this command will be ignored
Tab To Line	DC2+n (See Note 1)	This command causes the paper drive system to slew to the line specified by n after printing contents of the line buffer (n must be greater than the present line) If n is less than the present line this command will be ignored
Vertical Tab	VT	This command causes data if any in the line buffer to be printed and advances the paper to the next vertical tab location or top of form whichever occurs first If no vertical tabs are set this command causes the paper to be advanced to top of form
Vertical Tab Set	ESC+1+n_1 +n_2 +n_k +NUL	This command clears all existing vertical tabs and sets new tabs at lines n_1 n_2 and n_k
6 LPI	ESC+4	This command sets the paper drive system to 6 lines per inch (The paper drive system is automatically set to 6 lines per inch at power up)
8 LPI	ESC+5	This command sets the paper drive system to 8 lines per inch
10 CPI	ESC+6	This command sets the carriage system to 10 characters per inch (The carriage system is set to 10 characters per inch at power up)
16 5 CPI	ESC+7	This command sets the carriage system to 16 5 characters per inch
EXP	SO	With the expanded print option installed this command sets carriage system to the expanded print mode The SO control character will be recognized only if it is the first character of the new line

NOTE 2 The number N as used in the ESC 8 and ESC 9 commands represents the ASCII coded numbers from one through eight which correspond to the selected VFC channel

NOTE 3 The DC3 strappable option disables this feature

994386-143

Figure L-6. Software for the Model 810 Printer

***SPECIAL SOFTWARE PROVISIONS FOR PRINTERS WITH LINE BUFFER OPTION**

1. DC2 and all ESC (Escape) commands must be terminated with CR (Carriage Returns).
2. The DSC strappable option must be enabled to initiate printing when FF, LF, or VT commands are received.
3. Line width cannot be varied for printers with Line Buffer option.

COLUMN OR LINE "n" NUMBER CONVERSION

For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character	For Column Or Line Number	Send ASCII Code Character
1	SOH	26	SUB	51	3	76	L	102	f
2	STX	27	ESC	52	4	77	M	103	g
3	ETX	28	FS	53	5	78	N	104	h
4	EOT	29	GS	54	6	79	O	105	i
5	ENQ	30	RS	55	7	80	P	106	j
6	ACK	31	US	56	8	81	Q	107	k
7	BEL	32	SPACE	57	9	82	R	108	l
8	BS	33	!	58	:	83	S	109	m
9	HT	34	"	59	;	84	T	110	n
10	LF	35	#	60	<	85	U	111	o
11	VT	36	$	61	=	86	V	112	p
12	FF	37	%	62	>	87	W	113	q
13	CR	38	&	63	?	88	X	114	r
14	SO	39	'	64	@	89	Y	115	s
15	SI	40	(	65	A	90	Z	116	t
16	DLE	41	)	66	B	91	[	117	u
17	DC1	42	*	67	C	92	\	118	v
18	DC2	43	+	68	D	93	]	119	w
19	DC3	44	,	69	E	94	^	120	x
20	DC4	45	–	70	F	95		121	y
21	NAK	46	.	71	G	96		122	z
22	SYN	47	/	72	H	97	a	123	{
23	ETB	48	0	73	I	98	b	124	¦
24	CAN	49	1	74	J	99	c	125	}
25	EM	50	2	75	K	100	d	126	~
						101	e		

OMNI 800

electronic data terminals

MODEL 810 PRINTER
QUICK REFERENCE CARD

TEXAS INSTRUMENTS
INCORPORATED

P/N 994482-9701
REV D, October 1980

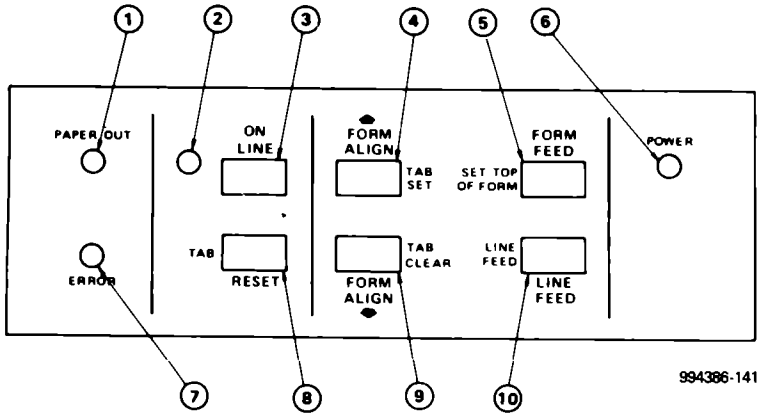

Figure L-7. Control Panel (CP)

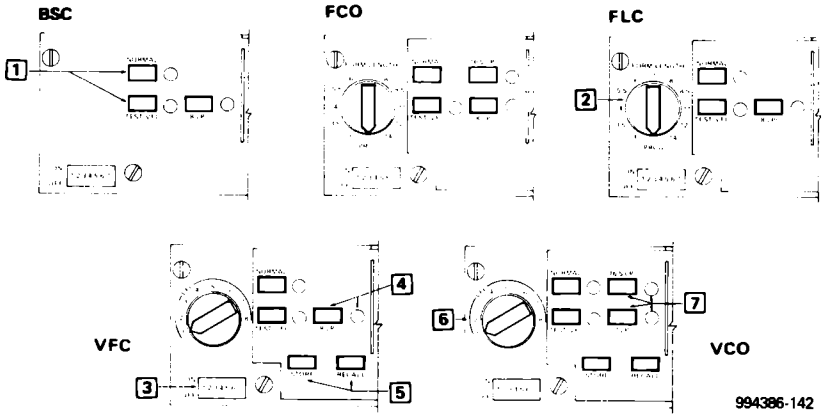

Figure L-8. Auxiliary Control Panel (ACP)

CONTROL PANEL (CP) CONTROLS AND INDICATORS

(1) Indicator lights when PAPER OUT switch is actuated.
(2) Indicator lights when printer is ON LINE.
(3) Switch alternately sets ON/OFF LINE. When TEST/VFC is activated, pressing ON LINE starts barberpole printout, provided baud rate is set [3].
(4) Switch active both ON/OFF LINE. Alternately moves paper up or sets vertical tab. SET TAB function enabled when TEST/VFC activated on ACP.
(5) Switch active both ON/OFF LINE. Alternately moves paper to top of next form (FORM FEED) or sets TOP OF FORM. SET TOP OF FORM function when TEST/VFC activated on ACP.
(6) Indicator lights when power is applied to printer.
(7) Steady light indicates input parity error. Blinking light indicates carriage jam or other carriage control malfunction.
(8) Switch alternately resets logic when error is cleared or advances paper to next vertical tab if TEST/VFC switch on ACP is activated.
(9) Switch active ON/OFF LINE. Alternately moves paper down or, when TEST/VFC activated on ACP, clears tab at present position.
(10) Active OFF LINE only. No alternate functions. Moves paper up one line.

FUNCTION	SWITCH POSITION* 4	5
IGNORE PARITY	OFF	OFF
ODD PARITY	ON	ON
EVEN PARITY	ON	OFF

*See [3]

FORM LENGTH AND VERTICAL TAB SETTING

1. Press Form Feed (5).
2. Using a convenient reference point, align top of form with Form Align ↑ (4) and ↓ (9).
3. Set Auxiliary Control Panel Normal/Test/VFC switch [1] to TEST/VFC mode.
4. If 8 LPI is desired, select with [4].
5. Press Set Top of Form (5).
6. Press Line Feed (10) until line to be tab-set is correctly positioned in reference to printhead. (Approximately 3 and 4 lines below top of ribbon guide on printhead carriage for 6 and 8 LPI respectively.)
7. Press Tab Set (4).
8. Repeat steps 6 and 7 as necessary to set all desired tabs.
9. With Line Feed (10) step paper to top of next form using same reference point as in 2. Press (5). This sets form length.
10. Set Auxiliary Control Panel Normal/Test/VFC switch [1] to NORMAL. This enters data into working memory.
11. Verify tab settings:
    a. Repeat steps 1 to 3 above.
    b. Press tab (8). If Tab is correct, press Tab (8) for next tab. If tab setting is incorrect, press (9) to clear and reenter tab per steps 6 and 7.
12. When (8) is pressed after last tab is verified, paper will move to top of next form.
13. Set Auxiliary Control Panel Normal/Test/VFC [1] to NORMAL.
14. If print is not centered exactly on form ↑ (4) and ↓ (9) can be used to adjust form while printing.

MODEL 810 PRINTER QUICK REFERENCE CARD

AUXILIARY CONTROL PANEL (ACP) CONTROLS AND INDICATORS

[1] NORMAL position for routine printer operation. In TEST/VFC, pressing ON LINE switch on CP starts barberpole printout. In TEST/VFC, with ON LINE switch OFF, TAB, TAB SET, TAB CLEAR, TOP OF FORM and LINE FEED are enabled on CP.
[2] Selects one of 11 fixed form lengths. In PROG, operator can program form lengths.
[3] Switches 1, 2, 3 select baud rate or parallel input. Switches 4 and 5 select parity. Switch 6 activates auto line feed. Switch 7 activates auto perforation skip.
[4] Alternately selects 8 or 6 lines per inch. Light ON in 8 LPI mode.
[5] In STORE position, stores manually programmed vertical tabs, form length and LPI in selected VFC channel. In RECALL position, activates format program stored in selected VFC channel. TEST/VFC switch must be activated.
[6] Eight-position rotary switch selects stored non-volatile vertical format programs.
[7] Selects compressed print mode (16.5 characters per inch) or, alternately, normal print mode (10 CPI). Indicator displays selected print mode. Also (see [4]).

BAUD RATE STANDARD	BAUD RATE BRO*	SWITCH POSITION 1	2	3
110	110	OFF	OFF	OFF
150	200	ON	OFF	OFF
300	300	OFF	ON	OFF
1200	1200	ON	ON	OFF
2400	2400	OFF	OFF	ON
4800	600	ON	OFF	ON
9600	9600	OFF	ON	ON
PARALLEL		ON	ON	ON

*Baud Rate Option

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Part No. 994386-0001

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